TMS320C6000 EMIF-to-External SDRAM Interface

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ABSTRACT

Interfacing external SDRAM to the Texas Instruments TMS320C6000™ digital signal processor (DSP) is simple, compared to previous generations of TI DSPs, because of the advanced external memory interface (EMIF). The EMIF is a glueless interface to a variety of external memory devices.

This application report describes the EMIF's control registers and SDRAM signals along with SDRAM functionality, including functions supported by the EMIF and performance considerations when used with the EMIF.

General examples include several SDRAM configurations supported by the EMIF, including timing analysis. In addition, specific examples are provided using Micron SDRAM.

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1 Interface of C6000 EMIF With SDRAM

The EMIF of all C6000™ devices offer a glueless interface to industry-standard SDRAM in the most commonly available configurations, including 16M bits x 8, 16M bits x 16, 64M bits x 16, and 64M bits x 32 devices.† Depending on the specific C6000 device, additional configurations may be supported.

1.1 C620x/C670x Compatible Memory Types

The C620x/C670x EMIF supports a glueless interface to a 16M-bit, 2-bank and a 64M-bit, 4-bank SDRAM, offering system designers an interface to high-speed and high-density memory. Table 1 lists the possible SDRAM configurations that are fully supported by the EMIF.

As Table 1 shows, the SDRAM supported by the C620x/C670x EMIF has either eight or nine column address bits and maps into a memory space equal to or smaller than 16M bytes. Because the C620x/C670x EMIF has a 32-bit word size, four 8-bit or two 16-bit devices must be used in parallel to create a 32-bit word.

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† For a complete list of Texas Instruments DSP devices, go to the TI web site at http://www.ti.com

Table 1. C620x/C670x Compatible Memory Type Characteristics

SDRAM Size	Banks	Width	Depth	Devices/ CE	Addressable Space (M Bytes)		Column Address	Row Address	Bank Select	Pre-charge
16M bits	2	x8	1M	4	8M	SDRAM	A8−A0	A10−A0	BA0	A10
						EMIF	EA10−EA2	SDA10, EA11−EA2	EA13	SDA10
	2	x16	512K	2	4M	SDRAM	A7−A0	A10−A0	BA0	A10
						EMIF	EA9−EA2	SDA10, EA11−EA2	EA13	SDA10
64M bits	4	x16	1M	2	16M	SDRAM	A7−A0	A11−A0	BA1−BA0	A10
						EMIF	EA9−EA2	SDA10, EA13−EA2	EA15−EA14	SDA10
	4	x32	512K	1	8M	SDRAM	A7−A0	A10−A0	BA1−BA0	A10
						EMIF	EA9−EA2	SDA10, EA11−EA2	EA14−EA13	SDA10
128M bits	4	X32	1M	1	16M	SDRAM	A7−A0	A11−A0	BA1−BA0	A10
						EMIF	EA9−EA2	EA13, SDA10, EA11−EA2	EA15−EA14	SDA10

Table 1 summarizes the page characteristics of the fully supported SDRAM memory types and illustrates the EMIF-to-SDRAM pin mapping. The SDRAM uses addresses A[x:0]. These pins are mapped to EA[x+2:2] on the EMIF because the EMIF assumes that SDRAM memory spaces are 32 bits wide. The four BE signals serve as the two LSBs (least significant bits) of the external address.

A key element of the supported SDRAM memory types is that A10 is always the precharge pin. To support this functionality, the EMIF's SDRAM interface uses a pin named SDA10, instead of EA12 in the pin map, to support the necessary SDRAM operations. During row activate, SDA10 is logically equivalent to EA12. For other SDRAM operations, SDA10 is used as the precharge pin.

1.2 C621x/C671x Compatible Memory Types

The C621x/C671x EMIF supports a glueless interface to almost any configuration of SDRAM memory types, including those supported by the C620x/C670x EMIF. This is possible because of 1) larger CE spaces and 2) programmable SDRAM page characteristics. Table 2 lists the common configurations of SDRAM that are fully supported by the C621x/C671x EMIF. Table 2 is not an exhaustive listing of supported SDRAM configurations. C621x/C671x EMIF supports a glueless interface to SDRAM memory with the following configuration:

- Pre−charge bit is A10.
- The number of column address bits is 8,9, or 10.
- The number of row address bits is 11,12, or 13.
- The number of total banks is 2 or 4 (requiring 1 or 2 bits).

Table 2 summarizes the page characteristics of the fully supported SDRAM memory types and illustrates the EMIF-to-SDRAM pin mapping. The SDRAM uses addresses A[x:0]. These pins are mapped to EA[x+2:2] on the EMIF because the C621x/C671x EMIF assumes that SDRAM memory spaces are 32 bits wide. The four BE signals serve as the two LSBs of the external address.

A key element of the supported SDRAM memory types is that A10 is always the precharge pin. Because hidden refresh is not supported on the C621x/C671x EMIF, EA12 maps directly to A10 on the SDRAM. The C621x/C671x EMIF does not use the SDA10 signal, as it does on the C620x/C670x EMIF. Note that the C621x/C671x EMIF also supports SDRAM memory space widths of 8- or 16-bits wide.

Table 2. C621x/C671x Compatible Memory Type Characteristics

SDRAM Size	Banks	Width	Depth	Max Devices/ CE	Addressable Space (M Bytes)		Column Address	Row Address	Bank Select	Pre-charge
16M bits	2	x4	2M	8	16M	SDRAM	A9−A0	A10−A0	BA0	A10
						EMIF	EA11−EA2	EA12−EA2	EA13	EA12
	2	x8	1M	4	8M	SDRAM	A8−A0	A10−A0	BA0	A10
						EMIF	EA10−EA2	EA12−EA2	EA13	EA12
	2	x16	512K	2	4M	SDRAM	A7−A0	A10−A0	BA0	A10
						EMIF	EA9−EA2	EA12−EA2	EA13	EA12
64M bits	4	x4	4M	8	64M	SDRAM	A9−A0	A11−A0	BA1−BA0	A10
						EMIF	EA11−EA2	EA13−EA2	EA15−EA14	EA12
	4	x8	2M	4	32M	SDRAM	A8−A0	A11−A0	BA1−BA0	A10
						EMIF	EA10−EA2	EA13−EA2	EA15−EA14	EA12
	4	x16	1M	2	16M	SDRAM	A7−A0	A11−A0	BA1−BA0	A10
						EMIF	EA9−EA2	EA13−EA2	EA15−EA14	EA12
	4	x32†	512K	1	8M	SDRAM	A7−A0	A10−A0	BA1−BA0	A10
						EMIF	EA9−EA2	EA12−EA2	EA14−EA13	EA12
128M bits	4	X8	4M	4	64M	SDRAM	A9−A0	A11−A0	BA1−BA0	A10
						EMIF	EA11−EA2	EA13−EA2	EA15−EA14	EA12
	4	X16	2M	2	32M	SDRAM	A8−A0	A11−A0	BA1−BA0	A10
						EMIF	EA10−EA2	EA13−EA2	EA15−EA14	EA12
	4	X32	1M	1	16M	SDRAM	A7−A0	A11−A0	BA1−BA0	A10
						EMIF	EA9−EA2	EA13−EA2	EA15−EA14	EA12
256M bits	4	x8	8M	4	128M	SDRAM	A9−A0	A12−A0	BA1−BA0	A10
						EMIF	EA11−EA2	EA14−EA2	EA16−EA15	EA12
	4	x16	4M	2	64M	SDRAM	A8−A0	A12−A0	BA1−BA0	A10
						EMIF	EA10−EA2	EA14−EA2	EA16−EA15	EA12
	4	x32	2M	1	32M	SDRAM	A8−A0	A11−A0	BA1−BA0	A10
						EMIF	EA10−EA2	EA13−EA2	EA15−EA14	EA12
512M bits	4	X16	8M	2	128M	SDRAM	A9−A0	A12−A0	BA1−BA0	A10
						EMIF	EA11−EA2	EA14−EA2	EA16−EA15	EA12

† The x32 width does not apply to C6712/12C/12D and the C6713/13B PYP package.

1.3 C64x Compatible Memory Types

The TMS320C64x™ EMIFA and EMIFB support a glueless interface to almost any configuration of SDRAM memory types, including those supported by the C620x/C670x and C621x/C671x EMIF. Like the C621x/C671x, this is possible because of 1) larger CE spaces and 2) programmable SDRAM page characteristics. Table 3 lists the common configurations of SDRAM that are fully supported by the C64x EMIF. Table 3 is not an exhaustive listing of supported SDRAM configurations. C64x EMIF supports a glueless interface to SDRAM memory with the following configuration:

- Pre−charge bit is A10.
- The number of column address bits is 8,9, or 10.
- The number of row address bits is 11,12, or 13.
- The number of total banks is 2 or 4 (requiring 1 or 2 bits).

Table 3. C64x Compatible Memory Type Characteristics

SDRAM Size	Banks	Width	Depth	Max Devices/ CE	Addressable Space (M Bytes)		Column Address	Row Address	Bank Select	Pre-charge
16M bits	2	x4	2M			SDRAM	A9−A0	A10−A0	BA0	A10
				16	32M	EMIFA	EA12−EA3	EA13−EA3	EA14	EA13
				4	8M	EMIFB	EA10−EA1	EA11−EA1	EA12	EA11
	2	x8	1M			SDRAM	A8−A0	A10−A0	BA0	A10
				8	16M	EMIFA	EA11−EA3	EA13−EA3	EA14	EA13
				2	4M	EMIFB	EA9−EA1	EA11−EA1	EA12	EA11
	2	x16	512K			SDRAM	A7−A0	A10−A0	BA0	A10
				4	8M	EMIFA	EA10−EA3	EA13−EA3	EA14	EA13
				1	2M	EMIFB	EA8−EA1	EA11−EA1	EA12	EA11
64M bits	4	x4	4M			SDRAM	A9−A0	A11−A0	A13−A12	A10
				16	128M	EMIFA	EA12−EA3	EA14−EA3	EA16−EA15	EA13
				4	32M	EMIBA	EA10−EA1	EA12−EA1	EA14−EA13	EA11
	4	x8	2M			SDRAM	A8−A0	A11−A0	BA1−BA0	A10
				8	64M	EMIFA	EA11−EA3	EA14−EA3	EA16−EA15	EA13
				2	16M	EMIFB	EA9−EA1	EA12−EA1	EA14−EA13	EA11
	4	x16	1M			SDRAM	A7−A0	A11−A0	BA1−BA0	A10
				4	32M	EMIFA	EA10−EA3	EA14−EA3	EA16−EA15	EA13
				1	8M	EMIFB	EA8−EA1	EA12−EA1	EA14−EA13	EA11
	4	x32	512K			SDRAM	A7−A0	A10−A0	BA1−BA0	A10
				2	16M	EMIFA	EA10−EA3	EA13−EA3	EA15−EA14	EA13

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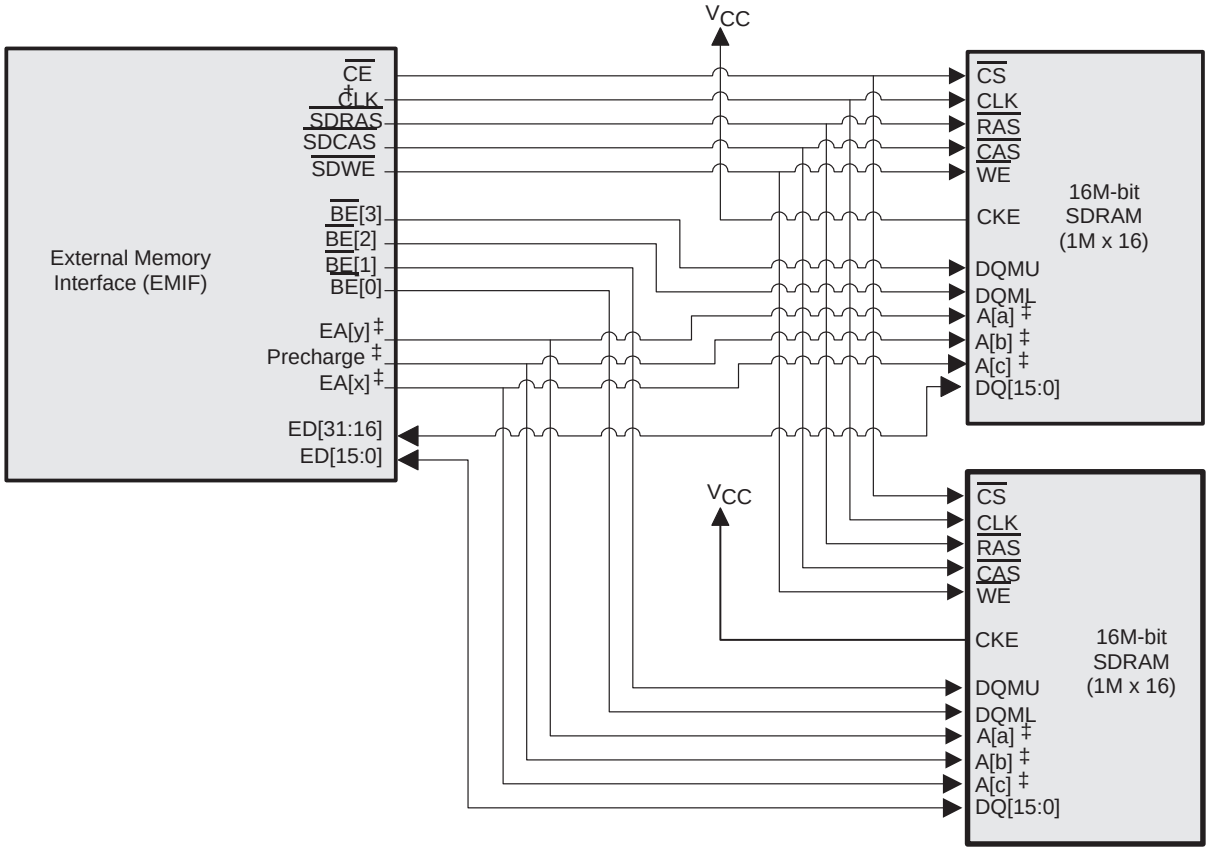
Table 3. C64x Compatible Memory Type Characteristics (Continued)

SDRAM Size	Banks	Width	Depth	Max Devices/ CE	Addressable Space (M Bytes)		Column Address	Row Address	Bank Select	Pre-charge
						EMIFB	–	–	–	–
128M bits	4	X8	4M			SDRAM	A9–A0	A11–A0	BA1–BA0	A10
				8	128M	EMIFA	EA12–EA3	EA14–EA3	EA16–EA15	EA13
				2	32M	EMIFB	EA10–EA1	EA12–EA1	EA14–EA13	EA11
	4	X16	2M			SDRAM	A8–A0	A11–A0	BA1–BA0	A10
				4	64M	EMIFA	EA11–EA3	EA14–EA3	EA16–EA15	EA13
				1	16M	EMIFB	EA9–EA1	EA12–EA1	EA14–EA13	EA11
	4	X32	1M			SDRAM	A7–A0	A11–A0	BA1–BA0	A10
				2	32M	EMIFA	EA10–EA3	EA14–EA3	EA16–EA15	EA13
						EMIFB	–	–	–	–
256M-bit	4	x8	8M			SDRAM	A9–A0	A12–A0	BA1–BA0	A10
				8	256M	EMIFA	EA12–EA3	EA15–EA3	EA17–EA16	EA13
				2	64M	EMIFB	EA10–EA1	EA13–EA1	EA15–EA14	EA11
	4	x16	4M			SDRAM	A8–A0	A12–A0	BA1–BA0	A10
				4	128M	EMIFA	EA11–EA3	EA15–EA3	EA17–EA16	EA13
				1	32M	EMIFB	EA9–EA1	EA13–EA1	EA15–EA14	EA11
	4	x32	2M			SDRAM	A8–A0	A11–A0	BA1–BA0	A10
				2	64M	EMIFA	EA11–EA3	EA14–EA3	EA16–EA15	EA13
						EMIFB	–	–	–	–
512M-bit	4	X16	8M			SDRAM	A9–A0	A12–A0	BA1–BA0	A10
				4	256M	EMIFA	EA12–EA3	EA15–EA3	EA17–EA16	EA13
				1	64M	EMIFB	EA10–EA1	EA13–EA1	EA15–EA14	EA11

1.4 C6000 EMIF-to-SDRAM Physical Interface

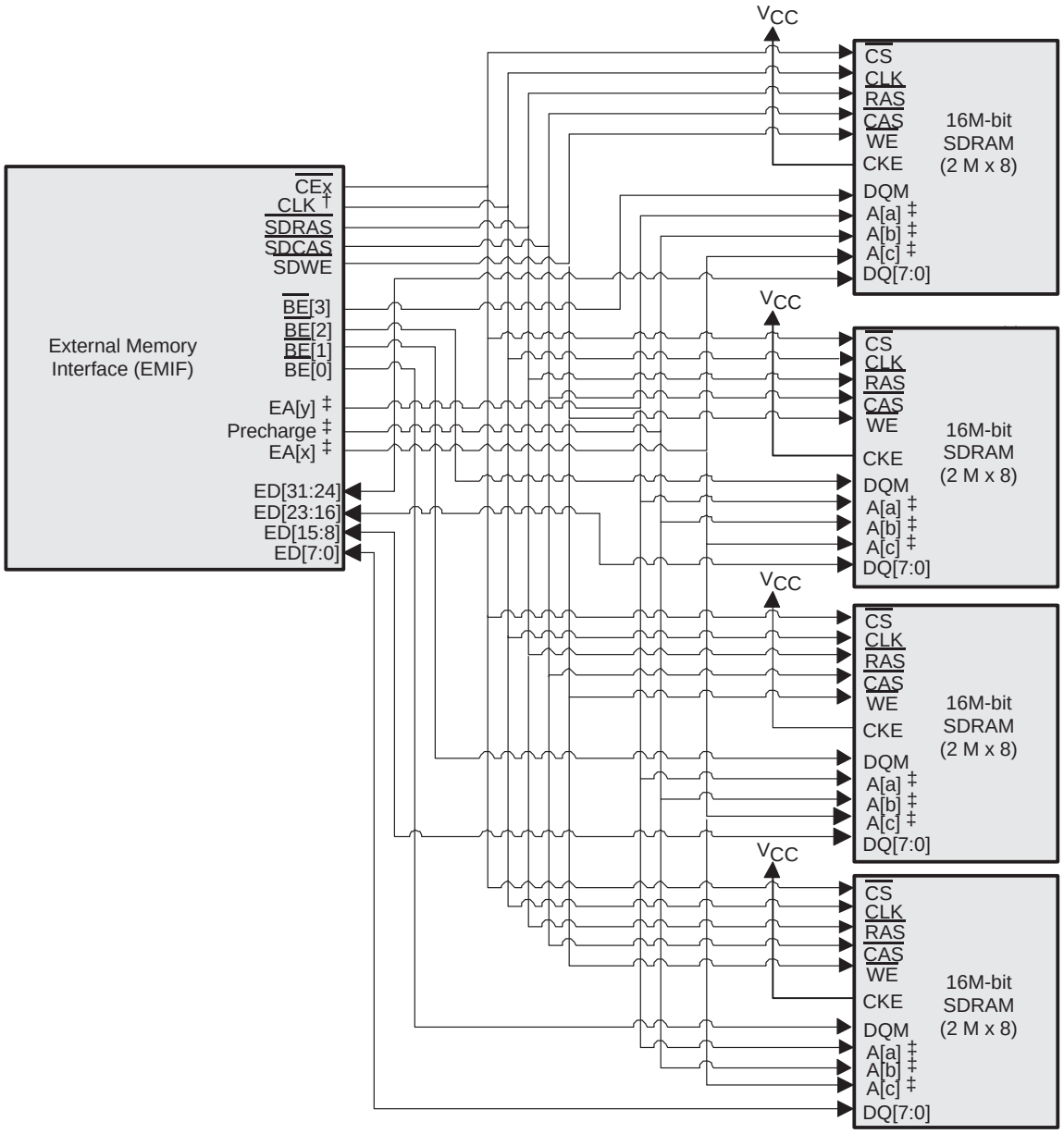
Figure 1 through Figure 7 illustrate the EMIF SDRAM interface for all C6000 devices. Table 8 describes the pin connection and related signals specific to SDRAM operations.

A 16-bit bus interface for the C621x/C671x (big-endian) is shown in Figure 5. Although not every possible interface is shown for the C621x/C671x, these figures can be used as a reference. For interfaces to denser SDRAMs (such as 128M-bit and 256M-bit), the only difference is that additional address bits are used. The control and data interfaces are identical to the figures shown here. Figure 6 shows a C64x EMIFA interfaced to two 64M-bit SDRAMs, and Figure 7 shows a C64x EMIFA interfaced to four 512M-bit-wide chip.



† CLK = SDCLK for C6701/C6701
CLK = CLKOUT2 for C6202
CLK = ECLKOUT for C621x/C671x
CLK = ECLKOUT1 for C64x
‡ See Table 1, Table 2, and Table 3 for appropriate addresses and precharge pin.

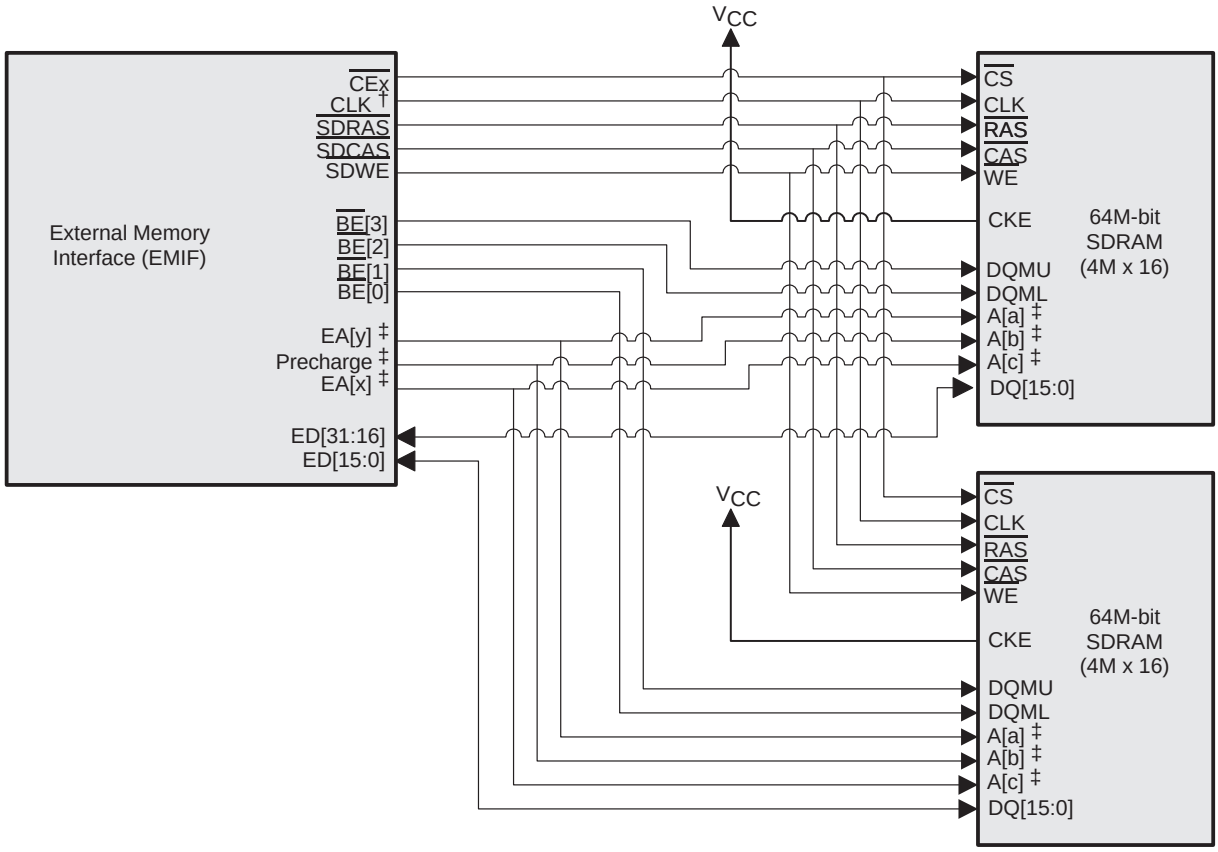
Figure 1. C6000 EMIF-to-16M-Bit SDRAM Interface Using Two 16-Bit-Wide Chips



† CLK = SDCLK for C6701/C6701
CLK = CLKOUT2 for C6202
CLK = ECLKOUT for C621x/C671x
CLK = ECLKOUT1 for C64x

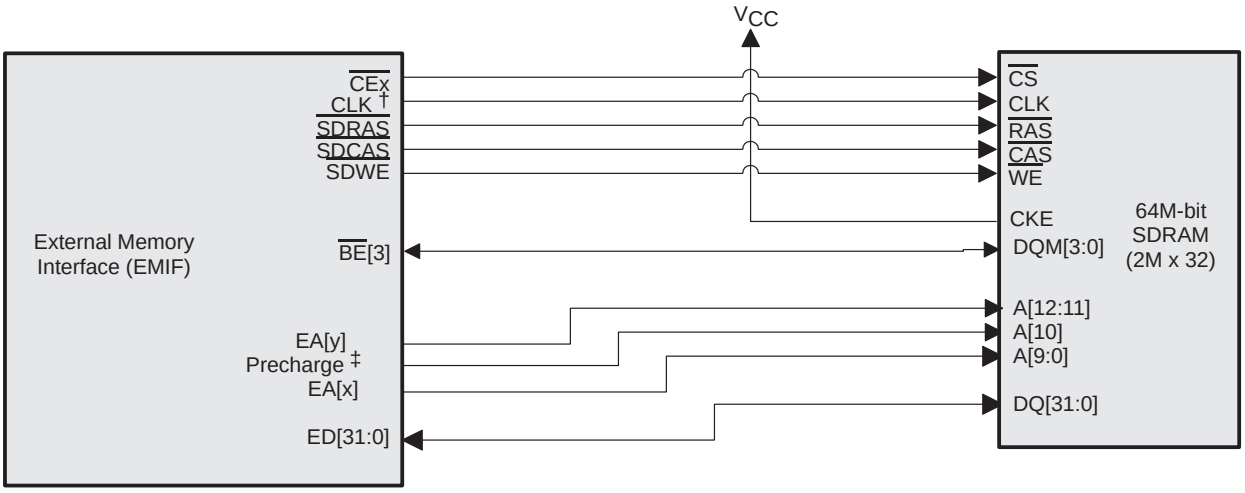
‡ See Table 1, Table 2, and Table 3 for appropriate addresses and precharge pin.

Figure 2. C6000 EMIF-to-16M-Bit SDRAM Interface Using Four 8-Bit-Wide Chips



† CLK = SDCLK for C6701/C6701
CLK = CLKOUT2 for C6202
CLK = ECLKOUT for C621x/C671x
CLK = ECLKOUT1 for C64x
‡ See Table 1, Table 2, and Table 3 for appropriate addresses and precharge pin.

Figure 3. C6000 EMIF1-to-64M-Bit SDRAM Interface Using Two 16-Bit-Wide Chips



† CLK = SDCLK for C6701/C6701
CLK = CLKOUT2 for C6202
CLK = ECLKOUT for C621x/C671x
CLK = ECLKOUT1 for C64x
‡ See Table 1, Table 2, and Table 3 for appropriate addresses and pre−charge pin.

(C6712, C6712C, and C6712D EMIFB on C64x does not support 32-bit interface)

Figure 4. C6000 EMIF-to-64M-Bit SDRAM Interface Using One 32-Bit-Wide Chip

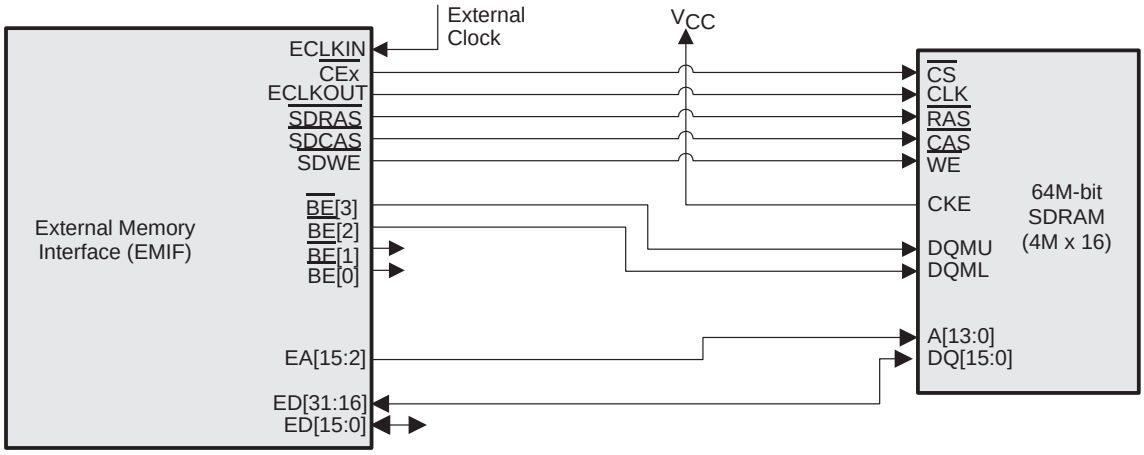


Figure 5. C621x/C671x EMIF-to-64M-Bit SDRAM Interface Using One 16-Bit-Wide Chip (Big Endian)

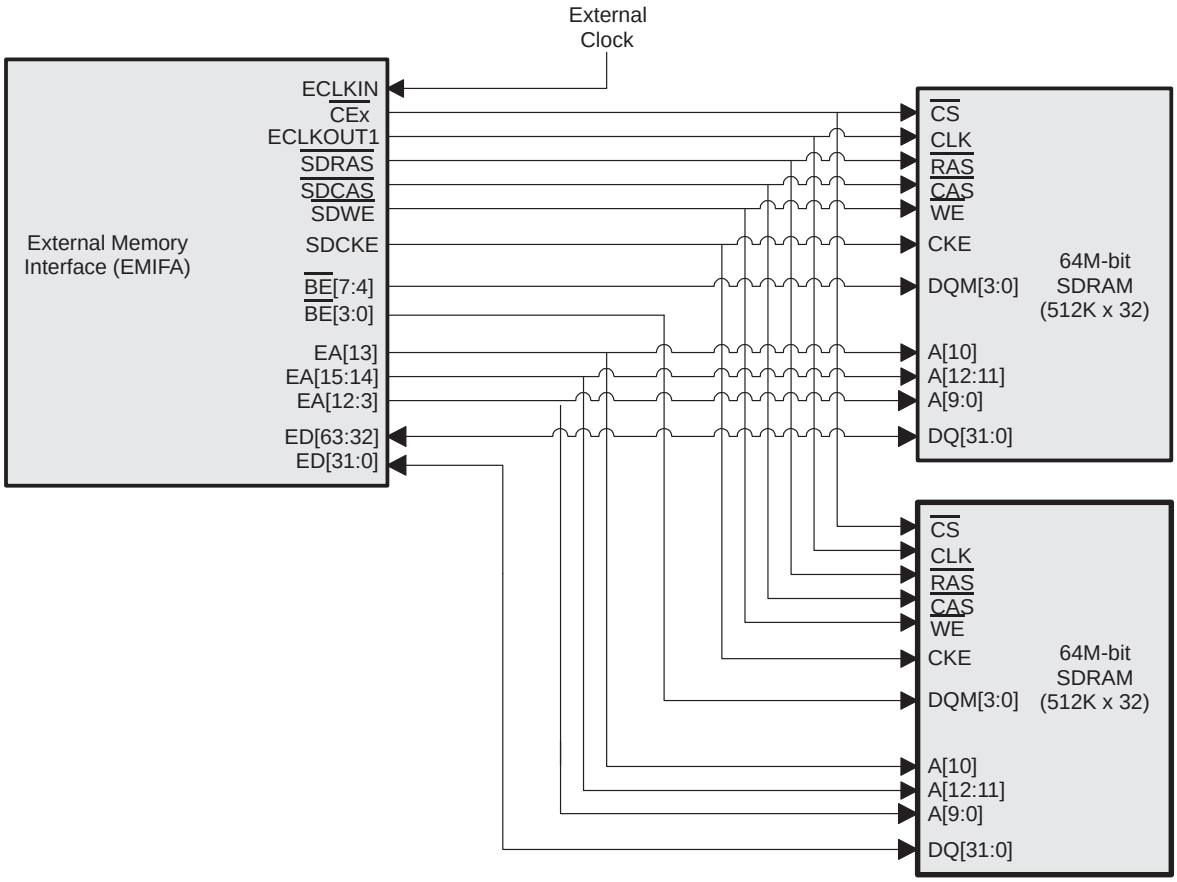


Figure 6. C64x EMIFA-to64M-Bit SDRAM Interface Using Two 32-Bit-Wide Chips

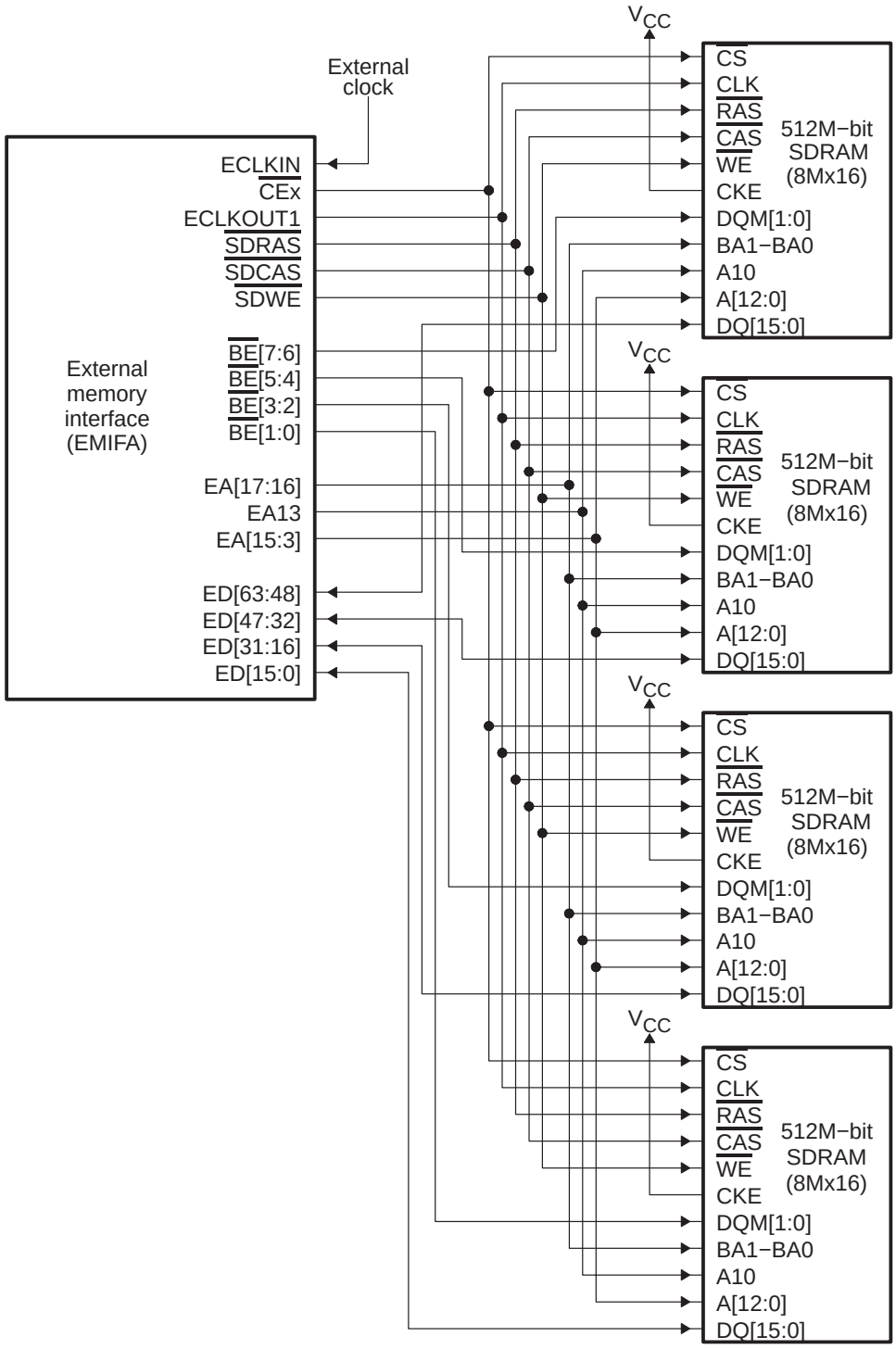


Figure 7. C64x EMIFA−to−512M Bit SDRAM Interface Using Four 16−bit Wide Chips

2 Overview of the C6000 EMIF

2.1 C620x/C670x SDRAM Interface Summary

- Supports 32-bit-wide SDRAM interface
- 16M-byte CE spaces
- Operates at 1/2x the CPU clock speed. Clock is generated internal to the DSP.
- Includes three programmable SDRAM controller values (TRC, TRCD, and TRP). Other values are static.
- Supports a single open page of SDRAM in each CE space
- Column size is programmable to either 8- or 9-column address bits. Four configurations of SDRAM are supported.
- Does not support SDRAM burst mode. Performs bursts by issuing back-to-back commands.
- C6201/C6701
  - SDCLK is used as the SDRAM clock.
  - Includes dedicated SDRAM control signals. Any combination of synchronous memory types is allowed.
- C6202/C6203/C6204/C6205
  - CLKOUT2 is used as the SDRAM clock.
  - SDRAM control signals are MUXed with SBSRAM control signals. Only one type of synchronous memory is allowed in the system.

2.2 C621x/C671x SDRAM Interface Summary

- Supports 32-bit, 16-bit, and 8-bit-wide SDRAM interfaces†
- 128M-byte addressable reach per CE spaces
- Clock speed is independent of internal CPU speed and can run at a maximum of 100 MHz. For C6211/C6711/C6711B, ECLKIN must be provided by system. For all other C621x/C671x devices the EMIF clock rate can be generated internal to the DSP or provided by the system (via ECLKIN). If ECLKIN is used, the ECLKIN input can be completely independent of the CPU clock.
- Very flexible programming of SDRAM timing parameters
- Supports four open pages of SDRAM. These can be in different CE spaces, all in a single CE space, or any combination of the two.
- Can program the SDRAM configuration (column size, row size, and bank size). Almost any SDRAM configuration can be used.
- Supports SDRAM burst mode with a 4-word burst
- ECLKOUT must be used as the synchronous memory clock and is a delayed version of ECLKIN, which must be provided by the system.
- SDRAM control signals are MUXed with SBSRAM and Async control signals. Any combination of synchronous memory types is allowed.

† The EMIF bus width varies on C621x/C671x devices. Please see the device specific datasheet for supported bus widths.

2.3 C64x SDRAM Interface Summary

- Supports 64-bit, 32-bit, 16-bit, and 8-bit-wide SDRAM interfaces[1]
- 256M-byte CE spaces
- Flexible clock selection allows the EMIF clock rate to be generated internal to the DSP (1/4th or 1/6th of the CPU clock rate) or provided by the system (via ECLKIN). If ECLKIN is used, the ECLKIN input can be completely independent of the CPU clock. In both cases (internal or external clock source), the EMIF clock rate must not exceed 133 MHz.
- Very flexible programming of SDRAM timing parameters
- Supports four open pages of SDRAM. These can be in different CE spaces, all in a single CE space, or any combination of the two.
- Can program the SDRAM configuration (column size, row size, and bank size). Almost any SDRAM configuration can be used.
- Supports SDRAM burst mode with a 4-word burst
- ECLKOUT1 must be used as the synchronous memory clock and is a mirror image of ECLKIN.
- SDRAM control signals are MUXed with Programmable Synchronous and Async control signals. Any combination of synchronous memory types is allowed.
- Supports self-refresh mode through the SLFRFR bit of the SDRAM control register[2]

2.4 C6000 EMIF Signal Descriptions

Figure 8, Figure 9, Figure 10, and Figure 11 show the block diagrams of the C6201/C6701, C6202/C6203/C6204/C6205, C621x/C671x, and C64x, respectively. Note that the clocks and control signals are slightly different for each of the four different style EMIFs. The signals listed in Table 4 describe the SDRAM interface and the shared interface signals.

[1] 64-bit and 32-bit interface supported by EMIFA only

[2] Supported on EMIFA only

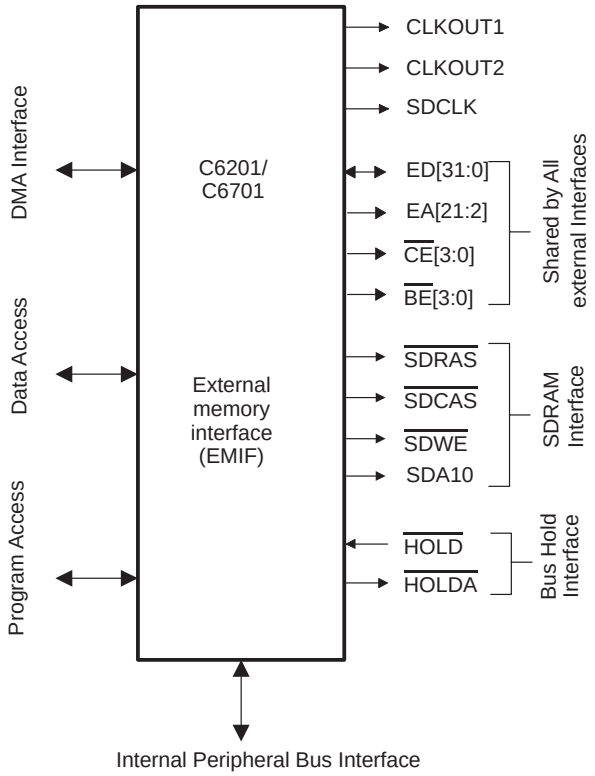


Figure 8. C6201/C6701 EMIF Block Diagram

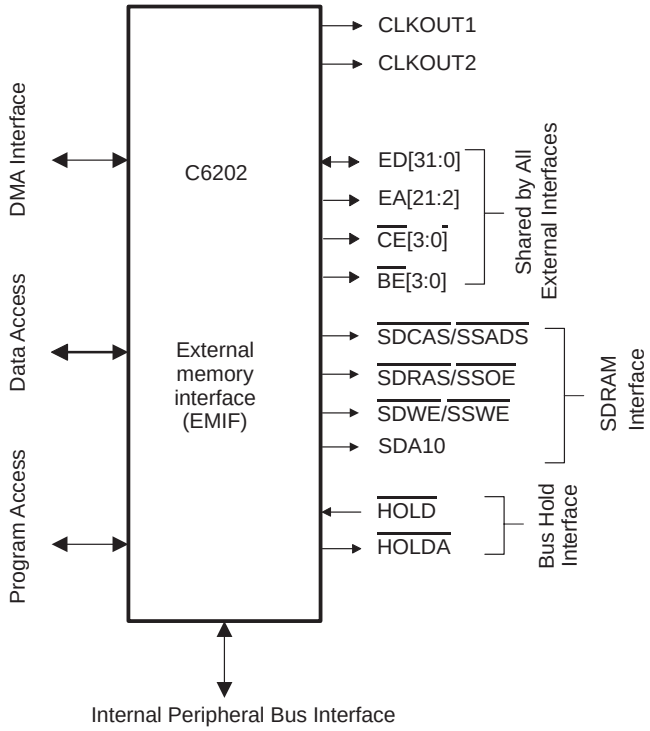


Figure 9. C6202/C6203/C6204/C6205 EMIF Block Diagram

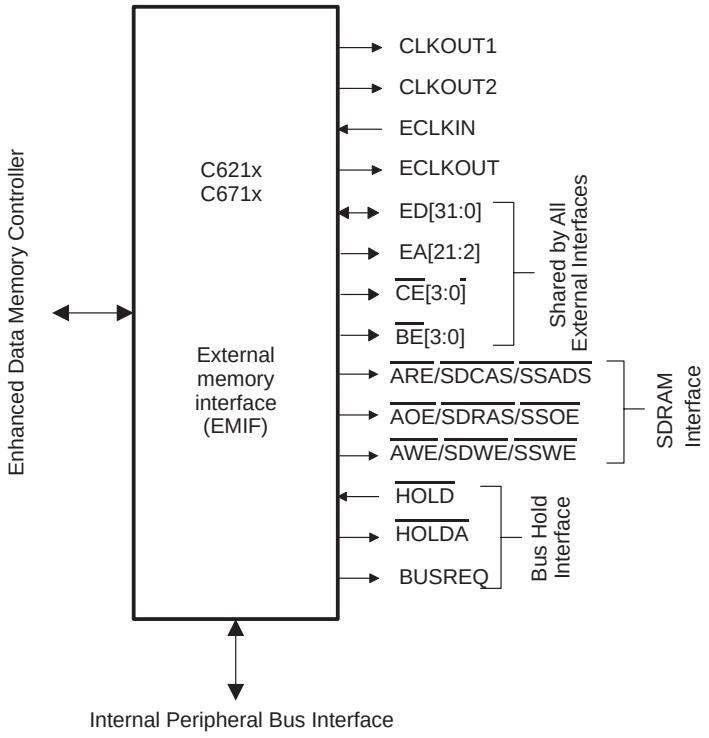
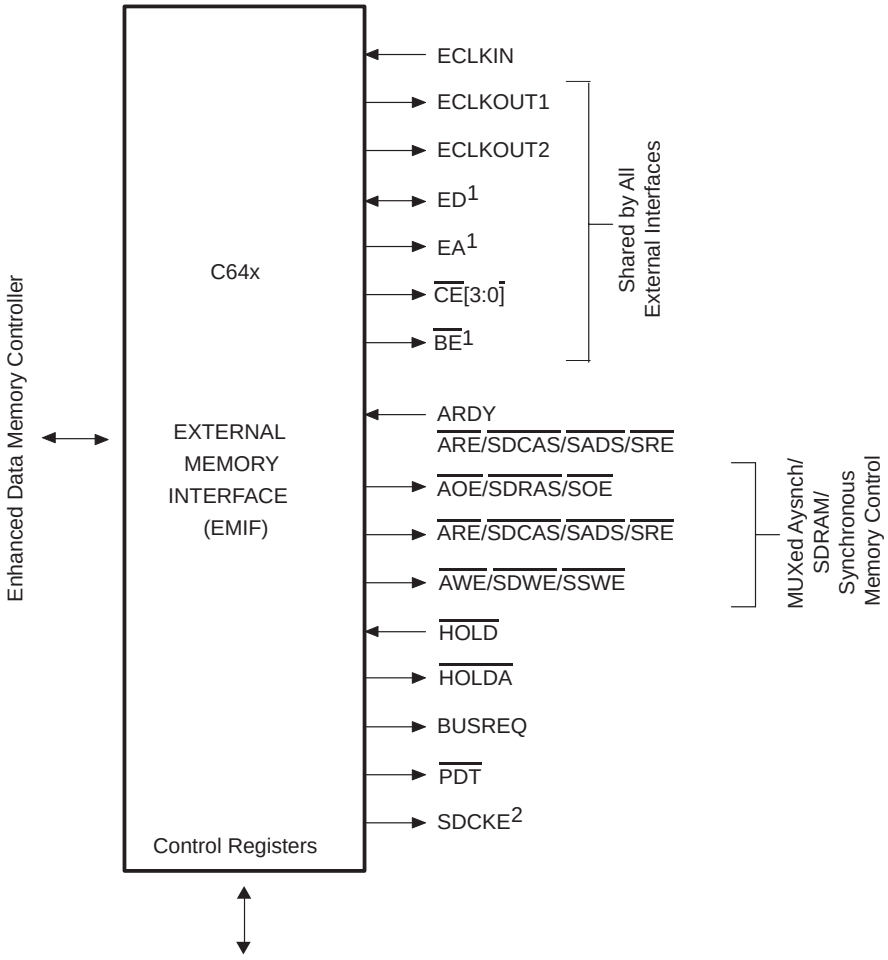


Figure 10. C621x/C671x EMIF Block Diagram



NOTES: 1. See Table 4 for ED, EA, and $\overline{BE}$ pins for EMIFA and EMIFB.
2. SDCKE applies to EMIFA only.

Figure 11. C64x EMIF Block Diagram

Table 4. TMS320C6000 SDRAM Signal Descriptions

	C62x/C67x EMIF				C64x EMIF		
					EMIFA		EMIFB
SDRAM Signal	**C6201/C6701**	**Other C620x/C670x†**	**C6712/12C/12D C6713/13B‡**	**Other§ C621x/C671x**	**C6416/15/14/12, DM642,C641xT**	**C6411, DM640/641**	**C641xT/ C6416/15/14**
DQ [x:0]	ED[31:0]	ED[31:0]	ED [15:0]	ED [31:0]	ED [63:0]	ED [31:0]	BED[15:0]
A [13:0]	EA[15:2]	EA[15:2]	EA [15:2]	EA [15:2]	EA [16:3]	EA [16:3]	BEA[14:1]
A10	SDA10	SDA10	EA12	EA12	AEA13	AEA13	BEA11
$\overline{CS}$	$\overline{CE0}$ $\overline{CE2}$, or $\overline{CE3}$	$\overline{CE0}$ $\overline{CE2}$, or $\overline{CE3}$	$\overline{CE0}$/$\overline{CEI}$/$\overline{CE2}$/ $\overline{CE3}$	$\overline{CE0}$/$\overline{CEI}$/$\overline{CE2}$/ $\overline{CE3}$	$\overline{ACEO}$,$\overline{ACE1}$, $\overline{ACE2}$,$\overline{ACE3}$	$\overline{ACEO}$,$\overline{ACE1}$, $\overline{ACE2}$,$\overline{ACE3}$	$\overline{BCE0}$, $\overline{BCE1}$, $\overline{BCE2}$, or $\overline{BCE3}$
DQM [3:0]	$\overline{BE}$[3:0]	$\overline{BE}$[3:0]	BE [1:0]	BE [3:0]	$\overline{ABE}$ [7.0]	$\overline{ABE}$ [3:0]	$\overline{BBE}$[1:0]
$\overline{RAS}$	$\overline{SDRAS}$	$\overline{SDRAS}$/ $\overline{SSOE}$	$\overline{AOE}$/$\overline{SDRAS}$/ $\overline{SSOE}$	$\overline{AOE}$/$\overline{SDRAS}$/ $\overline{SSOE}$	$\overline{AOE}$/$\overline{ASDRAS}$/ $\overline{ASOE}$	$\overline{AOE}$/$\overline{AS-DRAS}$/$\overline{ASOE}$	$\overline{BAOE}$/ $\overline{BSDRAS}$/ $\overline{BSOE}$
$\overline{CAS}$	$\overline{SDCAS}$	$\overline{SDCAS}$/ $\overline{SSADS}$	$\overline{ARE}$/$\overline{SDCAS}$/$\overline{S-SADS}$	$\overline{ARE}$/$\overline{SDCAS}$/ $\overline{SSADS}$	$\overline{AARE}$/$\overline{ASD-CAS}$/$\overline{ASADS}$/ $\overline{ASRE}$	$\overline{AARE}$/$\overline{ASD-CAS}$/$\overline{ASADS}$/ $\overline{ASRE}$	$\overline{BARE}$/ $\overline{BSDCAS}$/ $\overline{BSADS}$/ $\overline{BSBE}$
$\overline{WE}$	$\overline{SDWE}$	$\overline{SDWE}$/ $\overline{SSWE}$	$\overline{AWE}$/$\overline{SDWE}$/ $\overline{SSWE}$	$\overline{AWE}$/$\overline{SDWE}$/ $\overline{SSWE}$	$\overline{AAWE}$/$\overline{ASDWE}$/ $\overline{ASWE}$	$\overline{BAWE}$/ $\overline{BSDWE}$/ $\overline{BSWE}$	$\overline{BAWE}$/ $\overline{BSDWE}$/ $\overline{BSWE}$
CLK	SDCLK	CLKOUT2	ECLKOUT	ECLKOUT	AECLKOUT1	AECLKOUT1	BECLKOUT1
CKE	3.3V	3.3V	3.3V	3.3V	ASDCKE	ASDCKE	3.3V

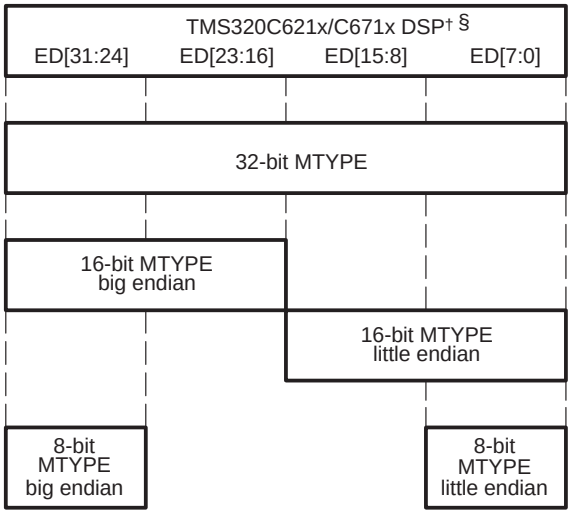
† This column applies to all C620x/C670x devices, except C6201/C6701 DSP.
‡ For C6713/13B devices, this column applies only to the PYP package type.
§ This column applies to all C621x/C67 devices, except C6712/C6712C/C6712D and C6713/13B PYP package type.

2.4.1 C621x/C671x Byte-Lane Alignment

The C621x/C671x EMIF offers the capability to interface to 32-bit, 16-bit, and 8-bit SDRAM. Depending on the endianness of the system, a different byte lane is used for the SDRAM interface. The alignment required is shown in Figure 12.

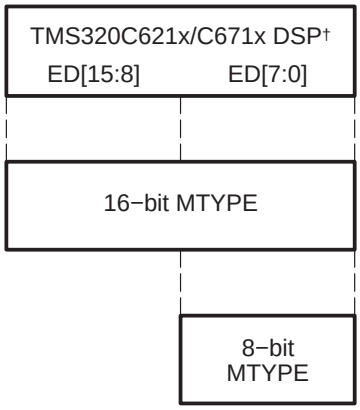
Note that BE3 always corresponds to ED[31:24], BE2 always corresponds to ED[23:16], BE1 always corresponds to ED[15:8], and BE0 always corresponds to ED[7:0], regardless of endianness.

(a) 32-bit bus‡



§ The C6713B and C6711D devices allow the flexibility of changing the EMIF data
placement on the EMIF bus. See the device specific data sheet for more details.

(b) 16-bit bus‡



† C6712/C6712C DSP do not support big-endian byte alignment. C6712D supports both big−endian and little endian with the above data alignment. For more details, see the device specific datasheet.

‡ Denotes total EMIF bus width, not MTYPE configuration.

Figure 12. C621x/C671x Byte-Lane Alignment vs. Endianness

2.4.2 C64x Byte-Lane Alignment

The C64x EMIFA offers the capability to interface to 64-bit, 32-bit, 16-bit, and 8-bit SDRAM. EMFIB supports interfaces to 16-bit and 8-bit SDRAM. Figure 13 shows the byte lanes used on the C64x for EMIFA and EMIFB.

Unlike the previous C6000 devices, the external memory on the C64x is always right aligned to the ED[7:0] side of the bus. The endianness mode determines whether byte lane 0 (ED[7:0]) is accessed as byte address 0 (little endian) or as byte address N (big endian), where 2^N is the memory width in bytes.

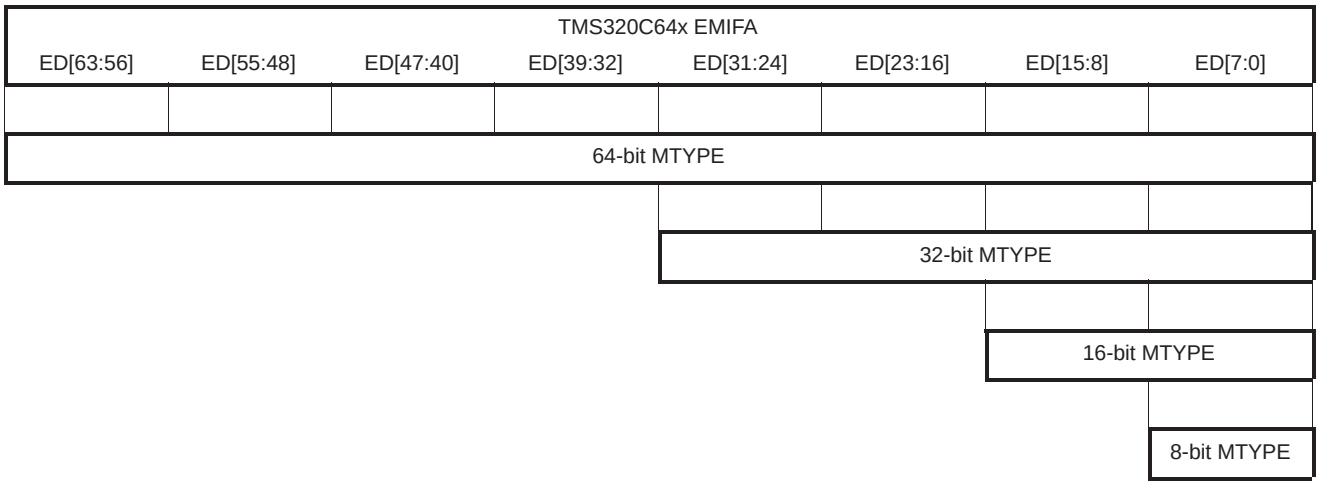
2.4.3 C621x/C671x/C64x Clocking

The EMIF of the C6211/C6711 requires an external clock provided via the ECLKIN input. For simplicity on the C6211/C6711, CLKOUT2 can be routed into the ECLKIN pin to avoid the extra hardware required to create a clock externally. This method has the restriction of only allowing a memory interface at 1/2x the CPU clock speed (or 75 MHz for a 150-MHz device).

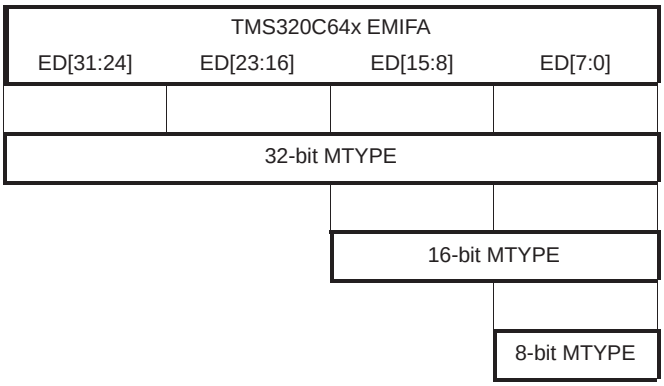
For C64x and C621x/C671x (excluding C6211/C6711) devices, one can use the internally provided CPU clock to simplify clocking. On C64x devices, when the Internal CPU clock is selected as the EMIF input clock source, the rate can be configured as either CPU14 or CPU16. On C621x/C671x devices, when the internal CPU clock is selected as the EMIF input clock source, the clock rate can be configured as fast as CPUx1 or as slow as CPU/32. For more details, see the device datasheet.

The data sheets for each device specify that the rise/fall time of the externally provided clock must be within a very specific range. This can prove difficult with most off-the-shelf oscillators. Our recommended approach is to use the ICS501 PLL multiplier chip, which can produce a wide range of frequency outputs with standard crystals.

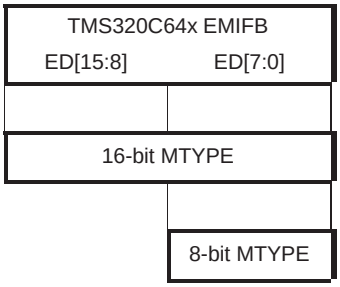
(c) EMIFA (64-bit bus):†



(d) EMIFA (32-bit bus):†



(e) EMIFB (16-bit bus):†



† Denote total EMIF bus width, not MTYPE configuration.

Figure 13. Byte Alignment by Endianness

2.4.4 C6000 Clock-to-Output Relationship

To optimize the synchronous memory interfaces of the various C6000 devices, the output signals are triggered off of different internal clocks of the C6000 DSP. Figure 14 and Figure 15 show the clock relationship used for the various C6000 DSPs. Because the C621x/C671x/C64x SDRAM interface is timed in reference to an externally provided clock, the C621x,C671x, and C64x data sheets provide t_{dmax} and t_{dmin}, but not t_{osu} and t_{oh}, parameters. The fact that the t_{osu} and t_{oh} parameters use a factor of *P* in the equations allows the user to be unconcerned about the output edge being used internally to the C6000. In this way, the t_{osu} parameter can be compared directly against the t_{isu} parameter of the memory at a given operating speed.

The t_{dmax} and t_{dmin} parameters reference the actual clock edge of the C6000 from which data is driven out. The t_{osu} and t_{oh} terms are the notation used in the C6000 data sheets, except those for the C621x,C671x, and C64x. The t_{osu} term shows the setup time to the rising edge of the clock. The t_{oh} term shows the hold time from the rising edge of the memory clock. *P* refers to the CPU clock period.

Notice that the data sheet notation directly implies the clocking relationship of the device. For example, the data sheet for the C6201B SDRAM interface states that t_{osu} = 1.5P – 3.5 ns. Referring to the diagram in Figure 14, it can be seen that t_{dmax} is relative to a point ½ P from the rising edge of SDCLK, providing a setup time of 1.5P – t_{dmax}. All other C6000 data sheets can be analyzed in the same way.

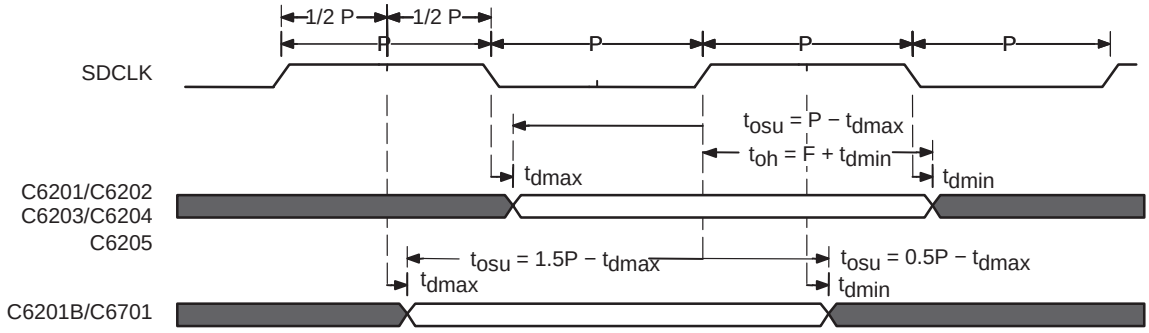


Figure 14. C6201/C6202/C6203/C6204/C6205 vs. C6201B/C6701 Output Timing

Figure 15 shows the clock relationship used for the C621x/C671x/C64x SDRAM interface. Because this interface is timed in reference to an externally provided clock, the C621x/C671x, and C64x data sheets provide t_{dmax} and t_{dmin} but not t_{osu} and t_{oh} parameters.

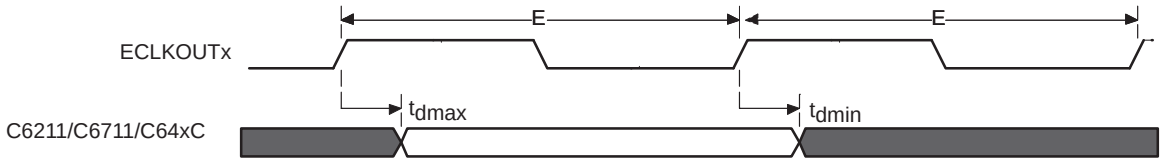


Figure 15. C621x/C671x/C64x Output Timing

2.5 C6000 EMIF Registers

Control of the EMIF and the memory interfaces it supports is maintained through a set of memory-mapped registers within the EMIF. The memory-mapped registers are shown in Table 5.

Table 5. C6000 EMIF Memory Mapped Registers

Byte Address			
EMIF and EMIFA	EMIFB †	Abbreviation	Description
0x01800000	0x01A80000	GBLCTL	EMIFx Global Control
0x01800004	0x01A80004	CE1CTL	EMIFx CE1 Space Control
0x01800008	0x01A80008	CE0CTL	EMIFx CE0 Space Control
0x0180000C	0x01A8000C		Reserved
0x01800010	0x01A80010	CE2CTL	EMIFx CE2 Space Control
0x01800014	0x01A80014	CE3CTL	EMIFx CE3 Space Control
0x01800018	0x01A80018	SDCTL	EMIFx SDRAM Control
0x0180001C	0x01A8001C	SDTIM	EMIFx SDRAM Refresh Period
0x01800020‡	0x01A80020‡	SDEXT	EMIFx SDRAM extension‡
0x01800044	0x01A80044	CE1SEC	EMIFx CE1 Space Secondary Control
0x01800048	0x01A80048	CE0SEC	EMIFx CE0 Space Secondary Control
0x0180004C	0x01A8004C		Reserved
0x01800050	0x01A80050	CE2SEC	EMIFx CE2 Space Secondary Control
0x01800054	0x01A80054	CE3SEC	EMIFx CE3 Space Secondary Control

† EMIFB applies to C64x only
‡ Applies to C621x, C671x, and C64x only. Reserved on other devices.

2.5.1 EMIF Global Control Register

The EMIF global control register configures parameters common to all the CE spaces (see Figure 16 and Figure 17). Table 6 lists only those parameters relevant for use with SDRAM.[3]

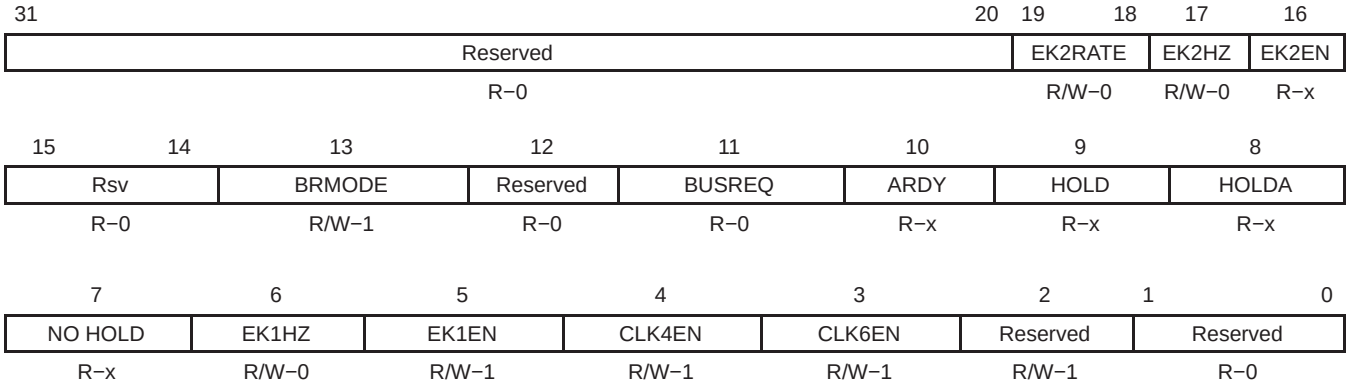
31	14	13	12	11	10	9	8
Reserved		Reserved		Reserved	ARDY	HOLD	HOLDA
R/W−0		R/W−1		R−0	R−0	R−0	R−0

7	6	5	4	3	2	1	0
NO HOLD	SDCEN	SSCEN	CLK1EN	CLK2EN§	SSCRT	RBTR8	MAP
R/W−0	R/W−1	R/W−1	R/W−1	R/W−1	R/W−0	R/W−0	R−x

Legend: R = Read, R/W= Read/Write
§ Fields do not exist in C6202/C6203/C6204/C6205.

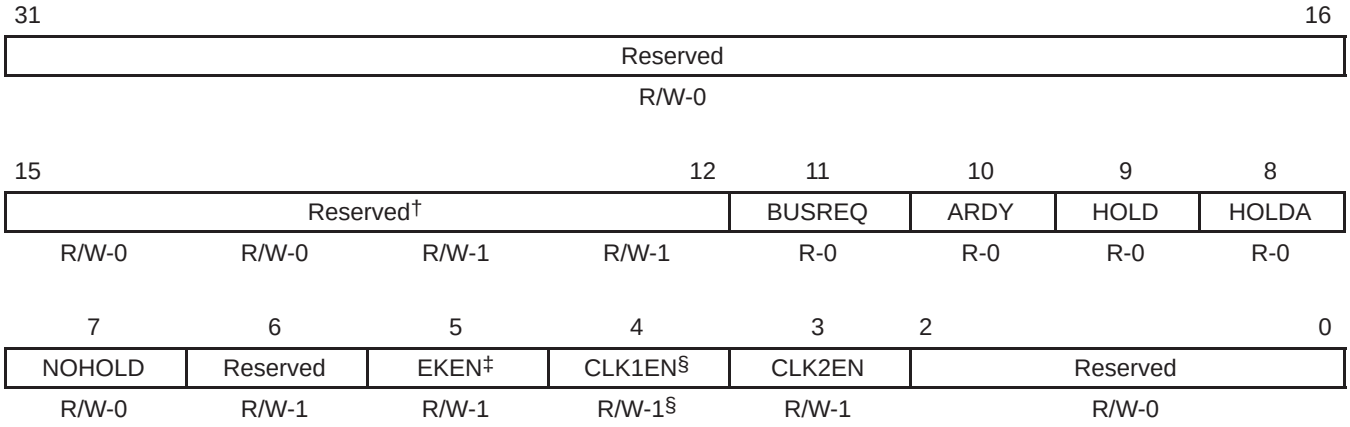
Figure 16. C620x/C670x EMIF Global Control Register Diagram

[3] For a description of all of the parameters of the EMIF global control register, see the *TMS320C6000 Peripherals Reference Guide*.



Legend: R = Read, R/W= Read/Write

Figure 17. C64x EMIF Global Control Register Diagram



† The reserved bit fields should always be written with their default values when modifying the GBLCTL. Writing a value other than the default value to these fields may cause improper operation.
‡ Available on C6713, C6712C, and C6711C devices only; on other C621x/C671x devices, this field is reserved with R/W-1.
§ This bit is reserved on C6713, C6712C, and C6711C devices with R/W-0. Writing a value other than 0 to this bit may cause improper operation.
Legend: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 18. C621x/C671x EMIF Global Control Register (GBLCTL)

Table 6. EMIF Global Control Register Bit Field Description

Field	Description
SDCEN	SDRAM clock enable (for C620x/C670x) C6201/C6701: SDCEN = 0, SDCLK held high SDCEN = 1, SDCLK enabled to clock C6202/C6203/C6204/C6205: SDCEN = 0, CLKOUT2 held high if MemType = SDRAM
EKEN ‡	ECLKOUT enable EKEN = 0, ECLKOUT held low ECKEN = 1, ECLKOUT enabled to clock
EK1EN †	ECLKOUT1 enable EK1EN = 0, ECLKOUT1 held low EK1EN = 1, ECLKOUT1 enabled to clock
EK2RATE †	ECLKOUT2 Rate. ECLKOUT2 runs at: EK2RATE = 00, 1x EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate EK2RATE = 01, 1/2x EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate EK2RATE = 10, 1/4x EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate

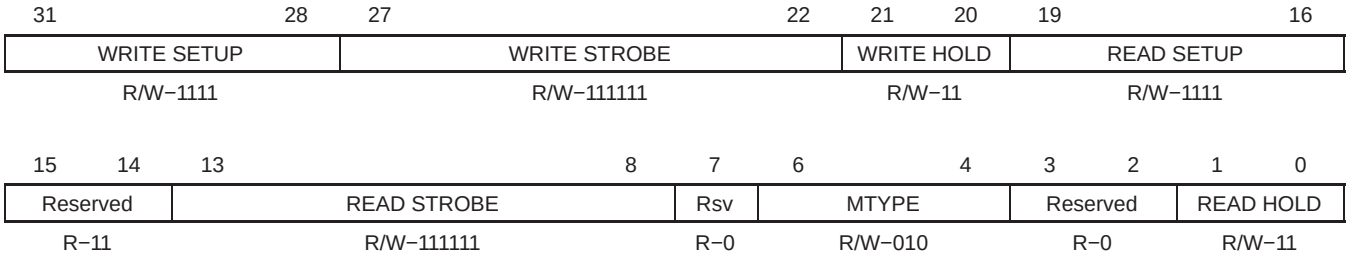
† Applies to C64x control register only
‡ Applies to C621x/C671x devices, excluding C6211/C6711.

Note that CLK2EN is not available on the C6202/C6203/C6204/C6205. CLKOUT2 is disabled by either SSCEN or SDCEN, depending on the MemType used. This is possible because only one synchronous MemType is allowed in a system.

2.5.2 CE Space Control Registers

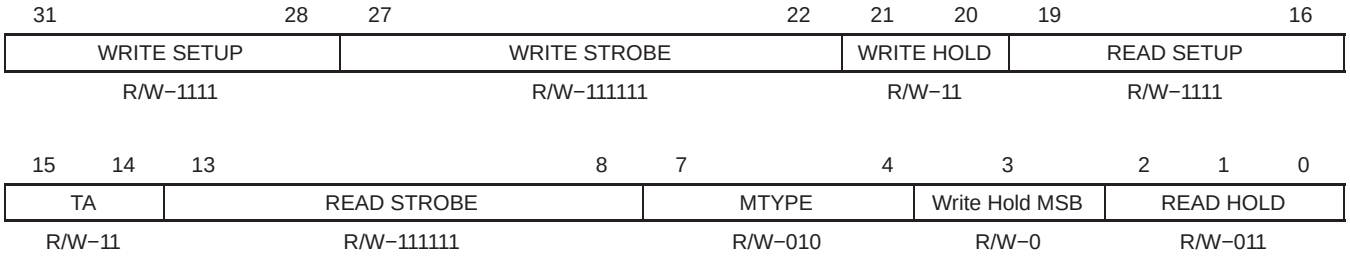
Figure 19 and Figure 20 show the four CE space control registers, which correspond to the four CE spaces supported by the EMIF. The MTYPE field identifies the memory type for the corresponding CE space. If MTYPE selects SDRAM or SBSRAM, the remaining fields in the register do not apply. If an asynchronous type is selected (ROM or asynchronous), the remaining fields specify the shaping of the address and control signals for access to that space. The only field of interest for SDRAM is the MTYPE field. Modification of a CE space control register should not be done until that CE space is inactive.

Table 7 lists the bit field descriptions for Figure 19 and Figure 20.



Legend: R = Read, R/W= Read/Write

Figure 19. C620x/C670x EMIF CE Space Control Register Diagram



Legend: R = Read, R/W= Read/Write

Figure 20. C621x/C671x/C64x EMIF CE Space Control Register Diagram

Table 7. C6000 EMIF CE Space Control Register Bit Field Description for SDRAM

Field	Description
MTYPE	Memory Type of the corresponding CE Spaces MTYPE for C620x/C670x MTYPE = 011b: 32-bit-wide SDRAM MTYPE for C621x/C671x/C64x † MTYPE = 0011b: 32-bit-wide SDRAM MTYPE = 1000b: 8-bit-wide SDRAM MTYPE = 1001b: 16-bit-wide SDRAM MTYPE = 1101b: 64-bit-wide SDRAM ‡

† 32-bit and 64-bit interfaces do not apply to C6712, C6712C, C6712D, as well as the PYP package type of C6713 and C6713B, and C64x EMIFB.

‡ 64-bit interface applies to C64x EMIFA only.

2.5.3 SDRAM Control Register (SDCTL)

The SDRAM control register controls SDRAM parameters for all CE spaces that specify an SDRAM memory type in the MTYPE field of its associated CE space control register (see Figure 21). Because the SDRAM control register controls all SDRAM spaces, each space should contain SDRAM with the same timing and page characteristics to ensure compatibility; however, it is not *absolutely* necessary to have the same page characteristics. See the following section, entitled *Interchangeable SDRAM Devices and Upgrading (C64x only)*, for more information.

The timing fields in the EMIF SDRAM control register are in terms of the EMIF clock period. For the C620x/C670x, t_{cyc} is twice the CPU period because SDCLK and CLKOUT2 are 1/2x the CPU frequency. For the C621x/C671x, t_{cyc} equals the ECLKOUT period. For the C64x, t_{cyc} equals the ECLKOUT1 period.

Table 8 lists the bit field descriptions for Figure 21.

† Refers to C621x/C671x and C64x only.
‡ Refers to C620x/C670x only.
§ Refers to C64x only.

Figure 21. EMIF SDRAM Control Register

Table 8. EMIF SDRAM Control Register Bit Field Description

Field	Description
TRC	Specifies t_{RC} value of the SDRAM in EMIF clock cycles. TRC = $(t_{RC}/t_{cyc}) - 1$.
TRP	Specifies t_{RP} value of the SDRAM in EMIF clock cycles. TRP = $(t_{RP}/t_{cyc}) - 1$.
TRCD†	Specifies t_{RCD} value of the SDRAM in EMIF clock cycles. TRCD = $(t_{RCD}/t_{cyc}) - 1$.
INIT	Forces an initialization of all SDRAM present. INIT = 0, no effect. INIT = 1, initialize SDRAM in each CE space configured for SDRAM.

† On the C64x, TRCD specifies the number of ECLKOUT1 cycles between an ACTV command and a READ or WRT command (CAS). The separation is maintained while driving write data 1 cycle earlier.

Table 8. EMIF SDRAM Control Register Bit Field Description (Continued)

Field	Description
RFEN	Refresh enable. RFEN = 0, SDRAM refresh disabled. RFEN = 1, SDRAM refresh enabled.
SDWID	SDRAM width select. (C620x/C670x) SDWID = 0, page size of 512 words (9-column address pins) SDWID = 1, page size of 256 words (8-column address pins)
SDCSZ	SDRAM column size. (C621x/C671x/C64x) SDCSZ = 00: 9-column address pins (512 elements per row) SDCSZ = 01: 8-column address pins (256 elements per row)) SDCSZ = 10: 10-column address pins (1024 elements per row) SDCSZ = 11: reserved
SDRSZ	SDRAM row size. (C621x/C671x/C64x) SDRSZ = 00: 11 row address pins (2048 rows per bank) SDRSZ = 01: 12 row address pins (4096 rows per bank) SDRSZ = 10: 13 row address pins (8192 rows per bank) SDRSZ = 11: reserved
SDBSZ	SDRAM bank size. (C621x/C671x/C64x) SDBSZ = 0: one bank-select pin (two banks) SDBSZ = 1: two bank-select pins (four banks)

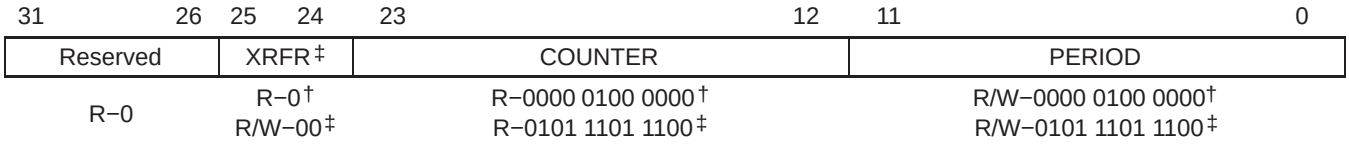
† On the C64x, TRCD specifies the number of ECLKOUT1 cycles between an ACTV command and a READ or WRT command (CAS). The separation is maintained while driving write data 1 cycle earlier.

2.5.4 SDRAM Timing Register (SDTIM)

The SDRAM timing register controls the refresh PERIOD for SDRAM in terms of EMIF clock cycles, t_{cyc}. t_{cyc} is twice the CPU clock period for the C620x/C670x. t_{cyc} is equal to the ECLKOUT period on the C621x/C671x/C64x. When the counter reaches zero, it is automatically reloaded with the PERIOD and continues decrementing. Figure 22 shows the register configuration for SDTIM, and Table 9 describes the bit fields.

The C621x/C671x and C64x can control the number of refreshes performed when the refresh counter expires via the XRFR field. Up to four refreshes can be performed when the refresh counter expires. This field is useful because the C621x/C671x and C64x does not differentiate between trickle and urgent refreshes. When the refresh counter expires, the C621x/C671x and C64x EMIF interrupts any accesses as soon as possible to execute the required number of refreshes.

Figure 22. EMIF SDRAM Timing Register



Legend: R = Read, R/W= Read/Write
† Applies to C620x/C670x only
‡ Applies to C621x/C671x/C64x only

Table 9. EMIF SDRAM Refresh Period Bit Field Description

Field	Description
PERIOD	For C620x/C670x, refresh period in CLKOUT2 cycles For C621x/C671x, refresh period in ECLKOUT cycles For C64x, refresh period in ECLKOUT1 cycles
COUNTER	Current value of the refresh counter.
XRFR †	Extra refreshes: controls the number of refreshes performed to SDRAM when the refresh counter expires

† Applies to C621x/C671x/C64x only

2.5.5 C621x/C671x/C64x SDRAM Extension Register (SDEXT)

The SDRAM extension register of the C621x/C671x/C64x allows programming of many SDRAM timing parameters. This programmability allows the C621x/C671x/C64x to interface to a wide variety of SDRAMs. Also, the timing register allows the interface to be tweaked to the characteristics of a specific SDRAM rather than use a set of default parameters that generally apply to worst-case parameters of a broad range of SDRAMs.

The SDRAM extension register applies to all SDRAM memory spaces in a system, so SDRAMs with identical timing characteristics must be used. Alternatively, the register can be programmed according to the worst-case timings of all of the SDRAMs in a system so that the system works correctly.

31	21	20	19 18	17	16
Reserved		WR2RD	WR2DEAC	WR2WR	R2WDQM
R−0		R/W−0	R/W−11	R/W−0	R/W−1

15	14 13 12	11 10	9	8 7	6 5	4	3 2 1	0
R2WDQM	RD2WR	RD2DEAC	RD2RD	THZP	TWR	TRRD	TRAS	TCL
R/W−1	R/W−111	R/W−11	R/W−0	TW,+11	R/W−11	R/W−1	R/W−111	R/W−1

Legend: R = Read, R/W= Read/Write

Figure 23. C621x/C671x/C64x SDRAM Extension Register

Table 10. C621x/C671x/C64x EMIF SDRAM Extension Register Bit Field Description

Field	Description †
TCL	Specified CAS latency of the SDRAM in ECLKOUT cycles TCL = 0, CAS latency = 2 ECLKOUT cycles TCL = 1, CAS latency = 3 ECLKOUT cycles
TRAS	Specifies t_{RAS} value of the SDRAM in ECLKOUT cycles T RAS = t_{RAS} – 1
TRRD	Specifies t_{RRD} value of the SDRAM in ECLKOUT cycles TRRD = 0, then t_{RRD} = 2 ECLKOUT cycles TRRD = 1, then t_{RRD} = 3 ECLKOUT cycles
TWR	Specifies t_{WR} value of the SDRAM in ECLKOUT cycles TWR = t_{WR} – 1
THZP	Specifies t_{HZP} value of the SDRAM in ECLKOUT cycles THZP = t_{HZP} – 1
RD2RD	Specifies number of cycles between READ to READ command (same CE space) of the SDRAM in ECLKOUT cycles RD2RD = 0, READ to READ = 1 ECLKOUT Cycle RD2RD = 1, READ to READ = 2 ECLKOUT Cycle
RD2DEAC	Specifies number of cycles between READ to DEAC/DCAB of the SDRAM in ECLKOUT cycles RD2DEAC = (# of cycles READ to DEAC/DCAB) – 1
RD2WR	Specifies number of cycles between READ to WRITE command of the SDRAM in ECLKOUT cycles RD2WR = (# of cycles READ to WRITE) – 1

† For C64x, ECLKOUT referenced in this table is equivalent to ECLKOUT1.

Table 10. C621x/C671x/C64x EMIF SDRAM Extension Register Bit Field Description (Continued)

Field	Description †
R2WDQM	Specifies number of cycles that BEx signals must be high preceding a WRITE interrupting a READ R2WDQM = (# of cycles BEx high) – 1
WR2WR	Specifies minimum number of cycles between WRITE to WRITE command of the SDRAM in ECLKOUT cycles WR2WR = (# of cycles WRITE to WRITE) – 1
WR2DEAC	Specifies minimum number of cycles between WRITE to DEAC/DCAB command of the SDRAM in ECLKOUT cycles WR2DEAC = (# of cycles WRITE to DEAC/DCAB) – 1
WR2RD	Specifies minimum number of cycles between WRITE to READ command of the SDRAM in ECLKOUT cycles WR2RD = (# of cycles WRITE to READ) – 1

† For C64x, ECLKOUT referenced in this table is equivalent to ECLKOUT1.

2.6 Interchangeable SDRAM Devices and Upgrading (C64x only)

The improved features and addressing of the C64x allows the device to be manipulated so that it can interface to multiple SDRAM devices with slightly different page characteristics from each other. This capability may allow the user to swap and upgrade the current SDRAM devices in the system with newer devices, given that a few specifications are met.

The C64x page register always stores 16 bits of address, instead of being limited to the number of row address bits plus the number of bank address bits as it is in the C621x/C671x. Also, the C64x can interface to 256M bytes of memory per CE space, compared to the C6x0x that can only interface to 16M bytes of memory per CE space, which limits the number of compatible memories on the market today. Even though the EMIF has only 1 SDCTL register for all four CE spaces, the extra bits in the page register can be manipulated to allow the use of multiple SDRAM devices and to allow for future upgrades.

The first constraint for this configuration is that all the SDRAMs connected to the four CE spaces must have the same number of COLUMN bits. Also, with any SDRAM interface, the number of column, row, and bank bits must fall within those specified by the device. In order to upgrade a SDRAM device, the footprint of the new memory device must match the old.

To upgrade an existing SDRAM device or add an additional, larger SDRAM device, the memories should be connected such that their BANK SELECTS are always common. The EMIF should then be configured according to the smallest row/bank combination. See Figure 24 for an example of two logical addresses for two types of SDRAM devices.

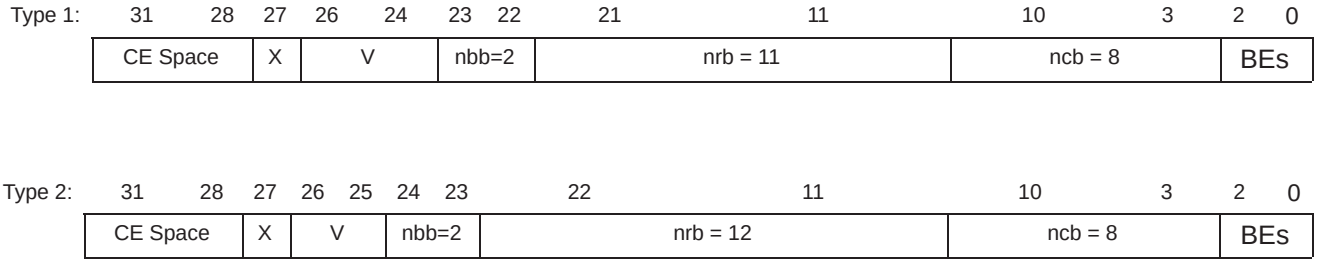


Figure 24. SDRAM Logical Address Bits

Given two memory types with different page characteristics, such as Type 1 and Type 2 seen in Figure 24, the EMIF must be configured to match that of Type 1. Using this configuration the bank select bits, BA0 and BA1, are connected as logical address bits 22 and 23. For the Type 2 memory device, since BA0 and BA1 are connected to logical address bits 22 and 23, the most significant row address bit will then be driven out on bit 24. Figure 25 shows the new configuration of the logical address bits and the non-linearly ordered row bits (rb[x] in the figure). This will allow us to take advantage of all the banks of the SDRAM and access all parts of the memory map for both SDRAMs.

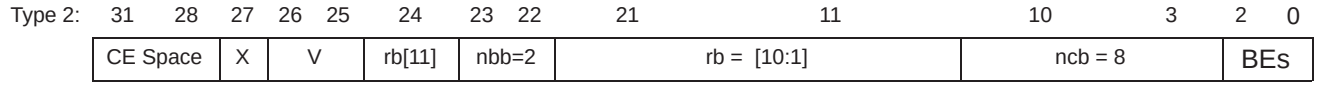
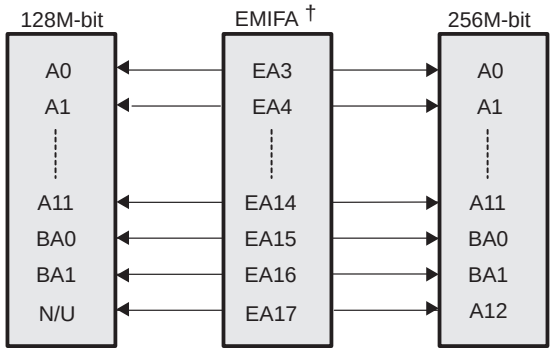


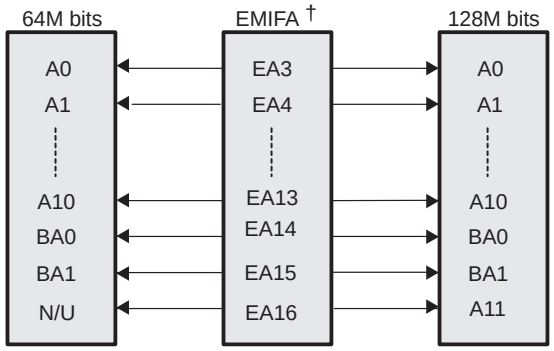
Figure 25. Modified Type 2 Logical Address Bits

This new logical address will allow the bank select pins of the EMIF to always connect with the bank select pins on the SDRAM, which will be driven by logical address bits 22 and 23 for Type 1 in Figure 24 and Type 2 in Figure 25. Figure 26 shows how this configuration should be set up at the pins to allow the interchangeability between two different SDRAM devices. Note for the 256M-bit device in Figure 26 that A12 is not connected to the address bit after A11, but rather BA0 and BA1 are placed in between the two. The same occurs for the 128M-bit device in Figure 27, except that A11 is placed after BA0 and BA1.



† EMIFB uses pins EA[x−2], where x is the pin number for EMIFA.

Figure 26. EMIFA to SDRAM Pin Interface for x16-Bit SDRAM



† EMIFB uses pins EA[x−2], where x is the pin number for EMIFA.

Figure 27. EMIFA to SDRAM Pin Interface for x32 Bit SDRAM

Table 11 shows the different SDRAM configurations that are compatible with the previous method.

Table 11. Upgradeable and Compatible SDRAM Devices

SDRAM Width	Column Addressing	Interchangeable Sizes
x32	A[0:7]	64 Mb, 128 Mb
x16	A[0:8]	128 Mb, 256 Mb

3 SDRAM

3.1 SDRAM Commands

The EMIF supports the SDRAM commands described Table 12. These commands are detailed in the following sections.

Table 12. EMIF SDRAM Commands

Command	Function
ACTV	Activate the selected bank and select the row.
READ	Input the starting column address and begin the read operation.
WRT	Input the starting column address and begin the write operation.
MRS	Mode register set. Configure SDRAM mode register.
REFR	Auto refresh cycle with internal address
DCAB	Deactivate (also known as precharge) all banks.
DEAC†	Deactivate single bank. Selected by bank-select address outputs.†
SLFREFR‡	Self-refresh mode‡

† DEAC is supported on C621x/C671x/C64x only.
‡ C64x only

Table 13. Truth Table for SDRAM Commands

SDRAM:	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A[19:16]	A[15:11]	A10	A[9:0]
16-bit EMIF:†	**SDCKE**	$\overline{CE}$	**SDRAS**	**SDCAS**	**SDWE**	**EA[20:17]‡**	**EA[16:12]**	**EA11**	**EA[10:1]**
32-bit EMIF:†	**SDCKE§**	$\overline{CE}$	**SDRAS**	**SDCAS**	**SDWE**	**EA[21:18]¶**	**EA[17:13]**	**EA12#**	**EA[11:2]☆**
64-bit EMIF:†	**SDCKE**	$\overline{CE}$	**SDRAS**	**SDCAS**	**SDWE**	**EA[22:19]‡**	**EA[18:14]**	**EA13**	**EA[12:3]‖**
ACTV	H	L	L	H	H	0001b or 0000b¶	Bank/Row	Row	Row
READ	H	L	H	L	H	X	Bank/ Column	L	Column
WRT	H	L	H	L	L	X	Bank/ Column	L	Column
MRS	H	L	L	L	L	L	L/Mode	Mode	Mode
DCAB	H	L	L	H	L	X	X	H	X
DEAC	H	L	L	H	L	X	Bank/X	L	X
REFR	H	L	L	L	H	X	X	X	X
SLFREFR	L	L	L	L	H	X	X	X	X

Legend: Bank = Bank Address; Row = Row Address; Column = Column Address; L = Low = 0b; H = High = 1b; X = Previous value; Mode = Mode Select

† 16-bit EMIF includes C64x EMIFB; 32-bit EMIF includes all C62x/C67x EMIF, both 32-bit and 16-bit interfaces; 64-bit EMIF includes C64x EMIFA, both 64-bit and 32-bit interfaces.

‡ For C64x DSP, upper address bits are used during ACTV to indicate non-PDT (0001b) vs. PDT (0000b) access. During all other accesses, address bits indicated with X hold previous value.

§ SDCKE does not exist on C62x/C67x DSP, or on C64 EMIFB.

¶ For C62x/C67x DSP, upper address bits are reserved for future use. Undefined.

SDA10 is used on C620x/C670x DSP. EA12 is used on C621x/C671x DSP.

‖ EMIF address numbering for the C64x 32-bit EMIFA begins with EA3 to maintain signal name compatibility with the C64x 64-bit EMIFA.

☆ EMIF address numbering for the C6712/C6712C 16-bit EMIF begins with EA2 to maintain signal name compatibility with the C62x/C67x 32-bit EMIF.

3.1.1 Timing Requirements

Several SDRAM timing parameters decouple the EMIF from SDRAM speed limitations. For the C6201B/C6202/C6203/C6204/C6205/C6701, three of these parameters are programmable via the EMIF SDRAM control register; the remaining two are assumed to be static values, as shown in Table 14. The three programmable values assure that EMIF control of SDRAM obeys these minimum timing requirements. Consult the manufacturer's data sheet for the particular SDRAM.

Table 14. C620x/C670x SDRAM Timing Parameters

Parameter	Description	Value in EMIF Clock Cycles
t_{RC}	REFR command to ACTV, MRS, or subsequent REFR command	TRC + 1
t_{RCD}	ACTV command to READ or WRT command	TRCD + 1
t_{RP}	DCAB command to ACTV, MRS, or REFR command	TRP + 1
t_{RAS}	ACTV command to DCAB command	7
t_{nEP}	Overlap between read data and a DCAB command	2

NOTE: Cycles shown in the following timing diagrams have TRCD = 10b (t_{RCD} = 3 CLKOUT2 cycles).

The C621x/C671x/C64x has additional programmable timing parameters that are programmable via the SDRAM control register and the SDRAM extension register. These parameters are a superset of the parameters of the C620x/C670x (see Table 15). Consult the manufacturer's data sheet for the particular SDRAM.

Table 15. C621x/C671x/C64x SDRAM Timing Parameters

Parameter	Description	Value in EMIF Clock Cycles
t_{RC}	REFR command to ACTV, MRS, or subsequent REFR command	TRC + 1
t_{RCD}	ACTV command to READ or WRT command	TRCD + 1
t_{RP}	DCAB/DEAC command to ACTV, MRS, or REFR command	TRP + 1
t_{CL}	CAS Latency of the SDRAM	TCL + 2
t_{RAS}	ACTV command to DEAC/DCAB command	TRAS + 1
t_{RRD}	ACTV bank A to ACTV bank B (same CE space)	TRRD + 2
t_{WR}	Write recovery, time from last data out of C6000 (write data) to DEAC/DCAB command	TWR + 1
t_{HZP}	High Z from precharge, time from DEAC/DCAB to SDRAM outputs (read data) in high Z	THZP + 1

The C621x/C671x/C64x also allows the user to program other functional parameters of the SDRAM controller. These parameters are not explicitly spelled out in the timing parameters of a data sheet, but the user must ensure that the parameters are programmed to a valid value. For most common SDRAMs, the following values can be used (see Table 16). The user must ensure that these values are appropriate for any specific SDRAM.

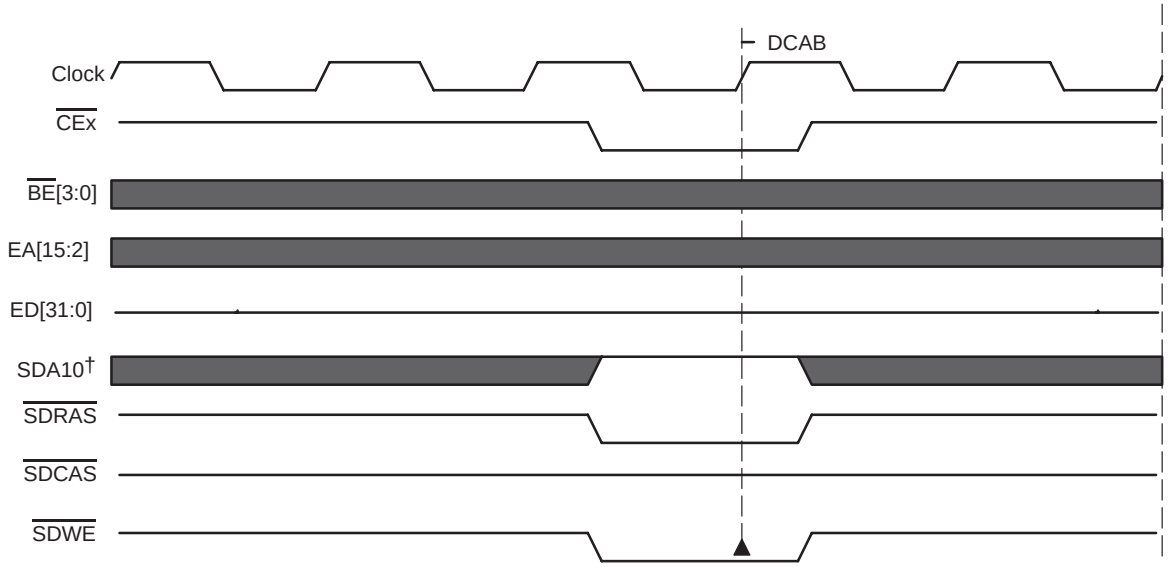
Table 16. C621x/C671x/C64x Recommended Values for CMD to CMD Parameters

Parameter	Description	Value in EMIF Clock Cycles	Suggested Value for CL = 2	Suggested Value for CL = 3
READ to READ	READ command to READ command. Used to interrupt a READ burst for random READ addresses.	RD2RD + 1	RD2RD = 0	RD2RD = 0
READ to DEAC	Used in conjunction with t_{HZP}. Specifies the minimum amount of time between READ command and DEAC/DCAB command.	RD2DEAC + 1	RD2DEAC = 1	RD2DEAC = 1
READ to WRITE	READ to WRITE command. The value programmed in this parameter depends on t_{CL}. READ to WRITE should be CAS latency plus 2 cycles (in EMIF clock cycles) to provide 1 turnaround cycle before WRITE command.	RD2WR + 1	RD2WR = 3	RD2WR = 4
BEx high before write interrupting read	Specifies the number of cycles that the BEx outputs should be high before a write is allowed to interrupt a read. This is related to READ to WRITE parameter.	R2WDQM + 1	R2WDQM = 1	R2WDQM = 2
WRITE to WRITE	Number of cycles between a WRITE interrupting a WRITE. Used for random WRITEs.	WR2WR + 1	WR2WR = 0	WR2WR = 0
WRITE to DEAC	Number of cycles between a WRITE command and a DEAC/DCAB command	WR2DEAC + 1	WR2DEAC = 1	WR2DEAC = 1
WRITE to READ	Number of cycles between a WRITE command and a READ command	WR2RD + 1	WR2RD = 0	WR2RD = 0

3.1.2 Deactivation (DCAB and DEAC)

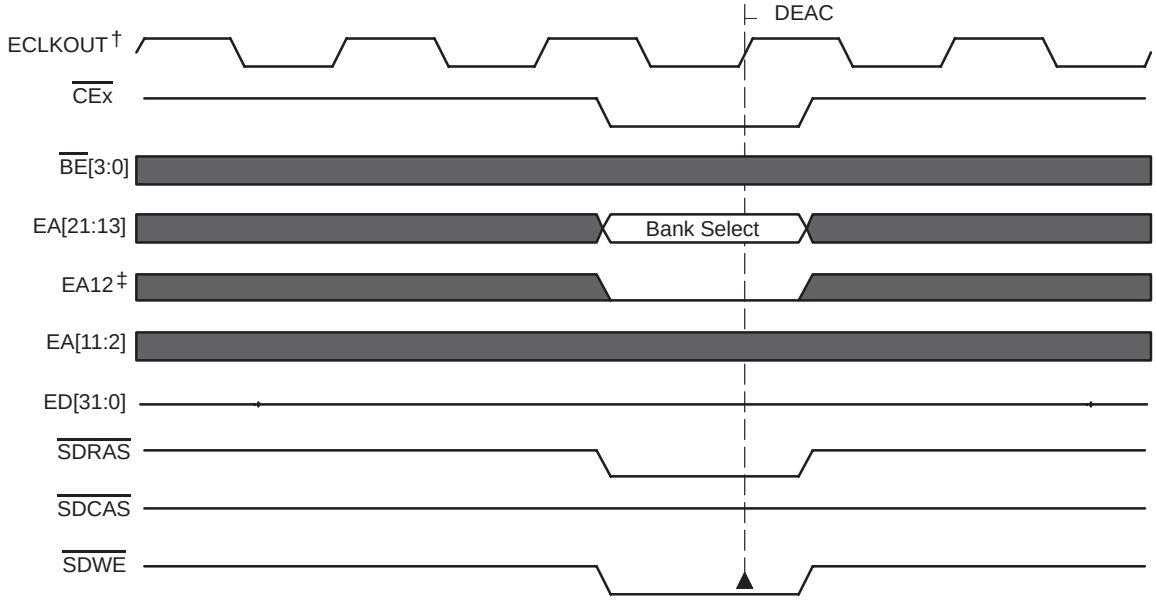
The DCAB command is issued to close all active pages of memory (shown in Figure 28). The SDRAM deactivation (DCAB) is performed after a hardware reset or when INIT = 1 in the EMIF SDRAM control register. This cycle is required by the SDRAMs prior to REFR and MRS. For the C620x/C670x, a DCAB is also issued when a page boundary is crossed. During the DCAB command, SDA10 (for C6201/C6202/C6203/C6204/ C6205/C6211), EA12 (C621x/C671x), EA13 (C64x EMIFA), or EA11 (C64x EMIFB) is driven high to ensure that all SDRAM banks are deactivated.

The C621x/C671x/C64x also supports the DEAC command (shown in Figure 29). The C621x/C671x/C64x has the ability to have more than one page open in a CE space simultaneously. The DEAC command allows the C621x/C671x/C64x to close only the desired page. When a page boundary is crossed, the DEAC command is used to close the open page. The C621x/C671x/C64x still supports the DCAB command to close all open pages before a REFR and MRS command is issued.



† For C621x/C671x, EA12 is used.
For C64x EMIFA, EA13 is used.
For C64x EMIFB, EA11 is used.

Figure 28. SDRAM DCAB—Closes All Banks in a CE Space



† For C64x, ECLKOUT1 is used.
‡ For C64x EMIFA, EA13 is used. For C64x EMIFB, EA11 is used.

Figure 29. C621x/C671x/C64x SDRAM DEAC—Closes Single Bank Specified by BS

3.1.3 Activate (ACTV)

The Activate (ACTV) command is issued before a read or write to a new row of SDRAM. The ACTV command opens up a page of memory, allowing future accesses (reads or writes) with minimum latency. As shown in Figure 30 and Figure 31, when an ACTV command is issued by the EMIF, a delay of t_{RCD} is incurred before a read or write command is issued (in this example, t_{RCD} = 3 EMIF clock cycles). Reads or writes to the currently active row and bank of SDRAM can achieve much higher throughput than reads or writes to random areas because every time a new page is accessed, the ACTV command must be issued.

3.1.4 SDRAM Read (READ)

For an SDRAM read, the selected bank is activated with the row address during the ACTV command. In this example, three read commands are performed to three successive column addresses in the same page.

3.1.4.1 C620x/C670x Read

The C620x/C670x EMIF uses a CAS latency of 3 and a burst length of 1. The three-cycle read latency causes data to appear three cycles after the corresponding column address, as shown in Figure 30.

If a Refresh cycle or an access to a different page of memory is required, a DCAB cycle is performed following the last column access to deactivate the bank. An idle cycle is inserted between the final read command and the DCAB command to meet SDRAM timing requirements. The transfer of data completes during and past the DCAB command (controlled by t_{nEP}). If no new access is pending, the DCAB command is not performed until the page information becomes invalid.

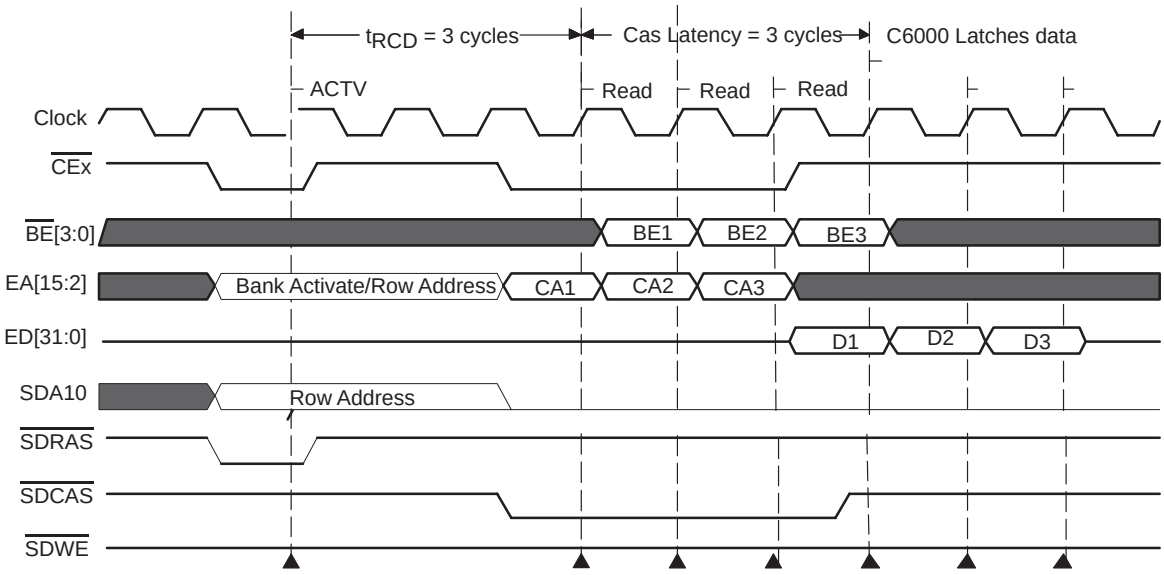


Figure 30. C620x/C670x SDRAM Read—CAS Latency 3

3.1.4.2 C621x/C671x Read

The C621x/C671x EMIF can be programmed to use a CAS latency of either two or three cycles. The burst length is fixed at four words for both reads and writes. In general, using a faster CAS latency results in slightly slower AC timings for the SDRAM device. This may require running the EMIF at a slower clock frequency. Depending on the requirements of the system, this may be acceptable.

The example shown in Figure 31 is a three-word read and uses a CAS latency of three cycles. The three-cycle read latency causes data to appear three cycles after the corresponding column address. This example assumes that no accesses are pending to the SDRAM. In this case, D4 is allowed to be driven by the SDRAM, but the C6000 ignores this data because only three words are required in this example.

If no new access is pending, the DEAC command is not performed until the page information becomes invalid.

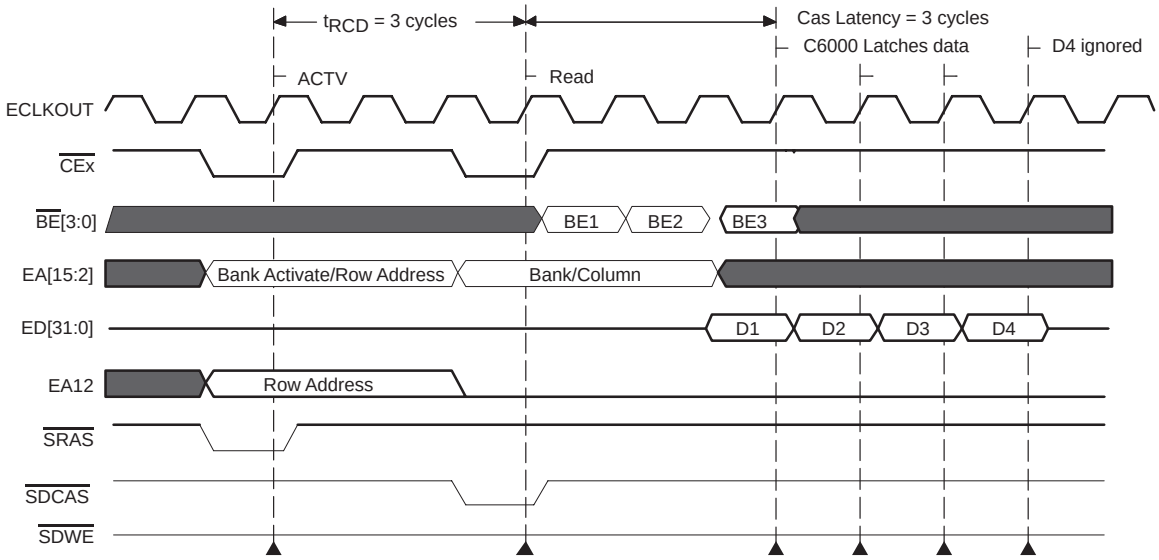


Figure 31. C621x/C671x SDRAM Read—CAS Latency 3

If a refresh cycle is pending, a DCAB cycle will be performed to deactivate the bank. If an access to a different page of memory in the same bank of SDRAM is required (that is, a page miss), a DEAC command will be issued following the last column access, followed by an ACTV to open the correct page.

The DEAC/DCAB command timing is controlled by THZP and RD2DEAC. These parameters are ideally programmed so that the transfer of data completes during and after the DCAB/DEAC command. The example in Figure 32 shows the same example as shown in Figure 30, but with a new access pending to a different page in the same bank. With THZP = 10b (tHZP = 3 cycles), the DEAC command is issued at the same time as D1 is latched, causing the outputs of the SDRAM to stop driving data before D4. This is good because only three words were needed. Because the next access is to the same bank of SDRAM, the ACTV command is issued as soon as possible and is controlled by the TRP parameter, which is three cycles in this example.

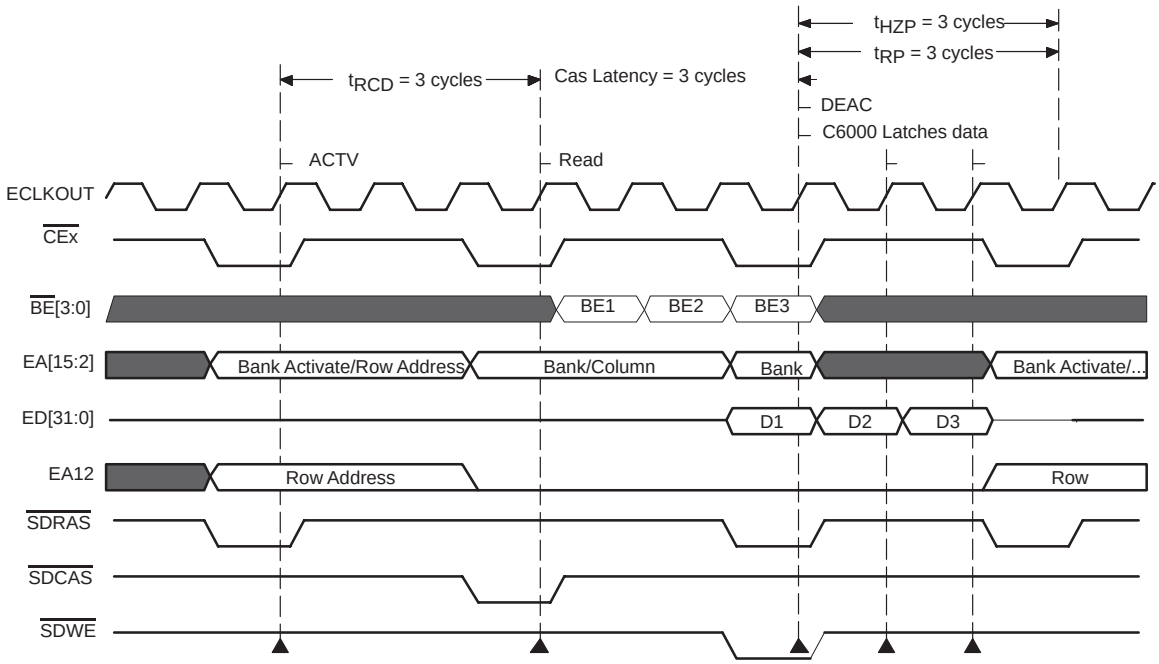
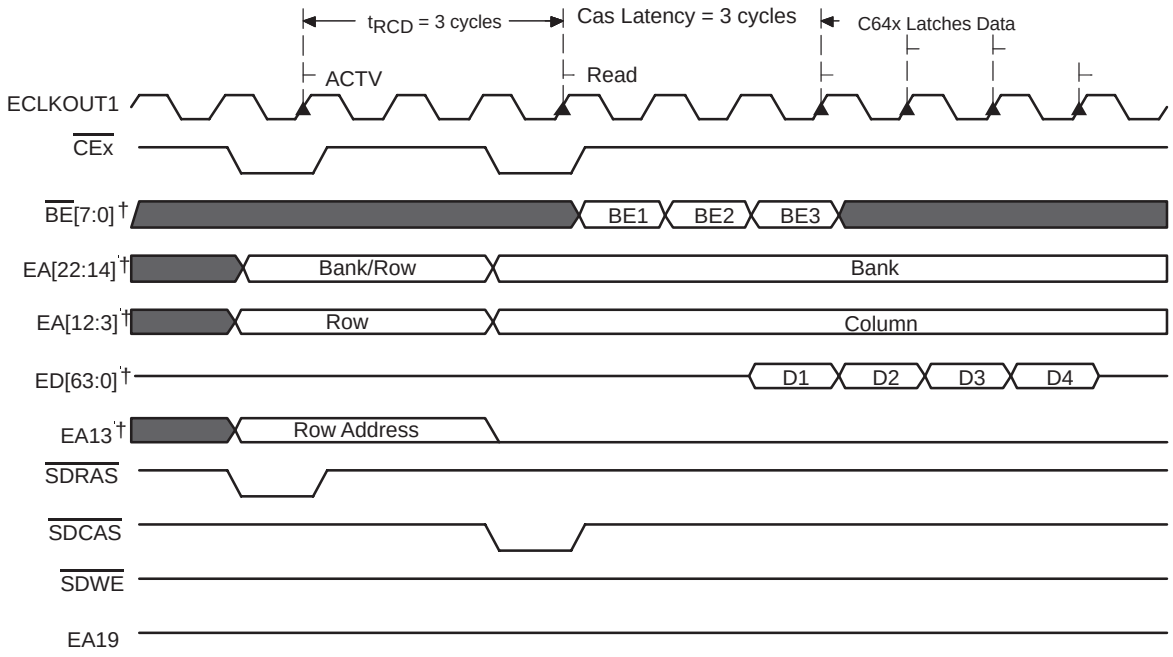


Figure 32. C621x/C671x SDRAM Read With DEAC

3.1.4.3 C64x Read

The C64x also uses a burst length of four. For a basic SDRAM read, the read is almost identical to that of the C621x/C671x.

The example shown in Figure 33 is a three doubleword (EMIFA) or half-word (EMIFB) read burst from SDRAM. A CAS latency of three cycles is used, which causes data to appear three cycles after the corresponding column address. The example assumes that no accesses are pending to the SDRAM. The ACTV command is not issued for future accesses to the same open page.



† For EMIFB, BE[1:0], EA[20:12], EA[10:1], ED[15:0], and EA11, respectively, are used.

Figure 33. C64x SDRAM Read—CAS Latency 3

If a refresh cycle is pending, a DCAB cycle will be performed to deactivate the bank. If an access to a different page of memory in the same bank of SDRAM is required (that is, a page miss), a DEAC command will be issued following the last column access, followed by an ACTV to open the correct page.

3.1.5 SDRAM Write (WRT)

For an SDRAM write, the selected bank is activated with the row address during the ACTV command. In this example, three write commands are performed to three successive column addresses in the same page.

3.1.5.1 C620x/C670x SDRAM Writes

All SDRAM writes have a burst length of 1 (see Figure 34). The bank is activated with the row address during the ACTV command. There is no latency on writes, so data is output on the same cycle as the column address. Byte and half-word writes are enabled via the appropriate DQM inputs. Following the final write command, an idle cycle is inserted to meet SDRAM timing requirements. If required, the bank is then deactivated with a DCAB command ,and the memory interface can begin a new page access. If no new access is pending, or if an access is pending to the same page, the DCAB command is not performed until the page information becomes invalid.

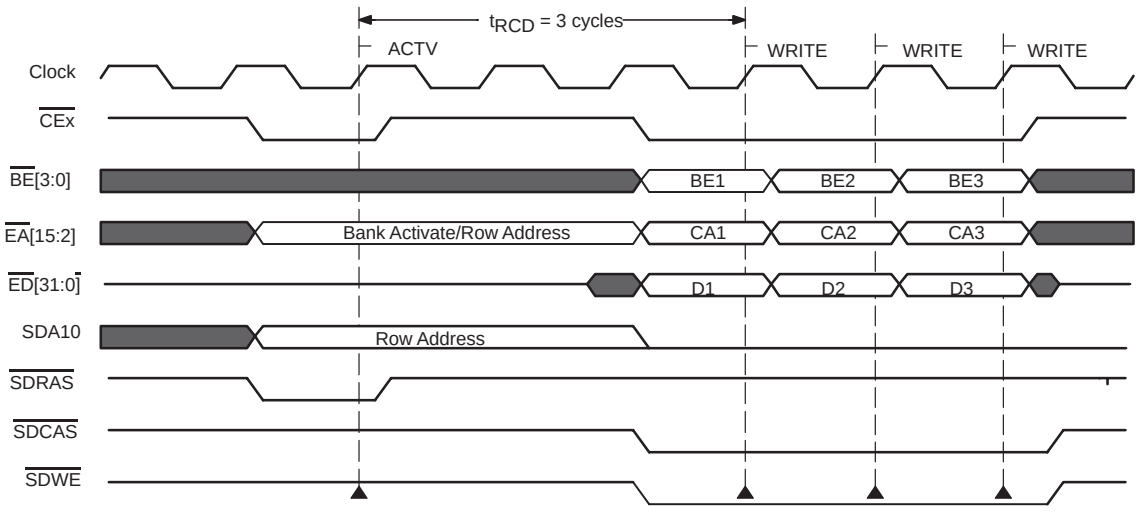


Figure 34. C620x/C670x SDRAM Burst Length 1 Write

3.1.5.2 C621x/C671x SDRAM Writes

For the C621x/C671x, all SDRAM writes have a burst length of 4 (see Figure 35). The bank is activated with the row address during the ACTV command. There is no latency on writes, so data is output on the same cycle as the column address. Byte and half-word writes are enabled via the appropriate DQM inputs. If less than a four-word burst is required, write data is masked out via the BEx outputs (tied to DQM inputs of the SDRAM).

Following the final write command, idle cycles are inserted according to the TWR, WR2DEAC, and/or WR2RD parameters to meet SDRAM timing requirements. If a refresh is pending, all banks are then deactivated with a DCAB command. If a page miss has occurred, a DEAC command is issued followed by an ACTV to the correct page. The DEAC/DCAB command is not performed until the page information becomes invalid.

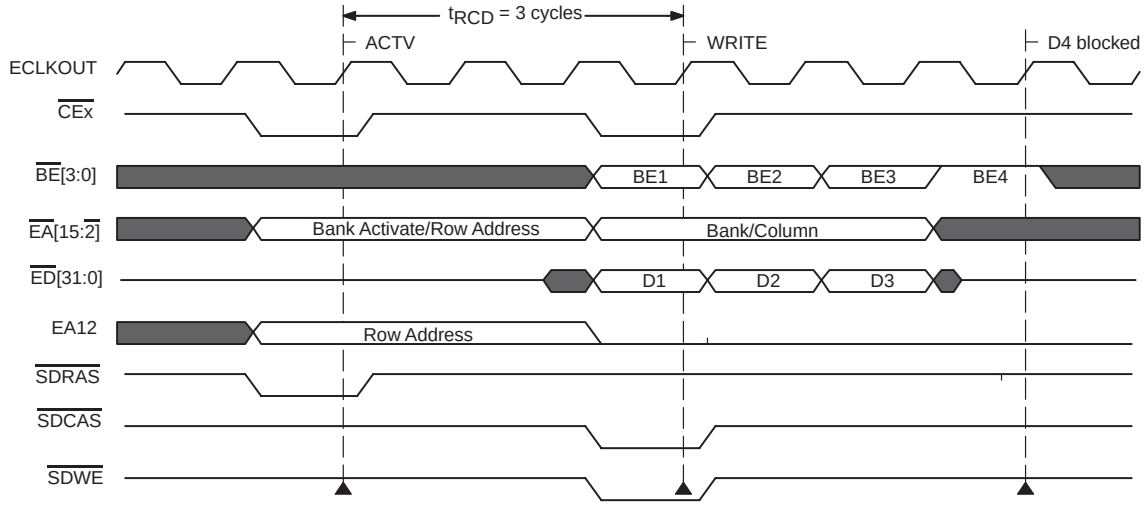


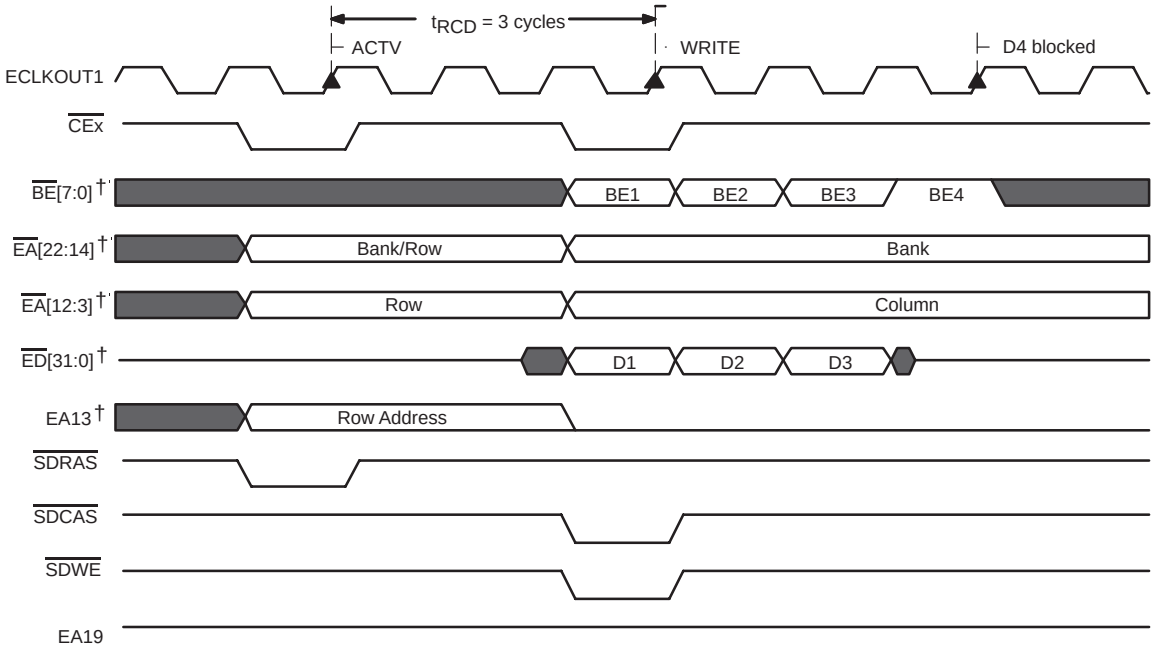
Figure 35. C621x/C671x SDRAM Burst Length 4 Write

3.1.5.3 C64x SDRAM Writes

The C64x also uses a burst length of four. The write is almost identical to that of the C621x/C671x with the following exception:

- Write data is driven one cycle early

The example shown in Figure 36 is a three doubleword (EMIFA) or half-word (EMIFB) write on the C64x. There is no latency on writes so data is output on the same cycle as the column address. The example assumes that no accesses are pending to the SDRAM. An ACTV command is not issued for future accesses to the same open page.



† For EMIFB, BE[1:0], EA[20:12], EA[10:1], ED[15:0], and EA11, respectively, are used.

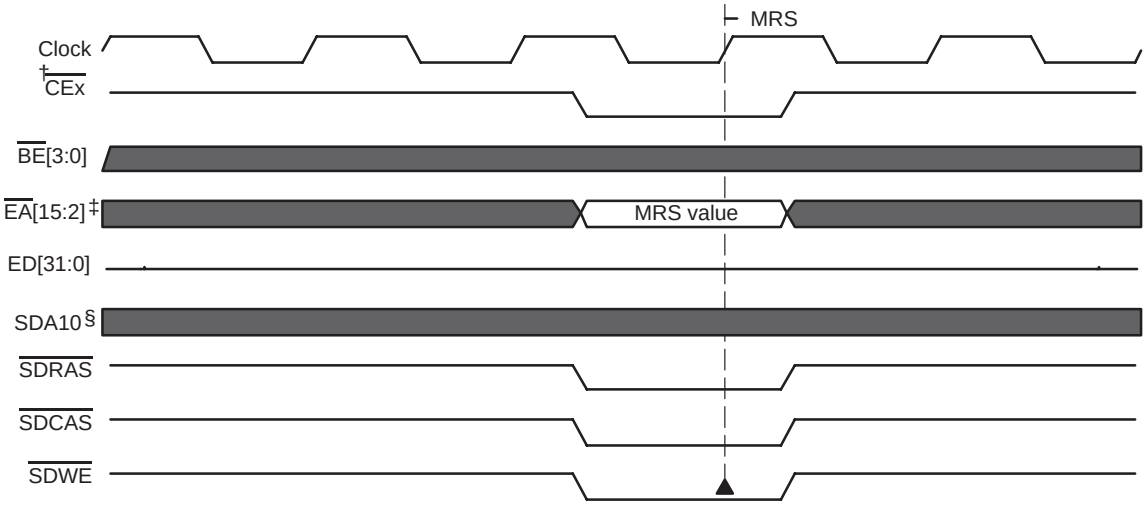
Figure 36. C64x SDRAM Burst Length 4 Write

3.1.6 Mode Register Set (MRS)

The mode register is located in the external SDRAM memory that dictates its operating characteristics. When initializing SDRAM, the EMIF must set this register to the value described here before normal read or write accesses can occur.

The EMIF automatically performs a DCAB command followed by eight refreshes, followed by an MRS command whenever the INIT field in the EMIF SDRAM control register is set. INIT can be set by device reset or a user write. As with the DCAB and REFR commands, MRS commands are sent to all CE spaces configured as SDRAM. Following the MRS cycle, the INIT bit is cleared to prevent multiple MRS cycles. The C620x/C670x EMIF always uses a mode register value of 0x0030 during an MRS command. The C621x/C671x/C64x uses a value of either 0x0032 or 0x0022, depending on the CAS latency of the interface. Figure 37 shows the mapping between mode register bits, EMIF pins, and the mode register value.

Table 17 shows the SDRAM configuration selected by this mode register value, and Table 18 shows the mplied SDRAM configuration by the MRS value.



† Clock = SDCLK for C6201/C6701.
CLKOUT2 for all C620x/C670x except C6201/C6701.
ECLKOUT for C621x/C671x.
ECLKOUT1 for C64x.
‡ For C64x EMIFA, EA[16:3] is used instead.
For C64x EMIFB, EA[14:1] is used instead.
§ For C621x/C671x, EA12 is used. For C64x EMIFA, EA13 is used. For C64x EMIFB, EA11 is used.

Figure 37. SDRAM Mode Register Set: MRS Command

Table 17. Mode Register Value†

Mode Register Bit	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EMIF Pins	EA15	EA14	EA13	SDA10	EA11	EA10	EA9	EA8	EA7	EA6	EA5	EA4	EA3	EA2
Field	Reserved				Write Burst Length	Reserved		Read Latency			S/I	Burst Length		
C6201/C6202 /C6203/C6204/ C6205/ C6701	0	0	0	0	0	0	0	0	1	1	0	0	0	0
C621x/C671x/ C64x w/CL = 3	0	0	0	0	0	0	0	0	1	1	0	0	1	0
C621x/C671x/ C64x w/CL = 2	0	0	0	0	0	0	0	0	1	0	0	0	1	0

† For C64x EMIFA, EA[16:3] is used instead.
NOTE: For C64x EMIFB, EA[14:1] is used instead.

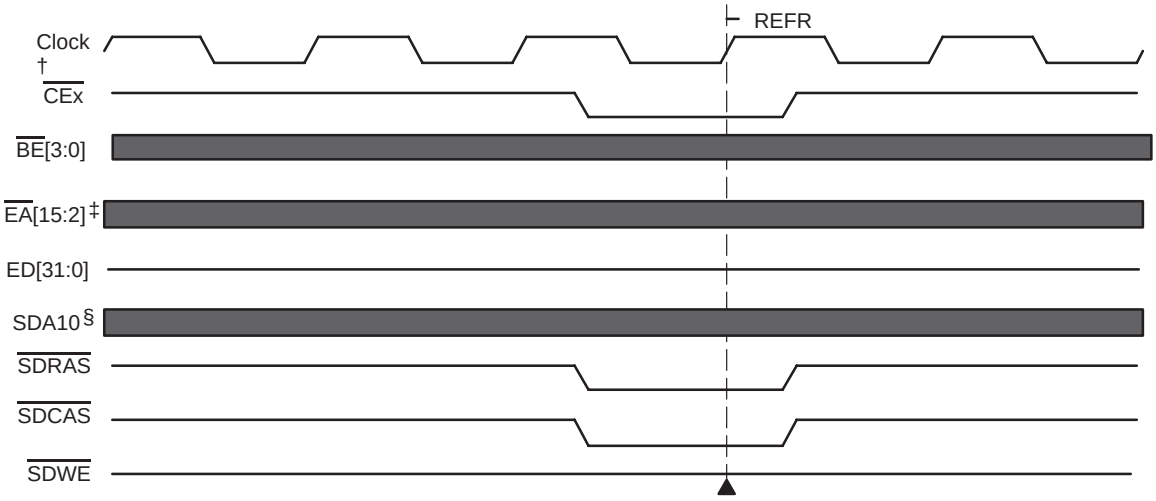
Table 18. Implied SDRAM Configuration by MRS Value

Field	C620x/C670x Selection	C621x/C671x/C64x Selection (CL = 3)	C621x/C671x/C64x Selection (CL = 2)
Write burst length	1	4	4
Read latency	3	3	2
Serial/interleave burst type	Serial	Serial	Serial
Burst length	1	4	4

3.1.7 Refresh

The RFEN bit in the SDRAM control register, shown in Figure 21, selects the SDRAM refresh mode of the EMIF. A value of 0 in the RFEN field disables all EMIF refreshes; the user must ensure that refreshes are implemented in an external device. A value of 1 in the RFEN field enables the EMIF to perform refreshes of SDRAM as described in this section.

The refresh command (REFR) is sent to all CE spaces configured to use SDRAM by the MTYPE field of the corresponding CE space control register. REFR is automatically preceded by a DCAB command. This ensures that all CE spaces selected with SDRAM are deactivated before refresh occurs. Page information is always invalid before and after a REFR command; thus a refresh cycle always forces a page miss on the next access. See Figure 38.



† *Clock = SDCLK for C6201/C6701.
CLKOUT2 for all C620x/C670x except C6201/C6701.
ECLKOUT for C621x/C671x.
ECLKOUT1 for C64x.
‡ For C64x EMIFA, EA[16:3] is used instead.
For C64x EMIFB, EA[14:1] is used instead.
§ For C621x/C671x, EA12 is used. For C64x EMIFA, EA13 is used. For C64x EMIFB, EA11 is used.

Figure 38. SDRAM Refresh

3.1.7.1 C620x/C670x Refresh Operation

Following the DCAB command, the EMIF begins performing *trickle* refreshes at a rate defined by the PERIOD value in the EMIF SDRAM control register, provided no other SDRAM access is pending.

The SDRAM interface monitors the number of refresh requests posted to it and performs them. Within the EMIF SDRAM control block, a 2-bit counter monitors the backlog of refresh requests. The counter increments once for each refresh request, and decrements once for each refresh cycle performed. The counter saturates at the values of 11 and at 00. At reset, the counter is automatically set to 11, to ensure that several refreshes occur before accesses begin.

The value of 11 indicates an urgent refresh condition, causing the page information register to be invalidated and forcing the controller to close the current SDRAM page. Thus, the EMIF SDRAM controller performs three REFR commands, decrementing the counter to 00 following the DCAB command before proceeding with the remainder of the current access. If SDRAM is present in multiple CE spaces, the DCAB-refresh sequence occurs in all spaces containing SDRAM.

During idle times on the SDRAM interface(s), if no request is pending from the EMIF, the SDRAM interface performs REFR commands as long as the counter value is nonzero. This feature reduces the likelihood of having to perform urgent refreshes during actual SDRAM accesses later. Note that if SDRAM is present in multiple CE spaces, this refresh occurs only if all interfaces are idle with invalid page information.

3.1.7.2 C621x/C671x/C64x Refresh Operation

The C621x/C671x/C64x EMIF does not use the concept of urgent versus trickle refresh. All refresh requests are considered high priority. If a refresh request is issued while a transfer is in progress, the EMIF will complete its current burst of data (see TMS320C64x EDMA Architecture (SPRA994) for default burst size), then perform the required number of refreshes (controlled by XRFR field). Once the refreshes have been completed, the transfer in progress will be resumed. The XRFR field allows up to four requests to be issued in succession each time the refresh counter expires. This gives the system designer the option of allowing requests to happen less often while still meeting the requirements of the SDRAM.

3.1.7.3 Self Refresh Mode (C64x Only)

The SLFRFR bit in the SDRAM control register (SDCTL) allows a user to force the EMIF to place the external SDRAM in a low-power mode, called Self Refresh. The SDRAM maintains valid data and consumes a minimal amount of power while in Self Refresh mode.

Self Refresh mode begins when a 1 is written to the SLFRFR bit and SDRAM exists in the system. The refresh enable bit, RFEN, in the SDCTL must be written with a 0 simultaneously. When the SLFRFR bit is asserted, all open pages of SDRAM are closed ,and a REFRESH command is issued on the same cycle that the SDCKE signal is driven low.

To exit SLFRFR mode, write a 0 to the SLFRFR bit and then immediately read back before performing other accesses. While the SLFRFR bit is asserted, the user should ensure that no SDRAM accesses are performed. Also, while in self refresh mode, the SDRAM clock (ECLKOUT1) can be turned off if it is not used elsewhere in the system ,and the system does not use the Hold interface.

The effects of the SLFRFR bit with a SDRAM in the system are summarized here:

- A write to SLFRFR while not in hold allows self refresh mode entry/exit.
- A write to SLFRFR while in hold will be ignored and no bit will be written.
- If HOLD request occurs while SLFRFR = 1, the EMIF ensures the device has been in self refresh mode at least TRAS cycles, where TRAS is defined in the SDEXT register. Then the EMIMF exits self refresh mode and after 16 ECLKOUT1 cycles, the EMIF will acknowledge the HOLD request.

3.2 SDRAM Initialization

After reset, none of the CE spaces are configured as SDRAM. The CPU should initialize all of the CE space control registers and the SDRAM extension register before performing SDRAM initialization by setting the INIT bit to 1. If SDRAM does not exist in the system, you should not write a 1 to the INIT bit.

The EMIF performs the following steps when INIT is set to 1:

1. Sends a DCAB command to all CE spaces configured as SDRAM.
2) Sends eight refresh commands.
3) Sends an MRS command to all CE spaces configured as SDRAM.

For the duration of SDRAM initialization, the $\overline{BE}$ signals are inactive high. The SDRAM initialization is noninterruptible by other EMIF accesses.

3.3 Monitoring Page Boundaries

Because SDRAM is a paged memory type, the EMIF SDRAM controller monitors the active row of SDRAM so that row boundaries are not crossed during the course of an access. To accomplish this monitoring, the EMIF stores the address of the open page and performs compares against that address for subsequent accesses to the SDRAM bank.

3.3.1 C620x/C670x Page Boundaries

The C620x/C670x allows a single page to be open in each CE space. The number of address bits compared is a function of the page size programmed in the SDWID field in the EMIF SDRAM control register. If SDWID = 0 in the SDRAM control register, the EMIF expects CE spaces configured as SDRAM to have page sizes of 512 words. Thus, the logical byte address bits compared are 25:11. If SDWID = 1, the EMIF expects CE spaces with SDRAM to have SDRAMs that have page sizes of 256. Thus, the logical byte address bits compared are 25:10.[4]

If a page boundary is crossed during the course of an access, the EMIF performs a DCAB command and starts a new row access. Note that simply ending the current access is not a condition that forces the active SDRAM row to be closed. The EMIF speculatively leaves the active row open until it becomes necessary to close it. This feature decreases the deactivate-reactivate overhead and allows the interface to fully capitalize on address locality of memory accesses.

[4] Note that the upper address bit, 25, for both 8-bit- and 16-bit-wide SDRAM is used to indicate the logical address range accessible for the EMIF, that is, the top of CE3, which is at address 0x03FFFFFF. Thus, 26 logical address lines (0:25) are needed.

3.3.1.1 *Crossing a Page Boundary*

As already stated above, if a write burst extends across the page boundary within the same CE space, the previous page must be closed before the correct page can be opened and the write continued. When this happens, the CAS and WE signals will transition to high, one cycle after the last write is performed. This occurs before the page is closed. The $\overline{\text{BEx}}$ signals will transition to high immediately after the last write is performed. This blocks any additional write that would be allowed by the CAS and WE signals staying high for an additional cycle. This behavior is true for C620x/C670x devices.

3.3.2 C621x/C671x Page Boundaries

The C621x/C671x allows four pages to be open simultaneously. Open pages can be distributed across all the CE spaces or can be located in the same CE space. For example, two pages can be open in CE0 and CE2 or four pages can be open in CE0. The maximum number of open pages in a single CE space is limited by the number of banks in the SDRAM, which is programmed into the SDBSZ field. Only one page can be open per bank at a time.

The combination of SDCSZ, SDRSZ, and SDBSZ control which logical address bits are compared to determine if a page is open. For example, a typical 2-bank x 512K x 16-bit SDRAM has settings of two banks, eleven row address bits, and eight column address bits. A 32-bit-wide SDRAM access uses logical address bits A[9:2] (two-bit offset for word addressing) to specify the column being accessed (that is, the address within a page). Bits A[20:10] specify the row offset (that is, the page within a bank) and bit A[21] specifies the bank. Logical address bits A[31:28] determine the CE space used.

If a page boundary is crossed during an access to the same bank in a CE space, the C621x/C671x performs a DEAC command and starts a new row access. If an access to a different bank is performed, the C621x/C671x EMIF does not always close the first page. Each bank of SDRAM in a CE space can simultaneously have an open page and pages are closed with a random replacement strategy. If a page miss occurs and the access is to a bank that currently has a page open, that bank must be closed to open the correct page. However, if an access occurs to a bank that does not have a page open, but all four page registers are in use, one of the four pages are randomly closed with a DEAC command, and the new page is opened.

For example, assume that an SDRAM that has two banks (such as the 2-bank x 512K x 16-bit device) is in CE0. Therefore, CE0, Bank0 and CE0, Bank1 can simultaneously have open pages. Assume Bank0 has an open page and Bank1 does not. If a new access to Bank0 results in a page miss, that page must be closed before the correct page in Bank0 can be opened. Any new access to Bank1 must first open the correct page. If all four page registers internal to the C6000 are in use (assuming that other CE spaces have open pages), a single page is closed at random and the correct page in CE0, Bank1 is opened. If all four page registers are not in use, CE0, Bank1, Pagex can be opened immediately. See Figure 39.

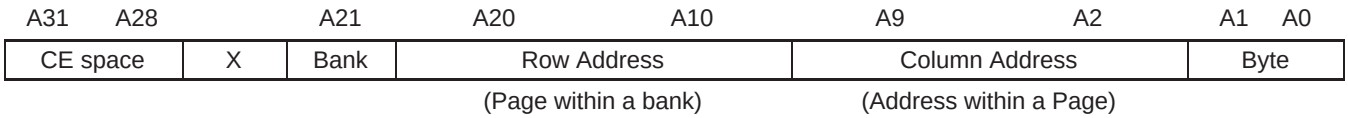


Figure 39. Logical Address Breakdown for 1 Bank Bit, 11 Row Bits, 8 Column Bits

3.3.3 C64x Page Boundaries

The C64x performs very similar to the C621x/C671x SDRAM paging scheme. Both allow four pages of SDRAM to be opened simultaneously, all in one CE space or spread across multiple CE spaces. Also, like the C621x/C671x, the number of column address bits controls the number of the least significant address bit stored in the page resister. The maximum number of open pages in a single CE space is limited by the number of banks in the SDRAM, which is programmed into the SDBSZ field.

Unlike the C621x/C671x, the C64x page register always stores 16 bits of address (instead of being limited by the number of row address bits plus the number of bank address bits (NRB_NBB)). Any logical address bits above the bank address bit are used as part of the page comparison. Also, address bits above the bank bits are used when issuing the row/column commands to the external SDRAM. This provides the device with more flexible designs and external visibility into the internal address aliasing.

The C64x EMIF employs a least recently used (LRU) page replacement strategy when necessary. When the total number of external SDRAM banks (not devices) exceeds four (since the EMIF only has four page registers) then the LRU strategy is used. If the total number of banks of SDRAM is less than or equal to four, then the page replacement strategy is fixed since SDRAM required that only one page can be open within a given bank. If a page miss is detected, then the C64x performs a DEAC command and starts a new row access.

Figure 40 shows an example of a 4−bank xIM x 32−bit SDRAM with two bank 645, twelve row address bits, and eight column address bits that is mapped to EMIFA.

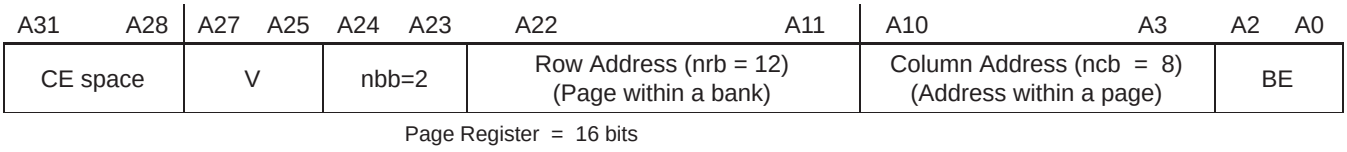


Figure 40. Logical Address Breakdown for 2 Bank Bits, 12 Row Bits, 8 Column Bits

3.4 Address Shift

Because the same EMIF pins address the row and column address, the EMIF interface appropriately shifts the address in row and column address selection. Table 19, Table 20, and Table 21 shows the translation between bits of the logical byte address and how they appear on the EA pins for row and column addresses. SDRAMs use the address inputs for control as well as address. With this consideration, the following items clarify the figure:

- The address line that corresponds to the SDRAM's bank-select bit is latched internally by the SDRAM controller. This ensures that the bank select remains correct during READ and WRT commands. Thus, EMIF maintains these values as shown in both row and column addresses.
- The EMIF forces the precharge disable (SDA10 on C620x/C670x, EA12 on C621x/C671x, EA13 on C64x EMIFA, EA11 on C64x EMIFB) to be low unless $\overline{RAS}$ is active low, yet high during DCAB commands at the end of a page of accesses. This prevents the auto precharge from occurring following a READ or WRT command.

Table 19. C620x/C670x Byte Address to EA Mapping for SDRAM $\overline{RAS}$ and $\overline{CAS}$[5]

EMIF Pins				EA [21:17]	EA 16	EA 15	EA 14	EA 13	SDA 10	EA 11	EA 10	EA 9	EA 8	EA 7	EA 6	EA 5	EA 4	EA 3	EA 2
SDRAM Pins	SDRAM Width	SDWID	DRAM Cmd			A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Address bit	x16	1	$\overline{RAS}$			23	22	21	20	19	18	17	16	15	14	13	12	11	10
			$\overline{CAS}$			23	22	21	L†	19	18	9	8	7	6	5	4	3	2
Address bit	x8	0	$\overline{RAS}$				23	22	21	20	19	18	17	16	15	14	13	12	11
			$\overline{CAS}$				23	22	L†	20	10	9	8	7	6	5	4	3	2

Legend: Bit is internally latched during an ACTV command.
Reserved for future use. Undefined.

Note: The $\overline{RAS}$ and $\overline{CAS}$ values indicate the bit of the byte address present on the corresponding EA pin during a $\overline{RAS}$ or $\overline{CAS}$ cycle.
† L = Low; SDA10 is driven low during READ or WRT commands to disable autoprecharge.

Table 20. C621x/C671x Byte Address to EA Mapping for SDRAM RAS and CAS[6]

No. of Column Address Bits	Interface Bus Width	DRAM Cmd	EA [21:17]	EA 16	EA 15	EA 14	EA 13	EA 12	EA 11	EA 10	EA 9	EA 8	EA 7	EA 6	EA 5	EA 4	EA 3	EA 2
				A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
8	8	$\overline{RAS}$		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
		$\overline{CAS}$		Bank‡				L†	L	L	7	6	5	4	3	2	1	0
	16	$\overline{RAS}$		23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
		$\overline{CAS}$		Bank‡				L†	L	L	8	7	6	5	4	3	2	1
	32	$\overline{RAS}$		24	23	22	21	20	19	18	17	16	15	14	13	12	11	10
		$\overline{CAS}$		Bank‡				L†	L	L	9	8	7	6	5	4	3	2
9	8	$\overline{RAS}$		23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
		$\overline{CAS}$		Bank‡				L†	L	8	7	6	5	4	3	2	1	0
	16	$\overline{RAS}$		24	23	22	21	20	19	18	17	16	15	14	13	12	11	10
		$\overline{CAS}$		Bank‡				L†	L	9	8	7	6	5	4	3	2	1
	32	$\overline{RAS}$		25	24	23	22	21	20	19	18	17	16	15	14	13	12	11
		$\overline{CAS}$		Bank‡				L†	L	10	9	8	7	6	5	4	3	2
10	8	$\overline{RAS}$		24	23	22	21	20	19	18	17	16	15	14	13	12	11	10
		$\overline{CAS}$		Bank‡				L†	9	8	7	6	5	4	3	2	1	0
	16	$\overline{RAS}$		25	24	23	22	21	20	19	18	17	16	15	14	13	12	11
		$\overline{CAS}$		Bank‡				L†	10	9	8	7	6	5	4	3	2	1
	32	$\overline{RAS}$		26	25	24	23	22	21	20	19	18	17	16	15	14	13	12
		$\overline{CAS}$		Bank‡				L†	11	10	9	8	7	6	5	4	3	2

Legend: Bit is internally latched during an ACTV command.
Reserved for future use. Undefined.
Bit may not be driven. The number of address bits driven during a $\overline{RAS}$ cycle is equal to the number of (row bits + bank-select bits).

† L = Low; EA12 is driven low during READ or WRT commands to disable autoprecharge.
‡ During CAS cycle for READ or WRT command, only the bank select address bits (1 or 2 bits, controlled by SDBSZ) are driven to valid values. The address bit(s) used are determined by the number of row address bits and number of bank address bits.

[5] The RAS and CAS values indicate the bit of the byte address present on the corresponding EA pin during a RAS or CAS cycle.

[6] The RAS and CAS values indicate the bit of the byte address present on the corresponding EA pin during a RAS or CAS cycle.

Table 21. C64x Byte Address to EA Mapping for SDRAM RAS and CAS[7]

No. of Column Address Bits	Interface Bus Width	DRAM Cmd																				
			EMIFB																			
			EA 20	EA 19	EA 18	EA 17‡	EA 16	EA 15	EA 14	EA 13	EA 12	EA 11	EA 10	EA 9	EA 8	EA 7	EA 6	EA 5	EA 4	EA 3	EA 2	EA 1
			EMIFA																			
			EA 22	EA 21	EA 20	EA 19‡	EA 18	EA 17	EA 16	EA 15	EA 14	EA 13	EA 12	EA 11	EA 10	EA 9	EA 8	EA 7	EA 6	EA 5	EA 4	EA 3
			A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12	A 11	A 10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
8	8	$\overline{RAS}$	L	L	L	H/L	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
		$\overline{CAS}$	L	L	L	H/L	23	22	21	20	19	L†	L	L	7	6	5	4	3	2	1	0
	16	$\overline{RAS}$	L	L	L	H/L	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
		$\overline{CAS}$	L	L	L	H/L	24	23	22	21	20	L†	L	L	8	7	6	5	4	3	2	1
	32	$\overline{RAS}$	L	L	L	H/L	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10
		$\overline{CAS}$	L	L	L	H/L	25	24	23	22	21	L†	L	L	9	8	7	6	5	4	3	2
	64	$\overline{RAS}$	L	L	L	H/L	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11
		$\overline{CAS}$	L	L	L	H/L	26	25	24	23	22	L†	L	L	10	9	8	7	6	5	4	3
9	8	$\overline{RAS}$	L	L	L	H/L	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
		$\overline{CAS}$	L	L	L	H/L	24	23	22	21	20	L†	L	8	7	6	5	4	3	2	1	0
	16	$\overline{RAS}$	L	L	L	H/L	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10
		$\overline{CAS}$	L	L	L	H/L	25	24	23	22	21	L†	L	9	8	7	6	5	4	3	2	1
	32	$\overline{RAS}$	L	L	L	H/L	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11
		$\overline{CAS}$	L	L	L	H/L	26	25	24	23	22	L†	L	10	9	8	7	6	5	4	3	2
	64	$\overline{RAS}$	L	L	L	H/L	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12
		$\overline{CAS}$	L	L	L	H/L	27	26	25	24	23	L†	L	11	10	9	8	7	6	5	4	3
10	8	$\overline{RAS}$	L	L	L	H/L	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10
		$\overline{CAS}$	L	L	L	H/L	25	24	23	22	21	L†	9	8	7	6	5	4	3	2	1	0
	16	$\overline{RAS}$	L	L	L	H/L	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11
		$\overline{CAS}$	L	L	L	H/L	26	25	24	23	22	L†	10	9	8	7	6	5	4	3	2	1
	32	$\overline{RAS}$	L	L	L	H/L	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12
		$\overline{CAS}$	L	L	L	H/L	27	26	25	24	23	L†	11	10	9	8	7	6	5	4	3	2
	64	$\overline{RAS}$	L	L	L	H/L	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13
		$\overline{CAS}$	L	L	L	H/L	28	27	26	25	24	L†	12	11	10	9	8	7	6	5	4	3

Legend: Bit is internally latched during an ACTV command.

† L = Low; logical address A10 is driven low during READ or WRT commands to disable autoprecharge.

‡ EA19 (EMIFA) and EA17 (EMIFB) are used during ACTV to indicate non-PDT vs. PDT access. For non-PDT access, this bit is 1. For PDT access, this bit is 0 during ACTV.

[7] The RAS and CAS values indicate the bit of the byte address present on the corresponding EA pin during a RAS or CAS cycle.

3.5 Timing Constraints

This section discusses the timing constraints used to determine if an SDRAM can operate with the C6000 at a given clock frequency. The methods discussed have provide a rough, error prone, estimate of the time margin present in a given system. The recommended method of performing AC timing analysis is to use I/O buffer specification (IBIS) models. To properly use IBIS models to attain accurate timing analysis for a given system, see Using IBIS Models for Timing Analysis (SPRA839).

For the following constraint calculations, a time t_{margin} is calculated representing the margin in the system after taking into account the worst-case numbers from the memory and the C6000 data sheets.

After calculating the time t_{margin}, it is a system-level issue to determine if the proper amount of margin has been met. The required timing margin is extremely system dependent, depending primarily on trace length and loading, but other factors can come into play. Therefore, this parameter should be determined for the particular system in question.

In the following discussion, *m* is used to denote the memory specifications. No additional designators are used to denote the C6000 DSP timing specifications.

3.5.1 C6000 Outputs (ED, EA, CE, BE, SDCAS, SDRAS, SDWE)

3.5.1.1 C620x/C670x Output Comparison

For simplicity, the C620x/C670x data sheets specify the outputs as a setup time (t_{osu}) to the next rising edge and a hold time (t_{oh}) from the previous rising edge. Thus, the comparison between C6000 specifications and memory specifications is extremely straightfoR/Ward. This also allows the user to be unconcerned with which clock edge triggers output data.

Use the following equations derived from Figure 41 to calculate the timing margin between the C6000 and the desired SDRAM.

- setup time: output setup time (t_{osu}) from inactive to active must provide an ample setup time ($t_{isu(m)}$) for the input. Therefore, the margin available is:
  - $t_{margin} = t_{osu} – t_{isu(m)}$
- Hold time: output hold time (t_{oh}) from active to inactive must be greater than the hold time required by the input ($t_{ih(m)}$). The margin is then:
  - $t_{margin} = t_{oh} – t_{ih(m)}$

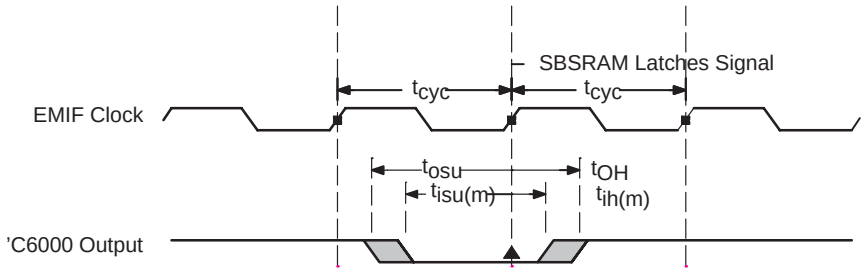


Figure 41. Outputs From C620x/C670x (Write Data [ED], Control, and Address Signals)

3.5.1.2 C621x/C671x/C64x Output Comparison

The C621x/C671x, and C64x data sheets specify the outputs as a minimum delay and a maximum delay from the rising edge of ECLKOUT[8]. When comparing these parameters against the specification for a particular SDRAM, the maximum delay (t_{dmax}) is used to verify that the input setup time ($t_{is(m)}$) of the memory is met. The minimum delay (t_{dmin}) is used to verify that the input hold time ($t_{ih(m)}$) of the memory is met.

Use the following equations derived from Figure 42 to calculate the timing margin between the C621x/C671x/C64x and the desired SDRAM.

- Setup time: the maximum delay (t_{dmax}) from clock to output signal valid must provide an ample setup time ($t_{isu(m)}$) for the input. Therefore, the margin available is:
  - $t_{margin} = t_{cyc} – (t_{dmax} + t_{isu(m)})$
- Hold time: the minimum delay (t_{dmin}) from clock to output signal invalid must be greater than the hold time required by the input ($t_{ih(m)}$). The margin is then:
  - $t_{margin} = t_{dmin} – t_{ih(m)}$

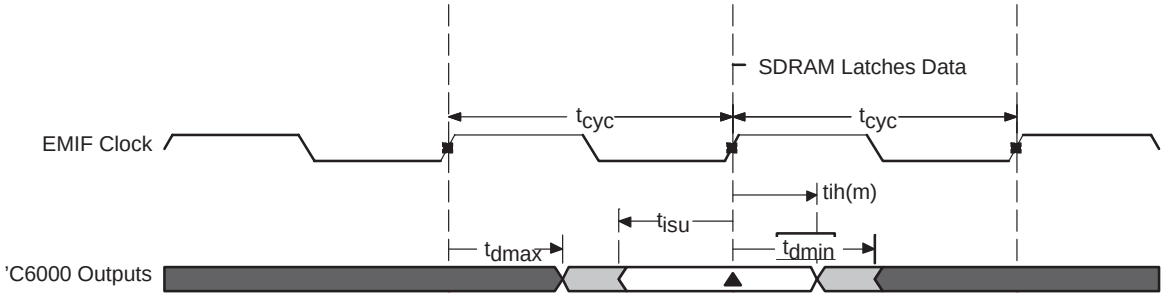


Figure 42. Outputs From C621x/C671x/C64x (Write Data [ED], Control, and Address Signals)

3.5.2 C6000 Inputs (Output Data From the SDRAM, Read ED)

Figure 43 shows the output data from the SDRAM as it occurs during a read cycle. The situation is similar to the outputs from the C6000 except that the SDRAM must provide an ample setup and input hold to the C6000.

The constraints can be expressed as follows:

- Setup times: the access time ($t_{acc(m)}$) of the SDRAM must provide a large enough input setup time (t_{su}) for the input to the C6000.
  - $t_{margin} = t_{cyc} – (t_{acc(m)} + t_{su})$
- Hold times: the output hold time ($t_{oh(m)}$) for data output from the SDRAM must provide a hold time greater than the hold time required by the input (t_{ih}) of the C6000.
  - $t_{margin} = t_{oh(m)} – t_{ih}$

[8] For C64x, ECLKOUT referenced in this section is equivalent to ECLKOUT1.

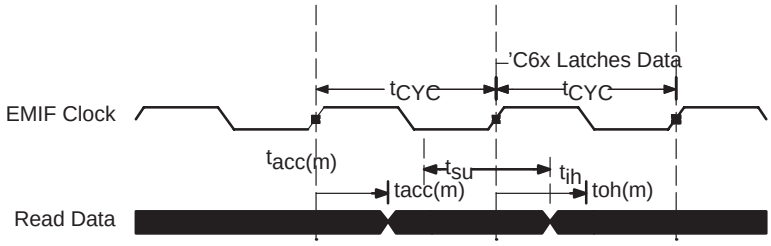


Figure 43. Input to C6000 (Read Data)

3.5.3 Timing Comparisons for Four SDRAMs

This section summarizes the comparisons listed above for four different SDRAMs with four different C6000 devices. Although not every C6000 device is shown in the following examples, the approach is the same for all of the current C6000 devices.

For the following examples, notice that more margin is achieved with a faster memory. For example, if a 100-MHz interface is desired, a 125-MHz SDRAM will provide more margin than a 100-MHz SDRAM. Although the C6000 DSPs are designed to operate with SDRAMs at the rated speeds, sometimes the extra margin may be worth the extra cost of faster memories. SDRAM data sheets should be compared to the C6000 data sheet to verify operation with the desired margins.

3.5.3.1 C6202/C6203/C6204/C6205 vs. Micron's MT48LC4M16A2-8 at 125 MHz

The MT48LC4M16A2-8 is a 64M-bit x 16-bit device. For the C6202/C6203/C6204/C6205 interface, two of these devices are used in parallel, resulting in an addressable space of 4M bytes.

This example uses the C6202/C6203/C6204/C6205-250 running at its maximum clock speed of 250 MHz (P = 4 ns). Because the C6202/C6203/C6204/C6205 EMIF uses CLKOUT2 (which is 1/2x the CPU speed) for synchronous memory interfaces, T_{cyc} = 8 ns.

The timing parameters of the MT48LC4M16A2-8 and the C6202/C6203/C6204/C6205-250 can be summarized as shown in Table 22:

Table 22. MT48LC4M16A2-8 and C6202/C6203/C6204/C6205-250 Timing Parameters

C6202/C6203/C6204/C6205-250 @ P = 4 ns		MT48LC1M16A1-8		T_{margin}
Outputs	T_{osu} = P – 1.5 = 2.5 ns	Inputs	T_{isu} (m) = 2 ns	T_{osu} – Tisu (m) = 0.5 ns a
	T_{oh} = P – 2.8 = 1.2 ns		T_{ih} (m) = 1 ns	T_{oh} – T_{ih} (m) = 0.2 nsa
Inputs	T_{isu} = 1.2	Outputs	T_{acc} (m) = 6 ns	T_{cyc} – T_{acc} (m) – tisu = 0.8 nsa
	T_{ih} = 2.7		T_{oh} (m) = 2.5 ns	T_{oh} – T_{ih} (m) = −0.2 ns r

3.5.3.2 C6414 vs. Micron's MT48LC32M8A2-7 at 133 MHz

The MT48LC32M8A2-7 is a 256M-bit x 8-bit device, which results in an addressable space of 128M bytes.

This example uses the C6414-500 running at its maximum clock speed of 500 MHz (P = 2 ns). Because the CPU speed is independent of the EMIF clock speed, we use an externally provided clock of 133 MHz for the synchronous memory interface, resulting in T_{cyc} = 7.5 ns. The latency is programmed to 3.

The timing parameters of the MT48LC16M8A2-8 and the C6414-500 can be summarized as shown in Table 23:

Table 23. MT48LC16M8A2-8 and C6414-500 Timing Parameters

C6414-500		MT48LC32M8A2-7		T_{margin}
Outputs	T_{dmax} = 6.4 ns	Inputs	T_{isu} (m) = 1.5 ns	$T_{cyc} - T_{dmax} - T_{isu}$ (m) = 1.0 ns [a]
	T_{dmin} = 1.3 ns		T_{ih} (m) = 0.8 ns	$T_{dmin} - T_{ih}$ (m) = 0.2 ns[a]
Inputs	T_{isu} = 2.1	Outputs	T_{acc} (m) = 5.4 ns	$T_{cyc} - T_{acc}$ (m) – t_{isu} = 0.1 ns[a]
	T_{ih} = 2.5		T_{oh} (m) = 3.0 ns	$T_{oh} - T_{ih}$ (m) = 1.5 ns[a]

4 Complete Example Using C6201B and Micron's MT48LC4M16A2-10

This section walks through the register configuration for interfacing the C6201B with Micron's MT48LC4M16A2-10, which is 512K x 16-bit x 4-bank SDRAM capable of operating at 100 MHz. If additional timing margin is needed, this device is available at 125 MHz and provides additional timing margin. Because the memory is 16 bits wide, we use two devices in parallel to complete the 32-bit word, giving a total addressable space of 16M bytes. The block diagram for the interface schematic is identical to that shown in Figure 3.

Assumptions:

- CLKOUT1 frequency of 200 MHz
- 100-MHz SDRAM clock frequency.
  (SDCLK = CLKOUT2 = ½ x CLKOUT1 frequency)
- T_{cyc} = 10 ns
- SDRAM to be located at CE2 (logical address 0x02000000)
- Driven by SDCLK
- SSCLK and CLKOUT1 used by other memory in system
- CLKOUT2 is not in use in the system.

4.1 Register Configuration for C6201B to MT48LC4M16A2

Table 24 shows the registers and bitfields that are configured to control the C6201B to MT48LC4M16A2 SDRAM interface.

Table 24. SDRAM Registers

Register Name	Fields Required
EMIF global control	SDCEN, CLK2EN, SSCEN, CLK1EN
EMIF CE2 space control	MTYPE
EMIF SDRAM control	TRC, TRP, TRCD, INIT, RFEN, SDWID
EMIF SDRAM timing	PERIOD

4.1.1 EMIF Global Control Registers for C6201B to MT48LC4M16A2

Because the MT48LC4M16A2-10 SDRAM is driven by SDCLK, we must then set the following, as shown in Figure 44:

31 14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	rsv	$\overline{\text{ARDY}}$	$\overline{\text{HOLD}}$	$\overline{\text{HOLDA}}$	NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
0	1 1	0	0	1	1	0	1	1	1	0	0	0	1

NOTE: SDCEN = 1 indicates that SDCLK is enabled to clock because we assume it is driving the SDRAM interface. SSCEN = 1 indicates that SSCLK is enabled because we assume it is in use by the system.
CLK1EN = 1 indicates that SSCLK is enabled because we assume it is in use by the system.
CLK2EN = 0 indicates that CLKOUT2 is disabled because we assume it is NOT in use by the system.

Figure 44. EMIF Global Control Register Diagram for C6201B to MT48LC4M16A2

Thus, a valid setting for the EMIF global control register is 0x00003371.

For additional information on the remainder of the fields, see the *TMS320C6000 Peripherals Reference Guide*.

4.1.2 EMIF CE2 Space Control Register for C6201B to MT48LC4M16A2

As shown in Figure 45, MTYPE = 011 indicates that 32-bit-wide SDRAM is located in the CE2 address space. The rest of the fields are irrelevant because they refer to asynchronous memory and SDRAM is configured for this space. A valid setting for EMIF CE2 space control is 0xFFFFFF33.

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
1111	111111	11	1111

15 14	13 8	7	6 4	3 2	1 0
rsv	READ STROBE	Rsv	MTYPE	Reserved	READ HOLD
11	111111	0	011	00	11

Figure 45. EMIF CE2 Space Control Register Diagram for C6201B to MT48LC4M16A2

4.1.3 EMIF SDRAM Control Register for C6201B to MT48LC4M16A2

For the SDRAM control register (Figure 46), values must actually be calculated based on the clock frequency used (100 MHz for this example, t_{CYC} = 10ns) and the parameters of the SDRAM used. Table 25 summarizes the values.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					SDWID	RFEN	INIT	TRCD				TRP			
00000					1	1	1	0001				0001			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRC				Reserved											
0110				000000000000											

NOTE: SDWID = 1 indicates that 16 bit wide SDRAM is used.
RFEN = 1 indicates that SDRAM refresh is enabled.
INIT = 1 forces initialization of the SDRAM.
TRCD = 0010b from previous calculation.
TRP = 0010b from previous calculation.
TRC = 1000b from previous calculation

Figure 46. EMIF SDRAM Control Register for C6201B to MT48LC4M16A2

Table 24 shows the registers and bitfields that are configured to control the C6201B to MT48LC4M16A2 SDRAM interface.

Table 25. Timing Parameter Calculation for SDRAM Control Register for C6201B to MT48LC4M16A2

Field Name	Formula	Value from Micron Data Sheet	Value Calculated for Field	Value Recommended
TRC	TRC = $(t_{RC} / t_{CYC}) - 1$	t_{RC} = 70 ns (min)	TRC = 6	6
TRP	TRP = $(t_{RP} / t_{CYC}) - 1$	t_{RP} = 20 ns (min)	TRP = 1	1
TRCD	TRCD = $(t_{RCD} / t_{CYC}) - 1$	t_{RCD} = 20 ns (min)	TRCD = 1	1

Based on the above calculations, a value of 0x07228000 should be written to the EMIF SDRAM control register.

4.1.4 EMIF SDRAM Refresh Period for C6201B to MT48LC4M16A2

Based on this result (see Figure 47 and Table 26), a value of 0x61A should be written to the refresh period field in the EMIF SDRAM timing register.

Figure 47. EMIF SDRAM Refresh Period for C6201B to MT48LC4M16A2

31 24	23 12	11 0
Reserved	COUNTER	PERIOD
00000000	0000 0000 0000	0110 0001 1010 (0x61A)
R−0	R−0000 0100 0000	R/W−0000 0100 0000

NOTE: Period = 0x61A from previous calculation.

Table 26. Period Calculation for SDRAM Refresh Period for C6201B to MT48LC4M16A2

Field Name	Formula	Value From TMS626812B Data Sheet	Value Calculated for Field
PERIOD	PERIOD = $t_{Refresh}/t_{CYC}$	$t_{Refresh}$ = 64 ms / 4096 = 15.625μS	Period = 1562cycles = 0x61A cycles

5 Complete Example Using C6211 and Micron's MT48LC16M8A2-8

This section walks through the register configuration for interfacing the C6211 with Micron's MT48LC16M8A2-8, which is a 4-M x 8-bit x 4-bank SDRAM capable of operating at 125 MHz. Because the memory is 8 bits wide, we use four devices in parallel to complete the 32-bit word, for a total addressable space of 64M bytes. The block diagram for the interface schematic is identical to that shown in Figure 2, except that ECLKOUT is used as the memory clock, and EA12 is used instead of SDA10.

This 125-MHz SDRAM is featured because it offers additional timing margin compared to typical 100-MHz SDRAMs and can be used in a system that requires extra margin.

Assumptions:

- 100-MHz SDRAM clock frequency.
  (ECLKIN = ECLKOUT = 100 MHz).
- T_{cyc} = 10 ns
- SDRAM to be located at CE3 (logical address 0xB0000000)
- CLKOUT1 and CLKOUT2 not in use by the system

5.1 Register Configuration for C6211 to MT48LC16M8A2

Table 27 shows the registers and bitfields that are configured to control the C6211 to MT48LC16M8A2 SDRAM interface.

Table 27. SDRAM Registers for C6211 to MT48LC16M8A2

Register Name	Fields Required
EMIF global control	CLK1EN, CLK2EN
EMIF CE3 space control	MTYPE
EMIF SDRAM control	TRC, TRP, TRCD, INIT, RFEN, SDCSZ, SDRSZ, SDBSZ
EMIF SDRAM timing	PERIOD
EMIF SDRAM extension	

5.1.1 EMIF Global Control Registers for C6211 to MT48LC16M8A2

Because none of the programmable clocks are in use in the system, we must set the following, as shown in Figure 48:

31 14	13 12	11	10	9	8	7	6 5	4	3	2 1 0
Reserved	Reserved	BUS REQ	$\overline{\text{ARDY}}$	$\overline{\text{HOLD}}$	$\overline{\text{HOLDA}}$	NOHOLD	Reserved	CLK1EN	CLK2EN	Reserved
0	1 1	0	0	1	1	0	0 0	0	0	0 0 0

NOTE: CLK1EN = 1 indicates that SSCLK is enabled because we assume it is in use by the system.
CLK2EN = 0 indicates that CLKOUT2 is disabled because we assume it is NOT in use by the system.

Figure 48. EMIF Global Control Register Diagram for C6211 to MT48LC16M8A2

Thus, a valid setting for the EMIF global control register is 0x00003300.

For additional information on the remainder of the fields, see the *TMS320C6000 Peripherals Reference Guide* (SPRU190).

5.1.2 EMIF CE3 Space Control Register for C6211 to MT48LC16M8A2

As shown in Figure 49, MTYPE = 011 indicates that 32-bit-wide SDRAM is located in the CE3 address space. The rest of the fields are irrelevant because they refer to asynchronous memory, and SDRAM is configured for this space. A valid setting for EMIF CE3 space control is 0xFFFFFF33.

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
1111	111111	11	1111

15 14	13 8	7 6 4	3 2	1 0
TA	READ STROBE	MTYPE	Reserved	READ HOLD
11	111111	0011	00	11

NOTE: MTYPE = 0011 indicates that a 32-bit-wide SDRAM is located in the CE3 address space. The rest of the fields are irrelevant because they refer to asynchronous memory, and SDRAM is configured for this space.

Figure 49. EMIF CE3 Space Control Register Diagram for C6211 to MT48LC16M8A2

A valid setting for EMIF CE3 space control is 0xFFFFFF33.

5.1.3 EMIF SDRAM Control Register for C6211 to MT48LC16M8A2

For the SDRAM control register (Figure 50), values must actually be calculated based on the clock frequency used (100 MHz for this example, t_{CYC} = 10 ns) and the parameters of the SDRAM used. Table 28 summarizes the values.

31	30	29 28	27 26	25	24	23 20	19 16
rsv	SDBSZ	SDRSZ	SDCSZ	RFEN	INIT	TRCD	TRP
0	1	01	10	1	1	0001	0001

15 12	11 0
TRC	Reserved
0110	000000000000

NOTE: SDCSZ = 10b indicates that 10d column address bits are used.
SDRSZ = 01b indicates that 12d row address bits are used.
SDBSZ = 1 indicates that two bank address bits are used (4 banks).
RFEN = 1 indicates that SDRAM refresh is enabled.
INIT = 1 forces initialization of the SDRAM.
TRCD = 0001b from previous calculation.
TRP = 0001b from previous calculation.
TRC = 0110b from previous calculation.

Figure 50. EMIF SDRAM Control Register for C6211 to MT48LC16M8A2

Table 28. Timing Parameter Calculation for SDRAM Control Register for C6211 to MT48LC16M8A2

Field Name	Formula	Value From KM416S4030 Data Sheet	Value Calculated for Field	Value Recommended
TRC	TRC = $(t_{RC} / t_{CYC}) - 1$	t_{RC} = 70 ns (min)	TRC = 6	6
TRP	TRP = $(t_{RP} / t_{CYC}) - 1$	t_{RP} = 20 ns (min)	TRP = 1	1
TRCD	TRCD = $(t_{RCD} / t_{CYC}) - 1$	t_{RCD} = 20 ns (min)	TRCD = 1	1

Based on the above calculations, a value of 0x5B116000 should be written to the EMIF SDRAM control register.

5.1.4 EMIF SDRAM Refresh Period for C6211 to MT48LC16M8A2

Based on this result, a value of 0x61A should be written to the refresh period field in the EMIF SDRAM timing register. See Figure 51 and Table 29.

31 24	23 12	11 0
Reserved	COUNTER	PERIOD
00000000	000000000000	11000011010 (0x61A)

NOTE: Period = 0x61A from previous calculation.

Figure 51. EMIF SDRAM Refresh Period for C6211 to MT48LC16M8A2

Table 29. Period Calculation for SDRAM Refresh Period for C6211 to MT48LC16M8A2

Field Name	Formula	Value From Micron Data Sheet	Value Calculated for Field
PERIOD	PERIOD = $t_{Refresh}/t_{CYC}$	$t_{Refresh}$ = 64 ms / 4096 = 15.625µS	Period = 1562cycles = 0x61A cycles

5.1.5 EMIF SDRAM Extension Register for C6211 to MT48LC16M8A2

For the SDRAM extension register, values must be calculated based on the clock frequency used (100 MHz for this example, t_{CYC} = 10ns) and the parameters of the SDRAM used. Table 30 summarizes the values.

Table 30. SDRAM Extension Register Values for C6211 to MT48LC16M8A2

Field Name	Formula	Value From SDRAM Data Sheet	Value Calculated for Field	Value Recommended
TCL	TCL = (t_{CL}) – 2	t_{CL} = 3 cycles	TCL = 1	TCL = 1
TRAS	TRAS = (t_{RAS} / t_{CYC}) – 1	t_{RAS} = 50 ns	TRAS = 4	TRAS = 4
TRRD	TRRD = (t_{RRD} / t_{CYC}) – 2	t_{RRD} = 20	TRRD = 0	TRRD = 0
TWR	TWR = (t_{WR} / t_{CYC}) – 1	t_{WR} = 15 ns	TWR = 1.5	TWR = 2
THZP	THZP = (t_{HZP}) – 1	t_{HZP} = 3 cycles	THZP = 2	THZP = 2
RD2RD	Recommended value from			RD2RD = 0
RD2DEAC				RD2DEAC = 1
RD2WR				RD2WR = 4
R2WDQM				R2WDQM = 2
WR2WR				WR2WR = 0
WR2DEAC				WR2DEAC = 1
WR2RD				WR2RD = 0

6 Complete Examples Using C6414 and Micron's MT48LC4M32B2-7

This section first walks through the register configuration for interfacing the C6414 with Micron's MT48LC4M32B2-7, which is a 1-M x 32-bit x 4-bank SDRAM capable of operating at speeds up to 143 MHz. Because the memory is 32 bits wide, we use two devices in parallel to complete the 64-bit doubleword. The block diagram for the interface schematic is very similar to that of Figure 3, except with the previously noticed differences in the C64x EMIFA interface.

The interface will use the full speed of the CPU and an interface speed of 133 MHz, the maximum current speed of the EMIF interface. This 143 MHz DRAM is featured because it offers additional timing margin compared to typical slower SDRAMs.

Assumptions:

- 133 MHz SDRAM clock frequency (ECLKIN = ECLKOUT1 = 133 MHz)
- T_{cyc} = 7.5 ns
- SDRAM to be located at EMIFA CE2 (logical address 0xA0000000)
- ECLKOUT2 not in use by the system (EK2EN = 0)

6.1 Register Configuration for C6414 to MT48LC4M32B2

Table 31 shows the registers and bitfields that are configured to control the C6414 to MT48LC4M32B2 SDRAM interface.

Table 31. SDRAM Registers for C6414

Register Name	Fields Required
EMIF global control	EK1EN, EK2EN, EK2RATE
EMIF CE3 space control	MTYPE
EMIF SDRAM control	TRC, TRP, TRCD, INIT, RFEN, SDCSZ, SDRSZ, SDBSZ
EMIF SDRAM timing	PERIOD
EMIF SDRAM extension	

6.1.1 EMIF Global Control Register for C6414 to MT48LC4M32B2

Because ECLKOUT1 is in use by the system and driven by ECLKIN, we must set the following, as shown in Figure 52. Table 32 summarizes the values.

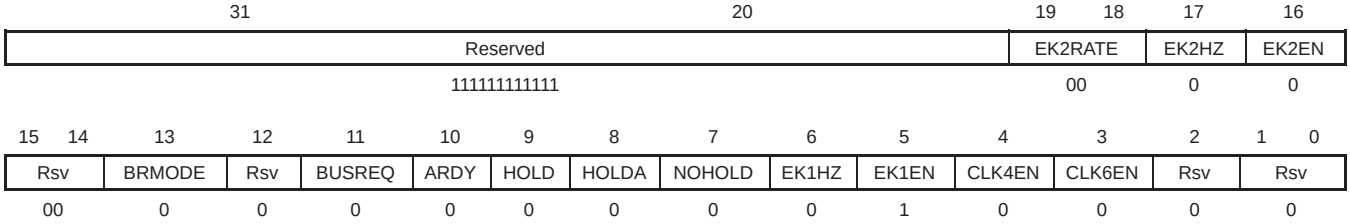


Figure 52. EMIF Global Control Register Diagram for C6414 MT48LC4M32B2

Table 32. Global Control Register for C6414

Formula	Description
EK1EN = 1	Indicates that ECLKOUT1 is enabled to clock and used to clock the SBSRAM.
EK2EN = 0	Indicates that ECLKOUT2 is disabled and not in use by the system.
EK2RATE = 00	Indicates that ECLKOUT2 would be 1x the EMIF input clock if it was enabled by the system

Thus, a valid setting for the EMIF global control register is 0x00000010.

For additional information on the remainder of the fields, see the TI *TMS320C6000 Peripherals Reference Guide*.

6.1.2 EMIF CE3 Space Control Register for C6414 to MT48LC4M32B2

MTYPE = 1101, as shown in Figure 53, indicates that 32-bit-wide SDRAM is located in the CE2 address space. The other fields are irrelevant because they refer to asynchronous memory. The additional settings for the SDRAM can be found in the CE2 space secondary control register.

A valid setting for EMIF CE2 Space Control is 0xFFFFFF33.

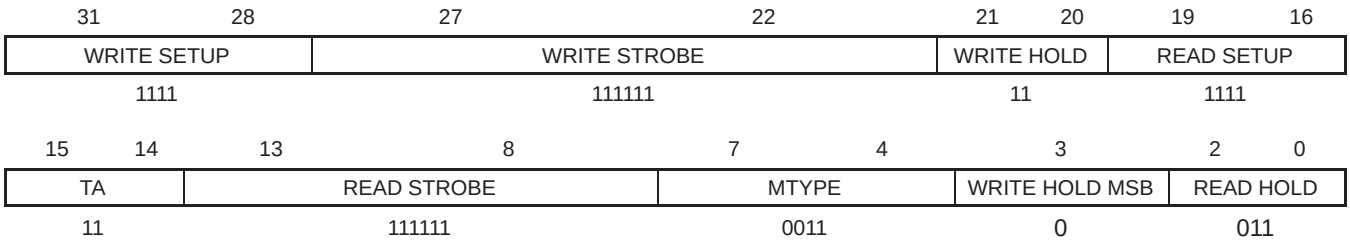


Figure 53. EMIF CE2 Space Control Register Diagram

6.1.3 EMIF SDRAM Control Register for C6414 to MT48LC4M32B2

For the SDRAM control register (Figure 54), values must actually be calculated based on the clock frequency used (133 MHz for this example, t_{CYC} = 7.5 ns) and the parameters of the SDRAM used. Table 33 summarizes the values.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
rsv	SDBSZ	SDRSZ		SDCSZ		RFEN	INIT	TRCD				TRP			
0	1	01		01		1	1	0001				0001			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRC				Reserved											SLFRFR
1001				00000000000											0

NOTE: SDCSZ = 01b indicates that 10d column address bits are used.
SDRSZ = 01b indicates that 12d row address bits are used.
SDBSZ = 1 indicates that two bank address bits are used (4 banks).
RFEN = 1 indicates that SDRAM refresh is enabled.
INIT = 1 forces initialization of the SDRAM.
TRCD = 0001b from previous calculation.
TRP = 0001b from previous calculation.
TRC = 1001b from previous calculation.
SLFRFR = 0 indicates that self-refresh mode is not enabled

Figure 54. EMIF SDRAM Control Register for C6414 to MT48LC4M32B2

Table 33. Timing Parameter Calculation for SDRAM Control Register for C6414 to MT48LC4M32B2

Field Name	Formula	Value From Data Sheet	Value Calculated for Field	Value Recommended
t_{RC}	$t_{RC} = (t_{RC} / t_{CYC}) - 1$	t_{RC} = 70 ns (min)	t_{RC} = 8.33	9
t_{RP}	$t_{RP} = (t_{RP} / t_{CYC}) - 1$	t_{RP} = 20 ns (min)	t_{RP} = 1.66	2
t_{RCD}	$t_{RCD} = (t_{RCD} / t_{CYC}) - 1$	t_{RCD} = 20 ns (min)	t_{RCD} = 1.66	2

Based on the above calculations, a value of 0x57119000 should be written to the EMIF SDRAM control register.

6.1.4 EMIF SDRAM Refresh Period for C6414 to MT48LC4M32B2

Based on this result (Figure 55), a value of 0x446 should be written to the refresh period field in the EMIF SDRAM timing register (see Table 34).

31 24	23 12	11 0
Reserved	COUNTER	PERIOD
00000000	000000000000	010001000110(0x446)

NOTE: Period = 0x446 from previous calculation.

Figure 55. EMIF SDRAM Refresh Period for C6414 to MT48LC4M32B2

Table 34. Period Calculation for SDRAM Refresh Period for C6414 to MT48LC16M8A2

Field Name	Formula	Value From Micron Data Sheet	Value Calculated for Field
PERIOD	PERIOD = $t_{Refresh}/t_{CYC}$	$t_{Refresh}$ = 64 ms / 4096 = 15.625µS	Period = 2084 cycles = 824 cycles

6.1.5 EMIF SDRAM Extension Register for C6414 to MT48LC4M32B2

For the SDRAM extension register, values must be calculated based on the clock frequency used (133 MHz for this example, t_{CYC} = 7ns) and the parameters of the SDRAM used. Table 35 summarizes the values.

Table 35. SDRAM Extension Register Values for C6414 to MT48LC4M32B2

Field Name	Formula	Value From SDRAM Data Sheet	Value Calculated for Field	Value Recommended
TCL	TCL = (t_{CL}) – 2	t_{CL} = 3 cycles	TCL = 1	TCL = 1
TRAS	TRAS = (t_{RAS} / t_{CYC}) – 1	t_{RAS} = 42 ns	TRAS = 5	TRAS = 5
TRRD	TRRD = (t_{RRD} / t_{CYC}) – 2	t_{RRD} = 14	TRRD = 0	TRRD = 0
TWR	TWR = (t_{WR} / t_{CYC}) – 1	t_{WR} = 14 ns	TWR = 1	TWR = 1
THZP†	THZP = (t_{HZP}) – 1	t_{HZP} = 3 cycles	THZP = 2	THZP = 2
RD2RD	Recommended value from			RD2RD = 0
RD2DEAC				RD2DEAC = 1
RD2WR				RD2WR = 4
R2WDQM				R2WDQM = 2
WR2WR				WR2WR = 0
WR2DEAC				WR2DEAC = 1
WR2RD				WR2RD = 0

† t_{HZP} is also known as T_{ROH}

7 References

1. *TMS320C6000 Peripherals Reference Guide* (SPRU190).
2. *TMS320C6x Peripheral Support Library Programmers Reference* (SPRU273).
3. *TMS320C6201 Digital Signal Processor* (SPRS051).
4. *TMS320C6202 Fixed-Point Digital Signal Processor* (SPRS072).
5. *TMS320C6211, TMS320C6211B DSPs* (SPRS073).
6. *TMS320C6701 Floating-Point DSP* (SPRS067)
7. *TMS320C6711, TMS320C6711B Floating-Point DSPs* (SPRS088).
8. *MT48LC4M16A2 Data Sheet*, Micron Technology, Inc.
9. *MT48LC1M16A1 Data Sheet*, Micron Technology, Inc.
10. *MT48LC16M8A2 Data Sheet*, Micron Technology, Inc.

Appendix A Code Example for C6201B to Micron MT48LC4M16A2-10

The following code segment sets up the EMIF as described above, using the TMS320C6000 Chip Support Library.

```
#include <csl.h>
#include <csl_emif.h>

void set_EMIF();

void main()
{
         /* initialize the CSL library */
         CSL_init();

         set_EMIF();
}

void set_EMIF()
{
      //Set value of global control register
      Uint32 global = EMIF_GBLCTL_RMK(
            EMIF_GBLCTL_NOHOLD_OF(0),
            EMIF_GBLCTL_SDCEN_ENABLE,
            EMIF_GBLCTL_SSCEN_ENABLE,
            EMIF_GBLCTL_CLK1EN_ENABLE,
            EMIF_GBLCTL_CLK2EN_DISABLE,
            EMIF_GBLCTL_SSCRT_OF(0),
            EMIF_GBLCTL_RBTR8_HPRI );

      //Set value of CE2 control register
      //  Field of interest is: MTYPE field
      //  (other field are set to the default values)
      Uint32 control3 = EMIF_CECTL_RMK(
            EMIF_CECTL_WRSETUP_DEFAULT,
            EMIF_CECTL_WRSTRB_DEFAULT,
            EMIF_CECTL_WRHLD_DEFAULT,
            EMIF_CECTL_RDSETUP_DEFAULT,
            EMIF_CECTL_RDSTRB_DEFAULT,
            EMIF_CECTL_MTYPE_SDRAM32,
            EMIF_CECTL_RDHLD_DEFAULT );

      //Set value of SDRAM control rgister
      //  Fields of interest are: TRC,TRP,TRCD,INIT,RFEN, and SDWID
      Uint32 sdcontrol = EMIF_SDCTL_RMK(
            EMIF_SDCTL_SDWID_DEFAULT,
            EMIF_SDCTL_RFEN_ENABLE,
            EMIF_SDCTL_INIT_YES,
            EMIF_SDCTL_TRCD_OF(1),
            EMIF_SDCTL_TRP_OF(1),
            EMIF_SDCTL_TRC_OF(6) );
```

```
        //Set value of SDRAM timing register with refresh period
        //  Field of interest is:  Period Field
        Uint32 sdtim = EMIF_SDTIM_RMK(
              EMIF_SDTIM_PERIOD_OF(1562) );

        EMIF_configArgs(
              EMIF_GBLCTL_OF(global),             // global control
              EMIF_CECTL_OF(0x00000018),          // 32-bit async mem
              EMIF_CECTL_OF(0x00000018),          // CE1 control
              EMIF_CECTL_OF(0x00000018),          // CE2 control
              EMIF_CECTL_OF(control3),            // CE3 control
              EMIF_SDCTL_OF(sdcontrol),           // SDRAM control
              EMIF_SDTIM_OF(sdtim)                // SDRAM timing
              );
}
```

Appendix B Code Example for C6211 to Micron MT48LC16M8A2-8

The following code segment sets up the EMIF as described above, using the TMS320C6000 Chip Support Library.

```
#include <csl.h>
#include <csl_emif.h>

void set_EMIF();

void main()
{
      /* initialize the CSL library */
      CSL_init();

      set_EMIF();
}
void set_EMIF()
{
      //Set  value of global control register
      Uint32 global = EMIF_GBLCTL_RMK(
            EMIF_GBLCTL_NOHOLD_OF(0),
            EMIF_GBLCTL_CLK1EN_DISABLE,
            EMIF_GBLCTL_CLK2EN_DISABLE );

      //Set value of CE2 control register
      // Field of interest is: MTYPE field
      // (other field are set to the default values)
      Uint32 control3 = EMIF_CECTL_RMK(
            EMIF_CECTL_WRSETUP_DEFAULT,
            EMIF_CECTL_WRSTRB_DEFAULT,
            EMIF_CECTL_WRHLD_DEFAULT,
            EMIF_CECTL_RDSETUP_DEFAULT,
            EMIF_CECTL_TA_DEFAULT,
            EMIF_CECTL_RDSTRB_DEFAULT,
            EMIF_CECTL_MTYPE_SDRAM32,
            EMIF_CECTL_RDHLD_DEFAULT );

      //Set value of SDRAM control rgister
      // Fields of interest are: TRC,TRP,TRCD,INIT,RFEN, and SDWID
      Uint32 sdcontrol = EMIF_SDCTL_RMK(
            EMIF_SDCTL_SDBSZ_4BANKS,
            EMIF_SDCTL_SDRSZ_12ROW,
            EMIF_SDCTL_SDCSZ_10COL,
            EMIF_SDCTL_RFEN_ENABLE,
            EMIF_SDCTL_INIT_YES,
            EMIF_SDCTL_TRCD_OF(1),
            EMIF_SDCTL_TRP_OF(1),
            EMIF_SDCTL_TRC_OF(6) );
```

```
        //Set value of SDRAM timing register with refresh period
        // Field of interest is:  Period Field
        Uint32 sdtim = EMIF_SDTIM_RMK(
              EMIF_SDTIM_XRFR_DEFAULT,
              EMIF_SDTIM_PERIOD_OF(1562) );

        EMIF_configArgs(
              EMIF_GBLCTL_OF(global),             // global control
              EMIF_CECTL_OF(0x00000018),          // 32-bit async mem
              EMIF_CECTL_OF(0x00000018),      // CE1 control
              EMIF_CECTL_OF(0x00000018),          // CE2 control
              EMIF_CECTL_OF(control3),            // CE3 control
              EMIF_SDCTL_OF(sdcontrol),           // SDRAM control
              EMIF_SDTIM_OF(sdtim),               // SDRAM timing
              EMIF_SDEXT_OF(0x00000000)           // SDRAM extension
              );
}
```

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