Application Report
SPRA393 – May 2003

TMS320C6211 to TMS320C6211B Migration Guide

C6000 Hardware Applications

ABSTRACT

This document describes migration from the TMS320C6211 to the TMS320C6211B. The objective of this document is to indicate differences between the two devices and show how handle these differences. Depending on the board layout and any system level timing assumptions, a migration may or may not require any changes. If changes are required, some systems may be able to implement any necessary timing changes through software control, whereas others may require hardware changes.

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1 Introduction

The TMS320C6211B slightly differs from the TMS320C6211. The differences are all timing of signal pins changes. Specifically, the changes are confined to the external memory interface (EMIF) and the host port interface (HPI). All other device parameters are identical between the two devices. Thus, board-level changes may not be necessary to move from the TMS320C6211 to the TMS320C6211B.

To appropriately consider the impact of these timings changes, it is necessary to understand the current interface timings for a given system. A timing analysis of the affected signals should be done to calculate the amount of available margin in the affected interfaces.

Previously implemented workarounds to C6211 errata need not be undone when migrating to C6211B. Revision 3.1 of the C6211B is compatible with all recommended workarounds shown in *TMS320C6211/TMS320C6211B Digital Signal Processors Silicon Errata* (SPRZ154)

2 Asynchronous Memory

Table 1 lists the asynchronous memory timing parameters that changed from C6211 to C6211B. The input hold requirement for data and ARDY increase from 1 ns to 2 ns, and the output hold time for $\overline{\text{AWE}}$ decreased from 1.5 ns to 1.2 ns. If there is not available margin in the current setup to absorb the timing change, the programmable settings can be changed to accommodate the new timing parameters.

Table 1. Asynchronous Memory Timing Changes

No.	Parameter	C6211 Min	C6211B Min	Unit
4	$t_{h(AREH–EDV)}$ Hold time, EDx valid after $\overline{\text{ARE}}$ high	1	2	ns
7	$t_{h(EKOH–ARDY)}$ Hold time, ARDY valid after ECLKOUT high	1	2	ns
10	$t_{d(EKOH–AWEV)}$ Delay time, ECLKOUT high to $\overline{\text{AWE}}$ valid	1.5	1.2	ns

2.1 Table 1, Parameters 4 and 7: For EDx, Input Hold Time is Increased by 1 ns

- If a timing analysis shows there is at least 1ns of extra hold time provided to the C6211, then no change is required for the C6211B.
- If this extra hold time is not available, then the asynchronous read hold period should be extended. This can be adjusted in the appropriate CE Space Control Register (CExCTL). Note that this assumes the memory continues to assert valid data as long as $\overline{\text{OE}}$ remains asserted

2.2 Table 1, Parameter 10: For $\overline{\text{AWE}}$, Output Hold is Reduced by 0.3 ns

- If a timing analysis shows the interface exceeds the memory's write strobe length requirement by 0.3 ns or more, then no change is required.
- If this extra strobe time is not available, then the programmed write strobe length should be extended. This can be adjusted in the appropriate CE Space Control Register (CExCTL). Note that the asynchronous setup time is measured from address/control/data valid to $\overline{\text{AWE}}$ low and is the same for C6211 and C6211B. Therefore, no changes to the programmed write setup time are necessary, despite the change in $\overline{\text{AWE}}$ timing.

2.3 ARDY Performance Improvement

For ARDY input hold time, no change is required. The timing change may alter the cycle which the DSP recognizes the ARDY assertion. If valid data is driven on ED before ARDY is asserted, this timing change will not impact the data sampled by the DSP, but may cause the asynchronous cycle on the C6211B to complete one clock earlier than the C6211.

3 Synchronous-Burst Memory and Synchronous DRAM Memory

Table 2 lists the synchronous-burst memory and Synchronous DRAM timing parameters that changed from C6211 to C6211B. Synchronous-burst and synchronous DRAM memory cycles are not programmable. If the timing analysis shows an extra 1ns of input hold is provided to the DSP and 0.3ns to the memory, then no changes are necessary. If the timing analysis shows the system is not tolerant of the timing changes, then board level changes are necessary to support correct operation. In most SDRAM systems it is unlikely that these will cause an issue because:

On output hold from the DSP (Table 2, parameters 1–5 and 8–12), in typical systems the SBSRAM or SDRAM will require less input hold than the DSP provides.

On input hold from the DSP (Table 2, Parameter 7), in typical systems the output hold from the SBSRAM or SDRAM plus the round trip delay from the DSP's ECLKOUT to return data from the SBSRAM or SDRAM will meet this requirement. In general, as the system is more heavily loaded the easier this requirement is met.

Table 2. Synchronous-Burst Memory and Synchronous DRAM Timing Changes

No.	Parameter	C6211 Min	C6211B Min	Unit
7	$t_{h(EKOH–EDV)}$ Hold time, EDx valid after ECLKOUT high	1	2	ns
1–5, 8–12	$t_{d(EKOH–xxxx)}$ Delay time, ECLKOUT high to signals valid	1.5	1.2	ns

4 Host Port Interface

Table 3 lists the HPI timing parameters that changed from C6211 to C6211B. **These host port timing changes should not impact any systems.** Only the maximum output hold of the C6211B is reduced compared to the C6211. Since output hold timing verification must be calculated from the worst-case (minimum) time, this change does not alter that timing analysis. Also, the delay time changes all represent an improvement when compared to the C6211. Therefore, no changes are required to handle the HPI timing differences.

Table 3. Host Port Interface Timing Changes

No.	Parameter	C6211 Max	C6211B Max	Unit
9	$t_{oh(HSTBH–HDV)}$ Output hold time, HD valid after $\overline{\text{HSTROBE}}$ high	15	12	ns
5	$T_{d(HCS–HRDY)}$ Delay time, $\overline{\text{HSTROBE}}$ to $\overline{\text{HRDY}}$	15	12	ns
6–7, 15–17	$T_{d(HSTBx–xxxx)}$ Delay time, $\overline{\text{HSTROBE}}$ to signals valid	15	12	ns
20	$T_{d(HASL–HRDYH)}$ Delay time, $\overline{\text{HAS}}$ low to $\overline{\text{HRDY}}$ high	15	12	ns

4.1 Cycle Performance Differences

While these timing changes do not impact functionality, it should be noted that HPI cycles may not be identical on the C6211 and C6211B. Performance improvements and bug fixes may cause data to be presented at a different time and different burst lengths to be supported. Both C6211 and C6211B adhere to the same behavioral specification (with the exceptions noted in the silicon errata). Therefore, if the host interface does not depend on cycles appearing a certain way, this change will not adversely impact the interface.

5 Conclusion

When migrating from the TMS320C6211 to the TMS320C6211B, the only changes to consider are timing changes to the EMIF and HPI. With an interface timing analysis for these two ports, the impact of the DSP timing changes can be considered. In the case where no conflicts are created, no changes are necessary to migrate. If the changes cause timing violations, then system software or hardware will need to be altered to address the violation.

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