Application Report
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Compatibility Considerations: Migrating From TMS570LS31x/21x or TMS570LS12x/11x to TMS570LS04x/03x Safety Microcontrollers

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ABSTRACT

This application report provides a summary of the differences between the TMS570LS04x/03x versus the TMS570LS31x/21x and TMS570LA12x/11x series of microcontrollers.

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1 Introduction

The LS04x/03x series incorporates a subset of the functionality incorporated on the LS31x/21x and LS12x/11x series. There are some enhancements implemented on the LS04x/03x similar to the enhancements implemented on the TMS570LS12x/11x series vs the overall superset LS31x/21x series, while still maintaining application code compatibility to the overall superset series when the code is targeted to the subset functionality. An application written for the LS31x/21x or LS12x/11x series runs correctly on the LS04x/03x series as long as only the common functions and features are exercised.

A product overview can be found in the Hercules Product Brochure that outlines content differences between all three series of devices.

2 Memory Configuration Differences

The memory configurations of each of the three series of microcontrollers are different. In each series, the memories are sized according to the targeted applications. Table 1 shows the primary memory spaces within each series of microcontrollers in order to highlight the differences.

Table 1. Memory Configuration Differences

Memory Type	TMS570LS31x/21x	TMS570LS12x/11x	TMS570LS04x/03x
Flash: Program Memory	3MB/2MB	1.25MB/1MB	384kB/256kB
Flash: Boot Sector	1 X 32kB Sector	Up to 2 X 16kB Sectors	Up to 12 X 8kB sectors
Flash: EEPROM Emulation	4 X 16kB Sectors	4 X 16kB Sectors	4 X 4kB Sectors
CPU Data RAM	Up to 256kB	Up to 192kB	32kB
MibADC1 RAM	64 Result Buffers	64 Result Buffers	64 Result Buffers
MibADC2 RAM	64 Result Buffers	64 Result Buffers	N/A
N2HET1 RAM	160 Instruction RAM	160 Instruction RAM	128 Instruction RAM
N2HET RAM	160 Instruction RAM	160 Instruction RAM	N/A
DCAN1 RAM	64 Mailboxes	64 Mailboxes	32 Mailboxes
DCAN2 RAM	64 Mailboxes	64 Mailboxes	16 Mailboxes
DCAN3 RAM	64 Mailboxes	64 Mailboxes	N/A
MibSPI1 RAM	128 Words	128 Words	128 Words
MibSPI3 RAM	128 Words	128 Words	N/A
MibSPI5 RAM	128 Words	128 Words	N/A
FlexRay RAM	8kB Message RAM	8kB Message RAM	N/A

3 Package Compatibility Considerations

Both the LS31x/21x and LS12x/11x series of microcontrollers are supported in either a 337 ball grid array (337 BGA) or a 144-pin quad flat pack (144 QFP) package. The LS04x/03x series of devices is available in a 100-pin quad flat pack (100 QFP) package.

3.1 Pin-Out Compatibility

Given that the LS04x/03x series of microcontrollers is not available in a common package or pinout with the LS31x/21x and LS12x/11x series of microcontrollers, an effort was made to insure there was functional compatibility between the series of devices such that the subset series could be easily adapted into a design that previously had used the super set series. This is accomplished by making each side of the family of devices very similar in order to minimize PCB layout migration issues when going from 144-pin to 100-pin devices. Table 2 demonstrates how the default functional pins of the 100QFP package for the LS04x/03x series map to the subset of default functional pins of the 144QFP on the LS31x/21x and LS12x/11x series of microcontrollers.

Table 2. Functional Pin Compatibility Mapping

LS04x/03x		LS31x/21x and LS12x/11x		Comments
Pin Number	Pin Name/Function	Pin Number	Pin Name/Function	
1	GIOA[0]/INT[0]	2	GIOA[0]/INT[0]	
2	GIOA[1]/INT[1]	5	GIOA[1]/INT[1]	
3	FLTP1	7	FLTP1	
4	FLTP2	8	FLTP2	
5	GIOA[2]/INT[2]	9	GIOA[2]/INT[2]	
6	VCCIO	10	VCCIO	
7	VSS	11	VSS	

Table 2. Functional Pin Compatibility Mapping (continued)

LS04x/03x		LS31x/21x and LS12x/11x		Comments
Pin Number	Pin Name/Function	Pin Number	Pin Name/Function	
8	GIOA[3]/INT[3]	12	CAN3TX	GIOA[3:4]/INT[3:4] are not available in the 144PGE package of the superset devices. CAN3TX and CAN3RX used in GIO mode will allow functional compatibility.
9	GIOA[4]/INT[4]	13	CAN3RX	
10	GIOA[5]/INT[5]	14	GIOA[5]/INT[5]	
11	N2HET[22]	15	N2HET[22]	
12	GIOA[6]/INT[6]	16	GIOA[6]/INT[6]	
13	VCC	17	VCC	
14	OSCIN	18	OSCIN	
15	KELVIN_GND	19	KELVIN_GND	
16	OSCOUT	20	OSCOUT	
17	VSS	21	VSS	
18	GIOA[7]/INT[7]	22	GIOA[7]/INT[7]	
19	N2HET[0]	25	N2HET[0]	
20	VSS	27	VSS	
21	VCC	29	VCC	
22	N2HET[2]	30	N2HET[2]	
23	SPI2nCS[0]	32	MibSPI5nCS[0]	SPI2 is not available in the 144 PGE package for the superset devices. With an offset change and configuration of the MibSPI5 module in compatibility mode, pin functional compatibility can be realized.
24	TEST	34	TEST	
25	N2HET[4]	36	N2HET[4]	
26	N2HET[6]	38	N2HET[6]	
27	MibSPI1nCS[2]	40	MibSPI1nCS[2]	
28	VCCIO	42	VCCIO	
29	VSS	43	VSS	
		44	VSS	
30	VCC	45	VCC	
31	nPORRST	46	nPORRST	
32	VCC	48	VCC	
		49	VCC	
33	VSS	50	VSS	
34	SPI3SOMI	51	MibSPI3SOMI	Subset is limited to standard/non-buffered mode
35	SPI3SIMO	52	MibSPI3SIMO	Subset is limited to standard/non-buffered mode
36	SPI3CLK	53	MibSPI3CLK	Subset is limited to standard/non-buffered mode
37	SPI3nENA	54	MibSPI3nENA	Subset is limited to standard/non-buffered mode

Table 2. Functional Pin Compatibility Mapping (continued)

LS04x/03x		LS31x/21x and LS12x/11x		Comments
Pin Number	Pin Name/Function	Pin Number	Pin Name/Function	
38	SPI3nCS[0]	55	MibSPI3nCS[0]	Subset is limited to standard/non-buffered mode
39	MibSPI1nCS[3]	3	MibSPI1nCS[3]	The directly compatible pin for MibSPI1nCS[3] is located on a different side of the 144QFP superset than on the 100QFP subset. This may require some additional board layout consideration when updating the superset/144QFP board design to accommodate the subset/100QFP.
40	ADIN[16]	58	AD1IN[16]	
41	ADIN[17]	59	AD1IN[17]	
42	ADIN[0]	60	ADIN[0]	
43	ADIN[7]	61	AD1IN[7]	
44	ADIN[20]	64	AD1IN[20]	
45	ADIN[21]	65	AD1IN[21]	
46	VCCAD/ADREFHI	66	ADREFHI	VCCAD and REFHI are combined on the subset package. REFHI limited to a range of 3-3.6V
		69	VCCAD	
47	VSSAD/ADREFLO	67	ADREFHI	VSSAD and REFLO are combined on the subset package. REFLO limited to GND.
		68	VSS	
48	ADIN[9]	70	AD1IN[9]	
49	ADIN[1]	71	AD1IN[1]	
50	ADIN[10]	72	AD1IN[10]	
51	ADIN[2]	73	AD1IN[2]	
52	ADIN[3]	74	AD1IN[3]	
53	ADIN[11]	75	AD1IN[11]	
54	ADIN[4]	76	AD1IN[4]	
55	ADIN[5]	78	AD1IN[5]	
56	ADIN[6]	80	AD1IN[6]	
57	ADIN[8]	83	AD1IN[8]	
58	ADEVT	86	ADEVT	
59	VSS	88	88	This subset pin has no direct matching pin in the 144QFE but can be connected directly to the common ground for the MCU
60	VCCIO	-	-	This subset pin has no direct matching pin in the 144QFE but can be connected directly to the common 3.3V rail for the MCU.
61	VCC	87	VCC	Connection to this pin involves additional trace routing to prevent crossing traces.

Table 2. Functional Pin Compatibility Mapping (continued)

LS04x/03x		LS31x/21x and LS12x/11x		Comments
Pin Number	Pin Name/Function	Pin Number	Pin Name/Function	
62	CAN1TX	89	CAN1TX	
63	CAN1RX	90	CAN1RX	
64	N2HET[24]	91	N2HET[24]	
65	MibSPI1SIMO	93	MibSPI1SIMO	
66	MibSPI1SOMI	94	MibSPI1SOMI	
67	MibSPI1CLK	95	MibSPI1CLK	
68	MibSPI1nENA	96	MibSPI1nENA	
69	SPI2SOMI	98	MibSPI5SOMI	There is no SPI2 or MibSPI2 available in the 144QFP superset package; therefore the subset pins map to the MibSPI5 functionally equivalent pins. The SPI2 module on the subset device is limited to non-buffered 4-pin mode only.
70	SPI2SIMO	99	MibSPI5SIMO	
71	SPI2CLK	100	MibSPI5CLK	
72	VSS	102	VSS	
73	MibSPI1nCS[0]	105	MibSPI1nCS[0]	
74	N2HET[8]	106	N2HET[8]	
75	TMS	108	TMS	
76	nTRST	109	nTRST	
77	TDI	110	TDI	
78	TDO	111	TDO	
79	TCK	112	TCK	
80	RTCK	113	RTCK	
81	nRST	116	nRST	
82	nERROR	117	nERROR	
83	N2HET[10]	118	N2HET[10]	
84	ECLK	119	ECLK	
85	VCCIO	120	VCCIO	
86	VSS	121	VSS	
87	VSS	122	VSS	
88	VCC	123	VCC	
89	N2HET[12]	124	N2HET[12]	
90	N2HET[14]	125	N2HET[14]	
91	CAN2TX	128	CAN2TX	
92	CAN2RX	129	CAN2RX	
93	MibSPI1nCS[1]	130	MibSPI1nCS[1]	
94	LINRX (UARTRX)	131	LINRX (UARTRX)	
95	LINTX (UARTTX)	132	LINTX (UARTTX)	
96	VCCP	134	VCCP	
97	N2HET[16]	139	N2HET[16]	
98	N2HET[18]	140	N2HET[18]	
99	VCC	143	VCC	
100	VSS	144	VSS	

4 Input/Output Considerations

There are some drive strength differences for output signals between the LS04x/03x series vs the LS31x/21x and LS12x/11x series of microcontrollers. These are listed in Table 3.

Table 3. Output Drive-Strength Differences Between LS04x/03x vs LS31x/21x and LS12x/11x

Output Signal Name LS04x/03x	Drive Strength on LS04x/03x	Output Signal Name LS31x/21x and LS12x/11x	Drive Strength on LS31x/21xand LS12x/11x
SPI2CLK	2 mA/ 8 mA Selectable (8mA default)	MibSPI5CLK	8 mA
SPI2SIMO	2 mA/ 8 mA Selectable (8mA default)	MibSPI5SIMO	8 mA
SPI2SOMI	2 mA/ 8 mA Selectable (8mA default)	MibSPI5SOMI	8 mA

5 Module Compatibility Considerations

The LS04x/03x series of microcontrollers are a subset of the features/functionality available on the LS12x/11x and LS31x/21x series of microcontrollers. As such, the majority of the software written for the superset devices, LS12x/11x and LS31x/21x, will be compatible with the LS04x/03x series of microcontrollers. However, in some cases, features that are utilized in the superset devices will need to be considered either during development of the software or during the porting process to the subset device. In addition, the LS04x/03x series of microcontrollers has similar enhancements to key peripherals as the LS12x/11x series of microcontrollers. Some key feature differences and brief description of the peripheral enhancements are listed below.

5.1 Feature Differences on LS04x/03x Series

The LS04x/03x series of microcontrollers is a subset of the LS31x/21x and LS12x/11x series of microcontrollers. Some features are not included as a result of the simpler implementation.

5.1.1 Feature Implementation Differences for the LS04x/03x Series

- Floating Point support

  The LS04x/03x series of microcontrollers do not support floating point operation (R4 vs R4F).
- Flash EEPROM emulation bank

  The module IP used for the Flash EEPROM emulation is new on the LS04x/03x series. This new bank is a 72-bit wide bank with slower access times than the bank used on super set series. The EWAIT parameter within the Flash Wrapper register set will need to be programmed according to the waitstates defines in the datasheet for LS04x/03x series of microcontrollers.
- Pin muxing/IOMM configuration

  During development, the definition of the pin muxing control registers in the IOMM module required significant deviation from the pin muxing implemented on the super set series of devices. As a result, the PINMMR register assignments are unique to the LS04x/03x series although there are some common muxed pin functions that are achievable.
- CPU BIST/STC implementation

  For the LS04x/03x series of microcontrollers, the number of STC intervals is greater than the implementation on the superset devices. The total number of intervals to achieve maximum CPU BIST testing on the LS04x/03x series is 26 vs 24 intervals on the superset devices. However, it is worth noting, that coverage >90% is achieved using only the 24 defined for the supersets.
- Time Base feature in the RTI module

  The Time Base feature is a feature that is primarily included on devices with FlexRay IP in order to synchronize timing between FlexRay network and the devices RTI counters. Given FlexRay is not included in the LS04x/03x series, this feature is not implemented.

- IF3 Interrupt for DCAN1 and DCAN2

  The IF3 interrupt is used, primarily, in conjunction with the DMA controller to notify when a DMA transfer of an updated message can occur. Given the DMA module is not implemented in the LS04x/03x series, this feature is not implemented.
- Full Auto and Semi-CPU modes within the CRC module

  The Full Auto and Semi-CPU modes of the CRC peripheral require the DMA controller. Given that DMA is not implemented in the LS04x/03x series, these features are not supported in this series. Full CPU mode with the bus "snooper" feature are supported as described in the Technical Reference Manual.
- 5V ADC capability

  The ADC as implemented in the LS04x/03x series, does not support 5V operation. The maximum ADC input is specified as 3.6V for this series of microcontrollers.
- ADREFHI/LO limitation

  In order to maximize the pin utilization in the 100pin QFP used for the LS04x/03x series, the ADC supply pins were combined with the reference pins. This limits the ADREFHI to 3-3.6V and ADREFLO to VSSAD/GND.
- DMA transfers to/from peripheral RAMs

  As previously noted, the LS04x/03x series of microcontrollers do not have a DMA controller. This means that accesses to/from the peripheral RAMS, must be made through the CPU with the exception of transfers to N2HET which can be made using the HTU module.

5.2 Module Enhancements on LS12x/11x and LS04x/03x Series

The LS12x/11x and LS04x/03x series of microcontrollers implements enhancements to two peripherals: the high-end timer (N2HET) and the multi-buffered analog-to-digital converter (ADC).

5.2.1 N2HET Enhancements on LS12x/11x and LS04x/03x Series

- Selectable Hardware Angle Generator (HWAG) Toothed-Wheel Input

  The N2HET modules, on all of the series of microcontrollers, the LS31x/21x, LS12x/11x as well as the LS04x/03x series of microcontrollers, supports an embedded HWAG. The function of the HWAG is to generate an angle value from a toothed-wheel input. This toothed-wheel input to the N2HET came from the N2HET[2] channel. This allocation was fixed and could not be programmed by the application on the LS31x/21x series of microcontrollers. The HWAG on the LS12x/11x and LS04x/03x series now includes a programmable register that allows the application to select the N2HET channel that is used to provide the toothed-wheel input. This register still defaults to using N2HET[2] as the toothed-wheel input, thereby, maintaining backwards compatibility to the N2HET peripheral on LS31x/21x.
- Input Capture Enhancements

  The N2HET input capture functionality is also enhanced on the LS12x/11x and LS04x/03x series of microcontrollers compared to the LS31x/21x series. On the LS31x/21x series, the input signal on an N2HET channel must follow these two rules:

  – The input signal period must be at least twice the N2HET loop-resolution-clock period, and

  – Each phase of the input signal must be at least one N2HET loop-resolution-clock period

  On the LS12x/11x and LS04x/03x series, the input signal on an N2HET channel must follow these two rules:

  – The input signal period must be at least one N2HET loop-resolution-clock period, and

  – Each phase of the input signal must be at least twice the N2HET high-resolution-clock period

  As can be seen, the N2HET on the LS12x/11x and LS04x/03x can be used to measure input pulse widths smaller than one loop-resolution-clock period.

5.2.2 ADC Enhancements on the LS12x/11x and LS04x/03x Series

- Enhanced Channel Selection Mode

  The ADC module on the LS31x/21x series performs sequential conversions on the number of channels selected in any particular conversion group (event group, group1 or group2). This conversion starts with the lowest numbered channel selected and proceeds in ascending order until all selected channels have been converted. The LS12x/11x and LS04x/03x series introduces an enhanced channel selection mode, wherein, a look-up table is used to define the channel number to be converted. This provides the application the capability of repeatedly sampling the same analog input channel, or to define an arbitrary channel conversion sequence, or to switch the conversion sequence while conversions are already ongoing. For more details, see the *ADC* chapter of the *TMS570LS12x/11x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual* (SPNU515) or the *TMS570LS04x/03x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual* (SPNU517)

- LS12x/11x also adds Support for External Analog Multiplexors

  The look-up table used to support the enhanced channel selection mode also allows the application to output external channel select and enable signals. These signals can then be connected to external analog multiplexors, thereby, increasing the number of analog input channels that can be converted by the ADC. The LS12x/11x series supports connecting up to 4:1 external analog multiplexor on each of the 24 unique ADC input channels, effectively providing the ability to convert up to 96 input channels. This feature is not available on the LS04x/03x series of microcontrollers.

5.3 LS04x/03x Compatibility With the New Modules on the LS12x/11x Series

The LS12x/11x series introduces three new enhanced timing peripherals (eTPWM, eCAP and eQEP). The LS04x/03x series of microcontrollers shares content for one of these modules (eQEP). In the LS04x/03x series, as in the LS12x/11x series, the terminals for this peripheral are multiplexed with existing functions and require additional configuration of the I/O multiplexing module to enable outputs. The multiplexing configuration and terminals that are associated with this peripheral are not implemented on common pins and will require adjustments in the PCB layout to accommodate the difference.

- Enhanced Quadrature Encoded Pulse Generator (eQEP)

  There is one eQEP module implemented on the LS04x/03x series versus two on the LS12x/11x series. The eQEP module uses a 32-bit position counter, supports low-speed measurement using the capture unit and high-speed measurement using a 32-bit unit timer. This module has a watchdog timer to detect motor stall and input error detection logic to identify simultaneous edge transition in QEP signals. In addition, There are several register configuration options within the PINMMR registers to configure input filtering and error notification routing. Since the LS04x/03x series does not include the eCAP and eTPWM modules, the implementation of eQEP is done in a way that assumes N2HET use as a replacement for the functions associated with these enhanced timing modules.

6 References

- *TMS570LS04x/03x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual* (SPNU517)

Revision History

Changes from Original (December 2012) to A Revision	Page
• Made updates to Table 2.	2

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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