Application Report
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Reduction of Power Consumption for RM48L950

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ABSTRACT

This application report describes methods to reduce the power consumption of the Hercules™-based microcontrollers and gives indications for the reduction that can be achieved.

All examples and values are based on the xRM48L950ZWTT (Rev. A) microcontroller and are measured on the TI internal silicon checkout board.

Measurement Notes

The measurements were done on non-production silicon and not under controlled environment conditions (unregulated room temp, unregulated humidity). The used measurement equipment was high industry standard. All values in this application report might differ from silicon to silicon, with the used measurement equipment and are superset by the values in the corresponding device-specific data sheets.

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1 Measurement Setup

The measurements were done on a TI internal silicon checkout board with a non-production xRM48L950ZWTT (Rev. B) microcontroller. The ambient temperature and humidity was unchecked and unregulated.

The current consumption of each power rail (1.2 V core + PLL and 3.3 V IO + Flash + ADC) was measured with two Keithley 2000 multimeters, the currents were directly measured through the multimeters.

The microcontroller startup and peripheral initialization were done with the hardware abstraction layer code generator (HALCoGen) v3.01.00 generated functions. All peripheral, as possible, were setup as GIO functional. All GIO pins were set as output and to drive low level. There was no activity on the peripherals. The used CPU frequency (HCLK) was 200 MHz with a 16 MHz oscillator as source. With these, an overall current consumption of about 200 mA for the 1.2 V rail and 70 mA for the 3.3 V was measured.

The reduction of the CPU frequency (HCLK) for the current consumption versus frequency measurements (Section 3.2) was done by reducing the PLL1 frequency. This means that the frequency of all other clock domains connected to PLL1 also was reduced.

Table 1 and Table 2 show the approximate current consumption and clock domain frequencies based on the setup described above for both devices.

Table 1. Clock Domain Frequencies

Clock Domain and Source	Source	Frequency [MHz]	Maximum Frequency [MHz]
OSC	Crystal	16.0	20.0
PLL1	OSC x 12.5	200.0	
PLL2	OSC x 3	48.0	
HCLK	PLL1	200.0	200.0
GCLK	HCLK	200.0	200.0
VCLK1	PLL1 / 2	100.0	100.0
VCLK2	PLL1 / 2	100.0	100.0
VCLK3	PLL1 / 2	100.0	100.0
AVCLK1	VCLK	100.0	100.0
AVCLK3	PLL2	48.0	48.0
AVCLK4	VCLK / 2	50.0	50.0
RTICLK	VCLK	100.0	100.0

Table 2. Overall Current Consumption

Power Rail [(1)]		xRM48L950ZWTT
Core + PLL [mA]	$I_{CC} + I_{CCPLL}$	197.6
IO + Flash + ADC [mA]	$I_{CCIO} + I_{CCAD} + I_{CCREFHI} + I_{CCP}$	72.0

(1) Rails are divided into 1.2 V and 3.3 V rail and are called as stated in the left column in the rest of this document.

2 Power Down Functions

Possible features to reduce the power consumption are:

- Peripheral Power Down
- Clock Domain Disable
- Local Peripheral Power Down
- Power Domain Disable
- Clock Source Disable
- Flash Bank Suspend
- Low-Power Mode

The peripheral power down, clock domain disable, and local peripheral power down features disable the clock going to the peripheral modules or the RAM's. This reduces the power consumption to its static state value.

The power domain disable feature switches of the supply voltage for a group of modules. With this feature the modules in the power domain will not consume any more power, but this is only available for a group of modules.

The clock sourced disable feature allows disabling the internal clock generation (PLL and LPO) if they are not needed.

The Flash bank suspend feature switch Flash banks into suspend modes. This reduces the power consumption of the Flash module.

The low-power mode feature is a combination of the clock domain disable, clock source disable, and Flash bank suspend features. Also, it sets the core into idle mode.

Table 3 lists the pros and cons of the different power down functions for the peripheral modules.

Table 3. Pros and Cons of the Different Power Down Functions

	Pros	Cons
Clock disable	Available for each single peripheral module and memory	Power consumption is only reduced to its steady state value
Supply disable	As the supply is completely switched off, no power consumption at all.	Only seven powered domains are available

2.1 Peripheral Power Down

The device has 32 peripheral select (PS) and each PS has a size of 1 KB. Depending on the module, the full, half or quarter of a PS can be used. So there are four quadrants for each PS. Each quadrant can be enabled or disabled using the set of Peripheral Central Resource Control Register (PCR): Peripheral Power-Down Set Register (PSPWRDWNSETx) and Peripheral Power-Down Clear Register (PSPWRDWNCLRx). Figure 1 shows the register implementation.

Figure 1. Peripheral Central Resource Control Register Implementation

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PS7 Q3	PS7 Q2	PS7 Q1	PS7 Q0	PS6 Q3	PS6 Q2	PS6 Q1	PS6 Q0	PS5 Q3	PS5 Q2	PS5 Q1	PS5 Q0	PS4 Q3	PS4 Q2	PS4 Q1	PS4 Q0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS3 Q3	PS3 Q2	PS3 Q1	PS3 Q0	PS2 Q3	PS2 Q2	PS2 Q1	PS2 Q0	PS1 Q3	PS1 Q2	PS1 Q1	PS1 Q0	PS0 Q3	PS0 Q2	PS0 Q2	PS0 Q0

This arrangement is the same for bits of PS8 to PS31.

Table 4 shows how the peripheral select is defined.

Table 4. Peripheral Select Definition

Peripheral Select		Start Address	End Address
PS7		0xFFF7E000	0xFFF7E3FF
PS6		0xFFF7E400	0xFFF7E7FF
PS5		0xFFF7E800	0xFFF7EBFF
PS4		0xFFF7EC00	0xFFF7EFFF
PS3		0xFFF7F000	0xFFF7F3FF
PS2		0xFFF7F400	0xFFF7F7FF
PS1		0xFFF7F800	0xFFF7FBFF
PS0	Q0	0xFFF7FC00	0xFFF7FCFF
	Q1	0xFFF7FD00	0xFFF7FDFF
	Q2	0xFFF7FE00	0xFFF7FEFF
	Q3	0xFFF7FF00	0xFFF7FFFF

PS 8 – 31 follows this scheme.

Table 5 shows which PS is used to select a peripheral module and MSINENA, which is used to initialize RAM, that is associated to the peripheral.

Table 5. Periphery and Their Peripheral Select, Peripheral Memory and Memory Initialization

Module Address Range	RM42L432	RM46Lx50	RM48Lx50
HTU1 0xFFF7A400 - 0xFFF7A4FF	PS[22] Q[0] MSINENA[4]	PS[22] Q[0] MSINENA[4]	PS[22] Q[0] MSINENA[4]
HTU2 0xFFF7A500 - 0xFFF7A5FF	- -	PS[22] Q[1] MSINENA[16]	PS[22] Q[1] MSINENA[16]
N2HET1 0xFFF7B800 - 0xFFF7B8FF	PS[17] Q[0] MSINENA[3]	PS[17] Q[0] MSINENA[3]	PS[17] Q[0] MSINENA[3]
N2HET2 0xFFF7B900 - 0xFFF7B9FF	- -	PS[17] Q[1] MSINENA[15]	PS[17] Q[1] MSINENA[15
GIO 0xFFF7BC00 - 0xFFF7BCFF	PS[16] Q[0] -	PS[16] Q[0] -	PS[16] Q[0] -
MibADC1 0xFFF7C000 - 0xFFF7C1FF	PS[15] Q[0, 1] MSINENA[8]	PS[15] Q[0, 1] MSINENA[8]	PS[15] Q[0, 1] MSINENA[8]
MibADC2 0xFFF7C200 - 0xFFF7C3FF	- -	PS[15] Q[2, 3] MSINENA[14]	PS[15] Q[2, 3] MSINENA[14]
I2C 0xFFF7D400 - 0xFFF7D4FF	- -	PS[10] Q[0]	PS[10] Q[0]
DCAN1 0xFFF7DC00 - 0xFFF7DDFF	PS[8] Q[0, 1] MSINENA[5]	PS[8] Q[0, 1] MSINENA[5]	PS[8] Q[0, 1] MSINENA[5]
DCAN2 0xFFF7DE00 - 0xFFF7DFFF	PS[8] Q[2, 3] MSINENA[6]	PS[8] Q[2, 3] MSINENA[6]	PS[8] Q[2, 3] MSINENA[6]
DCAN3 0xFFF7E000 - 0xFFF7E1FF	- -	PS[7] Q[0, 1] MSINENA[10]	PS[7] Q[0, 1] MSINENA[10]
LIN 0xFFF7E400 - 0xFFF7E4FF	PS[6] Q[0] -	PS[6] Q[0] -	PS[6] Q[0] -
SCI 0xFFF7E500 - 0xFFF7E5FF	- -	PS[6] Q[1] -	PS[6] Q[1] -
MibSPI1 0xFFF7F400 - 0xFFF7F5FF	PS[2] Q[0, 1] MSINENA[7]	PS[2] Q[0, 1] MSINENA[7]	PS[2] Q[0, 1] MSINENA[7]
SPI2 0xFFF7F600 - 0xFFF7F7FF	PS[2] Q[2, 3] -	PS[2] Q[2, 3] -	PS[2] Q[2, 3] -
MibSPI3 0xFFF7F800 - 0xFFF7F9FF	- -	PS[1] Q[0, 1] MSINENA[11]	PS[1] Q[0, 1] MSINENA[11]

Table 5. Periphery and Their Peripheral Select, Peripheral Memory and Memory Initialization (continued)

Module Address Range	RM42L432	RM46Lx50	RM48Lx50
SPI3 0xFFF7F800 - 0xFFF7F9FF	PS[1] Q[0, 1] -	- -	- -
SPI4 0xFFF7FA00 - 0xFFF7FBFF	- -	PS[1] Q[2, 3] -	PS[1] Q[2, 3] -
MibSPI5 0xFFF7FC00 - 0xFFF7FDFF	- -	PS[0] Q[0, 1] MSINENA[12]	PS[0] Q[0, 1] MSINENA[12]

For more information, see the *Device Memory Map* section of the device-specific data sheet.

NOTE: Every access to a register of a module where clock supply is disabled will reactivate the clock supply as long as the access continues.

2.1.1 Example Disabling MibSPI1

The corresponding PS decodes all addresses between 0xFFF7F400 and 0xFFF7F7FF. MIBSPI1 and SPI2 are mapped to this PS2 as following:

- PS2 quadrant 0 and quadrant 1 are for MibSPI1 for a total of 512 bytes
- PS2 quadrant 2 and quadrant 3 are for SPI2 for a total of 512 bytes

To disable the MibSPI1, bits 8 and 9 of the Peripheral Power-Down Set Register 0 (PSPWRDWNSET0) have to be set.

NOTE: Disabling a module that has a memory can produce an error when the Memory Initialization Enable Register (MSINENA) of the Memory Hardware Initialization Control Registers is not adjusted.

The preferred method should be to disable both the peripheral and the memory initialization.

For more information, see the *Auto-Initialization of Device Memories* section of the device-specific data manual.

2.1.2 Results

Table 6 shows the approximate current reduction in mA based on the setup described in Section 1, which can be achieved by switching the clock supply to a peripheral module off.

Table 6. Peripheral Select Reduction

Power Rail	HTU	N2HET	GIO	MibADC	I2C	DCAN	LIN	SCI	MibSPI
Core + PLL [mA]	1.5	5.7	2.1	2.4	3.0	4.2	2.4	2.2	3.4
IO + Flash ADC [mA]	0.0	0.0	0.0	6.0	0.0	0.0	0.0	0.0	0.0

2.2 Clock Domains

The clocking on the device is divided into multiple clock domains for flexibility in control as well as clock source selection. Figure 2 and Table 7 shows the available clock domains.

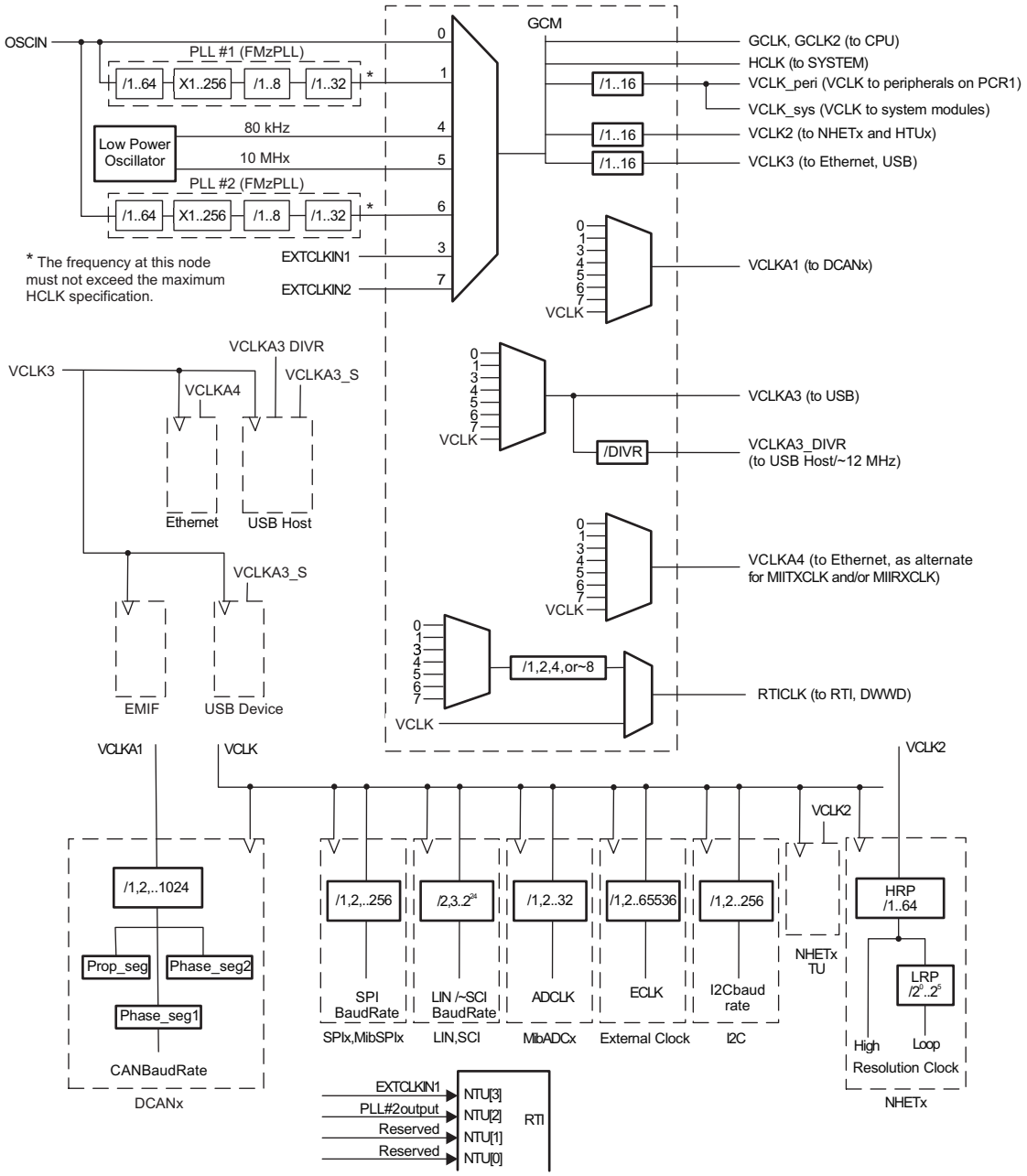

Figure 2. Clock Domain Diagram

Table 7. Clock Domains and Their Domain Number

Clock Domain	Domain Number
GCLK / GCLK2	0
HCLK	1
VCLK	2
VCLK2	3
VCLK3	8

Table 7. Clock Domains and Their Domain Number (continued)

Clock Domain	Domain Number
AVCLK1	4
AVCLK2 (1)	5
AVCLK3	10
AVCLK4	11
RTICLK	6

(1) Not available on RM48.

Each clock domain can be independently enabled or disabled using the set of registers: Clock Domain Disable Register (CDDIS), Clock Domain Disable Set Register (CDDISSET) and the Clock Domain Disable Clear Register (CDDISCLR).

Each bit in these registers corresponds to the clock domain number. For example:

Setting bit 1 in the CDDIS or CDDISSET registers disables the HCLK clock domain.

All clock domains are enabled by default, or upon a system reset, or whenever a wake up condition is detected.

NOTE: The clock domain is turned off only when every module that uses the HCLK domain is in idle or disabled.

For more information, see the *Clock Domains* chapter of the device-specific technical reference manual.

2.2.1 Results

Table 8 shows the approximate current reduction in mA based on the setup described in Section 1, which can be achieved by switching a clock domain off.

Table 8. Clock Domain Disable Reduction

Power Rail	VCLK	VCLK2	VCLK3	AVCLK1	AVCLK2	AVCLK3	AVCLK4	RTICLK1	HCLK	GCLK
Core + PLL [mA]	21.8	14.9	9.0	1.9	2.7	3.1	2.4	2.2	1.9	1.8
IO + Flash + ADC [mA]	11.0	0.0	25.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0

2.3 Clock Sources

Table 9 shows the available clock sources.

Table 9. Clock Sources and Their Source Number

Clock Source	Source Number
OSCIN	0
PLL 1	1
(Not implemented)	2
EXTCLKIN 1	3
LF LPO	4
HF LPO	5
PLL 2	6
EXTCLKIN 2	7

Each clock source can be independently enabled or disabled using the set of registers: Clock Source Disable Register (CSDIS), Clock Source Disable Set Register (CSDISSET), and the Clock Source Disable Clear Register (CSDISCLR).

Each bit in these registers corresponds to the clock source number. For example:

Setting bit 1 in the CSDIS or CSDISSET registers disables the PLL#1.

NOTE: The clock source is only disabled once there is no active clock domain that is using the clock source. So, the application has to first disable all of the clock domains that are using the clock source or switch them to another clock source.

The Clock Source Valid Status Register (CSVSTAT) indicates the current clock source stats.

On the RM48 microcontrollers, the clock sources 0, 4 and 5 are enabled by default.

NOTE: By default, the clock monitoring circuit is enabled and checks for the main oscillator frequency to be within a certain range using the HF LPO as a reference. If the main oscillator or the HF LPO are disabled with the clock monitoring still enabled, the clock monitor will indicate an oscillator fault. The clock monitoring must be disabled before disabling the main oscillator or the HF LPO clock source.

For more information, see the *Clock Sources* chapter of the device-specific technical reference manual.

2.4 Power Domains

The core logic is divided into several domains that can be independently turned on or off based on the application's requirements.

NOTE: The microcontrollers only support static switching of the power domains. That is, the power domains can be turned ON or OFF one time during device initialization. Once configured, it is not allowed to change the state of a power domain without first asserting a system reset.

Table 10 shows the available core power domains.

Table 10. Power Domains and Their Corresponding Register

Power Domain	Modules	Register
PD1	Cortex-R4F CPU, Flash interface, TCRAM interface, clock control, basic peripheral set, 64KB RAM	-
PD2	EGTM, RTP, DMM, ETMR4, FuseFarm, CSTPIU, POM	PDCLKDISREG[0] LOGICPDPWRCTRL0[27-24]
PD3	N2HET2, HTU2, SPI4, MIBADC2, DCAN3, SCI, I2C, DCC2	PDCLKDISREG[1] LOGICPDPWRCTRL0[19-16]
PD5	USB host and USB device, Ethernet, EMIF	PDCLKDISREG[3] LOGICPDPWRCTRL0[3-0]
RAM_PD1	64 KB RAM	MEMPDPWRCTRL0[27-24]
RAM_PD2	64 KB RAM	MEMPDPWRCTRL0[19-16]
RAM_PD3	64 KB RAM	MEMPDPWRCTRL0[11-8]

PD1 is an "always-ON" power domain, which cannot be turned off. PD2 - PD5 can be turned off by doing the following steps:

1. Set the corresponding bit in the Power Domain Clock Disable Register (PDCLKDISREG) to disable all clocks to the power domain.
2. Write 0xA to the corresponding position in the Logic Power Domain Control Register (LOGICPDPWRCTRL0) to power down the domain.
3. Optional: Poll for LOGICPDPWRSTATx to become "00". The power domain is now powered down.

A power domain with only SRAM macros does not have a clock input, so the sequence is shorter. This applies to RAM_PD1 - RAM_PD3:

1. Write 0xA to the corresponding position in the Memory Power Domain Control Register 0 (MEMPDPWRCTRL0) to power down the domain.
2. Optional: Poll for MEMPDPWRSTATx to become “00”. The power domain is now powered down.

NOTE: The logic in the modules that are powered down loses its power completely. Any access to modules that are powered down results in an abort being generated. When power is restored, the modules power-up to their default states (after normal power-up). No register or memory contents are preserved in the core domains that are turned off.

2.4.1 Results

Table 11 shows the approximate current reduction in mA based on the setup described in Section 1, which can be achieved by switching a power domain off.

Table 11. Power Domain Disable Reduction

Power Rail	PD2	PD3	PD5	RAM_PD
Core + PLL [mA]	9.5	3.3	12.4	2.1
IO + Flash + ADC [mA]	0.0	6.0	25.0	0.0

2.5 Flash Banks

Flash is divided into three banks that can be independently switched to active, standby, and sleep mode based on the time since the last access. The time and the mode can be set using the set of the Flash control register: Flash Bank Fallback Power Register (FBFALLBACK) and Flash Bank Access Control Register (FBAC).

Table 12 shows the Flash bank fallback mode implementation.

Table 12. Flash Bank Fallback Power Register

Field	Value	Description
BANKPWR0	0h	Sleep mode
	1h	Standby mode
	3h	Active mode

This arrangement is the same for the other banks.

After the last access to a Flash bank, the active grave time counter starts to count down before putting the bank into one of the fallback power modes as determined by the FBFALLBACK register. This active grave time can be assigned in the BAGP field of the Flash bank access control register.

NOTE: The active grave time value must be greater than 1 when the fallback mode is not active.

For more information, see the *Flash module* chapter of the device-specific technical reference manual.

2.5.1 Results

Table 13 shows the approximate current reduction in mA based on the setup described in Section 1, which can be achieved by switching a Flash bank to sleep mode.

Table 13. Flash Bank Sleep Mode Reduction

Power Rail	Bank 0	Bank 1	Bank 7
Core + PLL [mA]	0.0	0.0	0.0
IO + Flash + ADC [mA]	3.0	5.0	4.0

2.6 Low-Power Mode

The ARM® Cortex™-R4F CPU has internal power management logic, and requires a dedicated instruction to be used in order to enter a low-power mode. This is the Wait For Interrupt (WFI) instruction. When a WFI instruction is executed, the Cortex-R4F core flushes its pipeline, flushes all write buffers, and completes all pending bus transactions. At this time the core indicates to the system that the clock to the core can be stopped. This indication is used by the Global Clock Module (GCM) to turn off the CPU clock domain (GCLK) if the CDDIS register bit 0 is set. Table 14 shows the low-power modes.

Table 14. Low-Power Modes

	Active Clock Source	Active Clock Domain	Wake Up Options
Doze	Main oscillator	RTICLK	RTI, GIO, CAN, SCI
Snooze	LF LPO	RTICLK	RTI, GIO, CAN, SCI
Sleep	None	None	GIO, CAN, SCI

The typical software sequence to enter a low-power mode is as follows:

1. Program the Flash banks fallback modes to be “sleep”. The Flash banks start switching from active to sleep mode only after the banks are not accessed for at least a duration defined by the Active Grace Period (AGP) parameter configured for the banks.

   For more details, see Section 2.5.
2. Disable the clock sources that are not required to be kept active. A clock source does not get disabled until all clock domains using that clock source are disabled first or are configured to use an alternate clock source.
3. Disable the clock domains that are not required to be kept active. A clock domain does not get disabled until all modules using that clock domain are disabled or in idle.

   For more details, see Section 2.2.
4. Idle the Cortex-R4F core. To idle the core uses the WFI instruction.

2.6.1 Results

Table 15 shows the approximate current in mA based on the setup described in Section 1, which will be consumed after switching to a low-power mode.

Table 15. Low-Power Mode Consumption

Power Rail	Normal	Snooze	Doze	Sleep
Core + PLL [mA]	197.6	18.8	18.8	1.6
IO + Flash + ADC [mA]	72.0	6.0	6.0	1.0
Wake up time [us]	—	14.0	14.0	670.0

3 Hints and Tips

Some hints and tips to reduce the power consumption are listed and discussed in this section.

3.1 Terminate Unused GPIOs

When an unused port pin is left undefined or non-terminated, the floating voltage or shoot-through current on the pin can increase the overall current consumption. To avoid this, each and every port on the device needs to be initialized and terminated. Unused pins should be set as output and drive low level.

3.2 Reduce CPU Clock

A higher clock frequency results a faster charge reversal, this increases the overall current consumption. The highest frequency for the application should be used instead of using the highest 'available' frequency. Figure 3 shows the current reduction versus HCLK for RM48L950, the VLCK:HCLK ratio was fixed to 1:2 during these measurements. For more information regarding the setup, see Section 1.

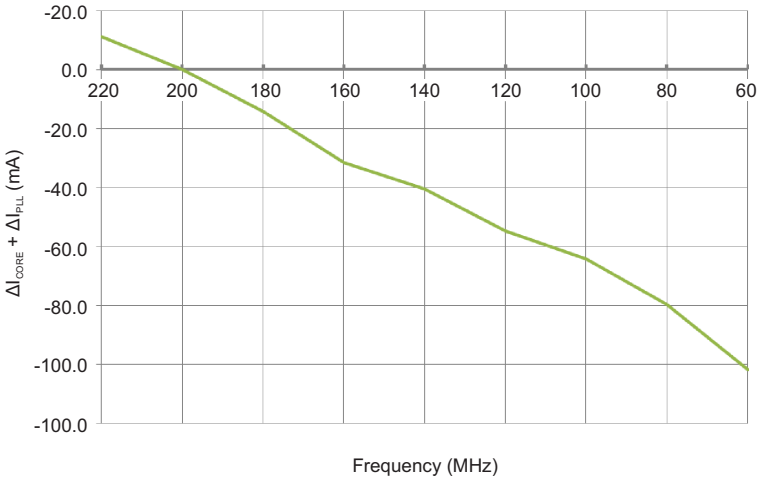

Figure 3. Current Reduction Versus HCLK on RM48L950

3.3 Disable Unused Peripherals

When an unused peripheral is left activated, it is still powered. To avoid unnecessary power consumption, all unused peripherals should be disabled.

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