ARM Core
Cortex™-M4 (AT520) and Cortex-M4F (AT521)
Errata Notice

This document contains confirmed errata in supported releases up to and including revision r0p1 of Cortex-M4

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General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- a unique defect tracking identifier
- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1   Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2   Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3   Behavior that was not the originally intended behavior but should not cause any problems in applications.

Implementation   Errata that are of particular interest to those implementing the product and that have no software implications

System   Errata or possible issues that have system implications and therefore should be considered by system designers

Change Control

14 Jan 2011: Changes in Document v3

Page	Status	ID	Cat	Summary
9	New	752770	Cat 2	Interrupted loads to SP can cause erroneous behaviour

29 Jun 2010: Changes in Document v2

Page	Status	ID	Cat	Summary
12	New	740454		System BRCHSTAT may be non-optimal in some cases

22 Dec 2009: Changes in Document v1

There are no errata contained in this version

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus $\boxed{\textbf{X}}$ indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0	r0p1
752770	Cat 2	Interrupted loads to SP can cause erroneous behaviour	X	X
740454	System	BRCHSTAT may be non-optimal in some cases	X	

Errata - Category 1

There are no Errata in this Category

Errata - Category 2

752770: Interrupted loads to SP can cause erroneous behaviour

Status

Affects: product Cortex-M4.

Fault status: Cat 2, Present in: r0p0,r0p1, Open.

Description

If an interrupt occurs during the data-phase of a single word load to the stack-pointer (SP/R13), erroneous behaviour can occur. In all cases, returning from the interrupt will result in the load instruction being executed an additional time. For all instructions performing an update to the base register, the base register will be erroneously updated on each execution, resulting in the stack-pointer being loaded from an incorrect memory location.

The affected instructions that can result in the load transaction being repeated are:

1. LDR SP,[Rn],#imm
2. LDR SP,[Rn,#imm]!
3. LDR SP,[Rn,#imm]
4. LDR SP,[Rn]
5. LDR SP,[Rn,Rm]

The affected instructions that can result in the stack-pointer being loaded from an incorrect memory address are:

1. LDR SP,[Rn],#imm
2. LDR SP,[Rn,#imm]!

Conditions

1. An LDR is executed, with SP/R13 as the destination
2. The address for the LDR is successfully issued to the memory system
3. An interrupt is taken before the data has been returned and written to the stack-pointer.

Implications

Unless the load is being performed to Device or Strongly-Ordered memory, there should be no implications from the repetition of the load. In the unlikely event that the load is being performed to Device or Strongly-Ordered memory, the repeated read can result in the final stack-pointer value being different than had only a single load been performed.

Interruption of the two write-back forms of the instruction can result in both the base register value and final stack-pointer value being incorrect. This can result in apparent stack corruption and subsequent unintended modification of memory.

Workaround

Both issues may be worked around by replacing the direct load to the stack-pointer, with an intermediate load to a general-purpose register followed by a move to the stack-pointer.

If repeated reads are acceptable, then the base-update issue may be worked around by performing the stack-pointer load without the base increment followed by a subsequent ADD or SUB instruction to perform the appropriate update to the base register.

Errata - Category 3

There are no Errata in this Category

Errata - System

740454: BRCHSTAT may be non-optimal in some cases

Status

Affects: product Cortex-M4.

Fault status: System, Present in: r0p0, Fixed in r0p1.

Description

Cortex-M4 performs branch speculation based on decode time branches. This can mean that a fetch access may not actually be required if the speculation is incorrect. The BRCHSTAT output of the core can be used to optimise the operation of memory controllers or prefetchers in the cases where the speculation is incorrect.

BRCHSTAT can indicate if a decode time branch is conditional, and therefore being speculated on, and in the next cycle it will indicate whether the branch is taken or not which can be used to determine whether the fetch access can be discarded or not. With this erratum the core may incorrectly indicate a branch as not being speculated, and therefore required, when in fact it may be a speculative fetch access. This means that the external memory system does not have an opportunity to discard the access and improve the system performance. This is not a functional erratum; it is a slight performance erratum.

Conditions

1. BRCHSTAT is being used in the memory system to help improve access performance

2. BRCHSTAT is being used to discard speculated fetch accesses

3. Wait states are present in the instruction fetches

4. A branch is present in an IT block

5. A stall is inserted before the branch (for example, the branch has not been fetched yet)

6. The branch is speculated and not taken but BRCHSTAT indicates it is not conditional

Implications

Since BRCHSTAT may indicate a branch is not conditional when it really is then the memory system believes that the fetch is required and therefore has no opportunity to cancel the unnecessary access. This is therefore a performance rather than a functional erratum.

Workaround

No workaround is possible.

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