Technical Reference Manual

LP873362-Q1 Technical Reference Manual

ABSTRACT

This document provides the register bit values for the one-time programmable (OTP) bits of the orderable part number, LP873362RHDRQ1.

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1 Introduction

This technical reference manual can be used as a reference for the LP873362-Q1 default register bits after OTP memory download. This technical reference manual does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the *LP8733xx-Q1 Dual High-Current Buck Converter and Dual Linear Regulator* data sheet.

2 OTP Memory Device Settings

This section lists all of the device settings that are downloaded from OTP memory.

Table 2-1 lists the device settings for I^2C and OTP revision ID values.

Table 2-1. Device Identification and I^2C Settings

	Description	Bit Name	LP873362-Q1
I^2C address			60h
DEVICE_ID	Device specific ID code	DEVICE_ID	02h
OTP_ID	Identification code for OTP version	OTP_ID	62h

Table 2-2 lists the device settings for BUCK0 and BUCK1. The maximum allowed slew-rate for BUCKx depends on the output capacitance. Refer to the *LP8733xx-Q1 Dual High-Current Buck Converter and Dual Linear Regulator* data sheet for output capacitance boundary conditions.

Table 2-2. BUCK0 and BUCK1 OTP Settings

	Description	Bit Name	LP873362-Q1
	Buck phase configuration (2 single phase Bucks or combined 2 phase, denoted as 1+1 or 2-phase)		2-ph
	Switching frequency		2 MHz
	Spread spectrum	EN_SPREAD_SPEC	Disabled

Table 2-2. BUCK0 and BUCK1 OTP Settings (continued)

	Description	Bit Name	LP873362-Q1
BUCK0	Output voltage	BUCK0_VSET	0.850 V
	Enable, EN-pin or I²C register	BUCK0_EN_PIN_CTRL	EN-pin
	Control for BUCK0	BUCK0_EN	High
	Force PWM mode or auto mode	BUCK0_FPWM	Force PWM
	Force Multiphase	BUCK0_FPWM_MP	Yes
	Peak current limit	BUCK0_ILIM	4 A
	Maximum load current limit	NA	3 A
	Slew rate	BUCK0_SLEW_RATE	3.8 mV/us
	Startup delay	BUCK0_STARTUP_DELAY	3 ms
	Shutdown delay	BUCK0_SHUTDOWN_DELAY	2 ms
BUCK1	Output voltage	BUCK1_VSET	0.850 V
	Enable, EN-pin or I²C register	BUCK1_EN_PIN_CTRL	EN-pin
	Control for BUCK1	BUCK1_EN	High
	Force PWM mode or auto mode	BUCK1_FPWM	Force PWM
	Peak current limit	BUCK1_ILIM	4 A
	Maximum load current limit	NA	3 A
	Slew rate	BUCK1_SLEW_RATE	3.8 mV/us
	Startup delay	BUCK1_STARTUP_DELAY	3 ms
	Shutdown delay	BUCK1_SHUTDOWN_DELAY	2 ms

Table 2-3 lists the device settings for LDO0 and LDO1.

Table 2-3. LDO0 and LDO1 OTP Settings

	Description	Bit Name	LP873362-Q1
LDO0	Output voltage	LDO0_VSET	1.800 V
	Enable, EN-pin or I²C register	LDO0_EN_PIN_CTRL	EN-pin
	Control for LDO0	LDO0_EN	High
	Startup delay	LDO0_STARTUP_DELAY	0 ms
	Shutdown delay	LDO0_SHUTDOWN_DELAY	4 ms
LDO1	Output voltage	LDO1_VSET	3.300 V
	Enable, EN-pin or I²C register	LDO1_EN_PIN_CTRL	EN-pin
	Control for LDO1	LDO1_EN	High
	Startup delay	LDO1_STARTUP_DELAY	1 ms
	Shutdown delay	LDO1_SHUTDOWN_DELAY	4 ms

Table 2-4 lists the device settings for GPIOs.

Table 2-4. EN, CLKIN, and GPIO Pin Settings

	Description	Bit Name	LP873362-Q1
EN pin	EN pin pulldown resistor enable or disable	EN_PD	Enabled
CLKIN pin	CLKIN or GPO2 mode selection	CLKIN_PIN_SEL	GPO2
	CLKIN pin pulldown resistor enable or disable (applicable for both CLKIN and GPO2 modes.)	CLKIN_PD	Enabled
	Frequency of external clock when connected to CLKIN	EXT_CLK_FREQ	2 MHz
	Enable for the internal PLL. When PLL disabled, internal RC OSC is used	EN_PLL	Not Used
GPO	GPO output type (push-pull or open drain)	GPO_OD	Open-Drain
	Enable, EN-pin or I²C register	GPO_EN_PIN_CTRL	EN-pin
	Control for GPO	GPO_EN	High
	Startup delay	GPO_ STARTUP_ DELAY	0 ms
	Shutdown delay	GPO_ SHUTDOWN_ DELAY	0 ms

Table 2-4. EN, CLKIN, and GPIO Pin Settings (continued)

	Description	Bit Name	LP873362-Q1
GPO2	GPO2 output type (push-pull or open drain)	GPO2_OD	Open-Drain
	Enable, EN-pin or I²C register	GPO2_EN_PIN_CTRL	EN-pin
	Control for GPO2	GPO2_EN	High
	Startup delay	GPO2_ STARTUP_ DELAY	0 ms
	Shutdown delay	GPO2_ SHUTDOWN_ DELAY	0 ms

Table 2-5 lists the device protection settings.

Table 2-5. Protections OTP Settings

	Description	Bit Name	LP873362-Q1
Protections	Thermal warning level (125°C or 137°C)	TDIE_WARN_LEVEL	137°C
	Input overvoltage protection	NA	Enabled

Table 2-6 lists the device settings for interrupts. When an interrupt from an event is unmasked, an interrupt is generated on the nINT pin.

Table 2-6. Interrupt Mask Settings

	Interrupt event	Bit Name	LP873362-Q1
General	PGOOD pin changing active to inactive	PGOOD_INT_MASK	Masked
	Sync clock appears or disappears	SYNC_CLK_MASK	Masked
	Thermal warning	TDIE_WARN_MASK	Unmasked
	Load measurement ready	I_MEAS_MASK	Masked
	Register reset	RESET_REG_MASK	Masked
BUCK0	Buck0 PGood active	BUCK0_PGR_MASK	Masked
	Buck0 PGood inactive	BUCK0_PGF_MASK	Masked
	Buck0 current limit	BUCK0_ILIM_MASK	Masked
BUCK1	Buck1 PGood active	BUCK1_PGR_MASK	Masked
	Buck1 PGood inactive	BUCK1_PGF_MASK	Masked
	Buck1 current limit	BUCK1_ILIM_MASK	Masked

3 Power-up and Power Down Sequence

This section shows the power-up and power-down sequence for the device. The power-up and power-down delays for each rail are shown in Figure 3-1.

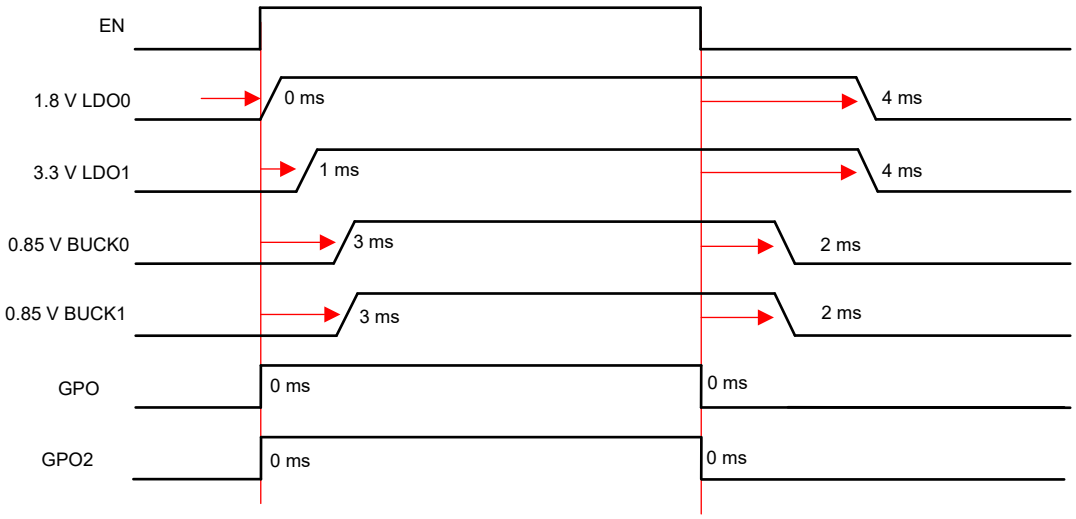

Figure 3-1. LP873362-Q1Power-up and Power Down Sequence

4 Register Bits Loaded From OTP Memory

Table 4-1 lists the register bit values loaded from the OTP memory during device start-up.

Table 4-1. Summary of Control Registers

Address	Register Name	Bit	LP873362-Q1 Value
0x00	DEV_REV	DEVICE_ID[1:0]	02h
0x01	OTP_REV	OTP_ID[7:0]	62h
0x02	BUCK0_CTRL_1	BUCK0_FPWM_MP	01h
0x02	BUCK0_CTRL_1	BUCK0_FPWM	01h
0x02	BUCK0_CTRL_1	BUCK0_EN_PIN_CTRL	01h
0x02	BUCK0_CTRL_1	BUCK0_EN	01h
0x03	BUCK0_CTRL_2	BUCK0_ILIM[2:0]	05h
0x03	BUCK0_CTRL_2	BUCK0_SLEW_RATE[2:0]	04h
0x04	BUCK1_CTRL_1	BUCK1_FPWM	01h
0x04	BUCK1_CTRL_1	BUCK1_EN_PIN_CTRL	01h
0x04	BUCK1_CTRL_1	BUCK1_EN	01h
0x05	BUCK1_CTRL_2	BUCK1_ILIM[2:0]	05h
0x05	BUCK1_CTRL_2	BUCK1_SLEW_RATE[2:0]	04h
0x06	BUCK0_VOUT	BUCK0_VSET[7:0]	2Fh
0x07	BUCK1_VOUT	BUCK1_VSET[7:0]	2Fh
0x0C	BUCK0_DELAY	BUCK0_SHUTDOWN_DELAY[3:0]	04h
0x0C	BUCK0_DELAY	BUCK0_STARTUP_DELAY[3:0]	06h
0x0D	BUCK1_DELAY	BUCK1_SHUTDOWN_DELAY[3:0]	04h
0x0D	BUCK1_DELAY	BUCK1_STARTUP_DELAY[3:0]	06h
0x10	GPO_DELAY	GPO_SHUTDOWN_DELAY[3:0]	00h
0x10	GPO_DELAY	GPO_STARTUP_DELAY[3:0]	00h
0x11	GPO2_DELAY	GPO2_SHUTDOWN_DELAY[3:0]	00h
0x11	GPO2_DELAY	GPO2_STARTUP_DELAY[3:0]	00h
0x12	GPO_CTRL	GPO2_OD	01h
0x12	GPO_CTRL	GPO2_EN_PIN_CTRL	01h
0x12	GPO_CTRL	GPO2_EN	01h
0x12	GPO_CTRL	GPO_OD	01h
0x12	GPO_CTRL	GPO_EN_PIN_CTRL	01h
0x12	GPO_CTRL	GPO_EN	01h
0x13	CONFIG	STARTUP_DELAY_SEL	00h
0x13	CONFIG	SHUTDOWN_DELAY_SEL	00h
0x13	CONFIG	CLKIN_PIN_SEL	00h
0x13	CONFIG	CLKIN_PD	01h
0x13	CONFIG	EN_PD	01h
0x13	CONFIG	TDIE_WARN_LEVEL	01h
0x13	CONFIG	EN_SPREAD_SPEC	00h
0x14	PLL_CTRL	EN_PLL	00h
0x14	PLL_CTRL	EXT_CLK_FREQ[4:0]	01h
0x15	PGOOD_CTRL_1	PGOOD_POL	00h
0x15	PGOOD_CTRL_1	PGOOD_OD	01h
0x15	PGOOD_CTRL_1	PGOOD_WINDOW_BUCK	01h
0x15	PGOOD_CTRL_1	EN_PGOOD_BUCK1	01h
0x15	PGOOD_CTRL_1	EN_PGOOD_BUCK0	01h
0x16	PGOOD_CTRL_2	EN_PGOOD_TWARN	00h
0x16	PGOOD_CTRL_2	PG_FAULT_GATES_PGOOD	00h
0x16	PGOOD_CTRL_2	PGOOD_MODE	00h
0x20	TOP_MASK_1	PGOOD_INT_MASK	01h
0x20	TOP_MASK_1	SYNC_CLK_MASK	01h

Table 4-1. Summary of Control Registers (continued)

Address	Register Name	Bit	LP873362-Q1 Value
0x20	TOP_MASK_1	TDIE_WARN_MASK	00h
0x20	TOP_MASK_1	I_MEAS_MASK	01h
0x21	TOP_MASK_2	RESET_REG_MASK	01h
0x22	BUCK_MASK	BUCK1_PGF_MASK	01h
0x22	BUCK_MASK	BUCK1_PGR_MASK	01h
0x22	BUCK_MASK	BUCK1_ILIM_MASK	01h
0x22	BUCK_MASK	BUCK0_PGF_MASK	01h
0x22	BUCK_MASK	BUCK0_PGR_MASK	01h
0x22	BUCK_MASK	BUCK0_ILIM_MASK	01h

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2025	*	Initial Release

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