EVM User's Guide: LM5126AEVM-BST

LM5126AEVM-BST Evaluation Module

Description

The LM5126AEVM-BST evaluation module showcases the features and performance of the LM5126A-Q1 wide input voltage synchronous boost controller. This EVM is designed for ease of configuration, enabling the user to evaluate different conditions on the module. The standard configuration is designed to provide a 24V/150W output. The output voltage can be dynamically adjusted via ATRK/DTRK pin.

Get Started

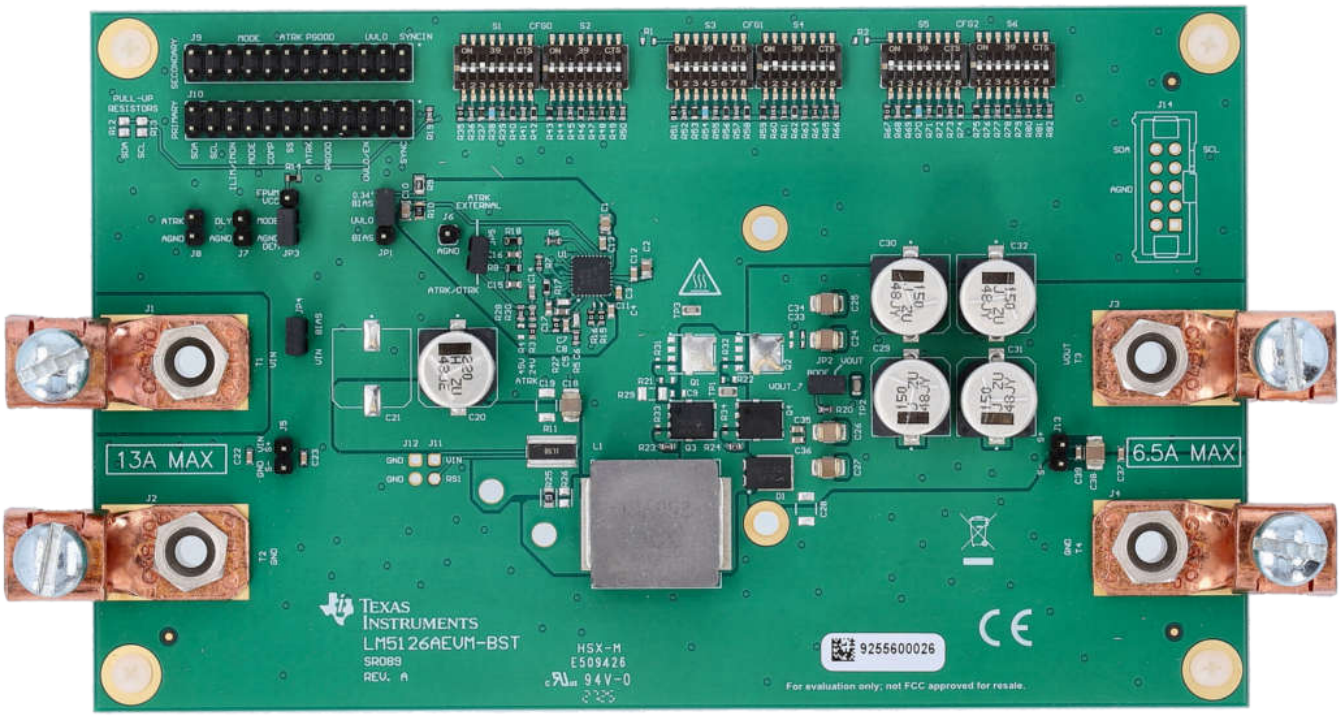
1. Set the jumpers and DIP switches properly
2. Connect EVM to power supply and load

Features

- Single-phase boost controller
- Output voltage tracking from analog/PWM
- Bypass mode
- Optional dual random spread spectrum (DRSS)
- Programmable undervoltage lockout (UVLO),Soft-start and deadtime
- Comprehensive fault protections
  - Peak current limit
  - Average current limit
  - Over voltage protection
- Stackable with LM5125AEVM-BST

Applications

- Automotive Class H audio power amplifier
- Automotive LED headlight applications



1 Evaluation Module Overview

1.1 Introduction

The LM5126AEVM-BST evaluation module provides a fully functional single phase synchronous boost converter to evaluate LM5126A-Q1. The EVM operates over an input voltage range of 9V to 18V and can handle input transients up to 42V. The EVM provides an output voltage of 24V with 150W rated power and 500W peak power. The output voltage is adjustable up to 45V via ATRK/DTRK pin. The LM5126AEVM-BST evaluation module can be stacked with a LM5125AEVM-BST evaluation module for 3-phase operation.

1.2 Kit Contents

- One LM5126AEVM-BST PCB assembly
- EVM Disclaimer Read Me

1.3 Specification

Table 1-1. EVM Specification

Parameter	Condition	MIN	TYP	MAX	UNIT
Input Voltage	Operation	9	14.4	18	V
Output Voltage	R_{ATRK} = 40.2kΩ		24		V
	R_{ATRK} = 75kΩ		45		V
Rated Output Power	V_{in} = 14.4V		150		W
Peak Output Power, 100ms	V_{in} = 14.4V		500		W
Switching frequency			400		kHz
Efficiency	V_{in} = 14.4V, V_{OUT} = 24V, P_{out}=300W		97.5		%
	V_{in} = 14.4V, V_{OUT} = 45V, P_{out}=300W		95.7		%

1.4 Device Information

The LM5126A-Q1 is a synchronous boost controller with the below features:

- Wide input voltage range from 2.5V to 42V
- Programmable output voltage 6V to 60V
- Dynamic output voltage tracking
- Bypass mode
- Programmable OVP
- Cycle by cycle peak current limit
- Inductor current monitor
- Average input current limit
- Selectable dead time
- Stackable for 3phase operation

2 Hardware

2.1 Connector, Jumper, DIP switch and Test point Description

The connectors, jumpers, DIP switches and test points of the EVM are introduced in this section.

2.1.1 Connector Descriptions

Table 2-1. Connectors

Connector	Pin	Description
J1/T1	VIN	Positive power input for the evaluation module
J2/T2	GND	Negative power input for the evaluation module
J3/T3	VOUT	Positive power output for the evaluation module
J4/T4	GND	Negative power output for the evaluation module
J5	1	Input voltage sensing VIN
	2	Input voltage sensing GND
J13	1	Output voltage sensing VOUT
	2	Output voltage sensing GND

2.1.2 Jumper Descriptions

Table 2-2. Jumper Descriptions

Connector	Pins	Description	Default Connection
JP1	1, 2	UVLO/EN pin connected to VIN resistor divider	Y
	2, 3	UVLO/EN pin connected to BIAS	
JP2	1, 2	Injection signal input for bode plot measurements	Y
JP3	1, 2	Set to FPWM	
	2, 3	Set to DEM	Y
JP4	1, 2	BIAS pin connected to VIN	Y
JP5	1, 2	RC filter from J8 connected to ATRK/DTRK pin.	Y
J7	1, 2	DLY pin	
J8	1,2	Input to ATRK/DTRK pin. RC filter is inserted.	
J9	1	SYNCIN to the secondary EVM	
	3	No Connection	
	5	UVLO/EN to the secondary EVM	
	7	EN2 to the secondary EVM	
	9	PGOOD to the secondary EVM	
	11	ATRK/DTRK to the secondary EVM	
	13	SS to the secondary EVM	
	15	COMP to the secondary EVM	
	17	MODE to the secondary EVM	
	19	ILIM/IMON to the secondary EVM	
	21	SCL to the secondary EVM	
	23	SDA to the secondary EVM	
	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24	GND	

Table 2-2. Jumper Descriptions (continued)

Connector	Pins	Description	Default Connection
J10	1	SYNCOUT from the primary EVM	
	3	No Connection	
	5	UVLO/EN from the primary EVM	
	7	EN2 from the primary EVM	
	9	PGOOD from the primary EVM	
	11	ATRK/DTRK from the primary EVM	
	13	SS from the primary EVM	
	15	COMP from the primary EVM	
	17	MODE from the primary EVM	
	19	ILIM/IMON from the primary EVM	
	21	SCL to the primary EVM	
	23	SDA to the primary EVM	
	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24	GND	
J13	10-pin header	Connector for I^2C operation	

2.1.3 DIP Switch Descriptions

The CFG0 pin defines the deadtime and the ATRK/DTRK pin 20µA current source for V_{OUT} programming.

Table 2-3. CFG0 Pin Settings

Level	Deadtime [ns]	20µA ATRK Current
1	18	on
2	30	on
3	50	on
4	75	on
5	100	on
6	125	on
7	150	on
8	200	on
9	18	off
10	30	off
11	50	off
12	75	off
13	100	off
14	125	off
15	150	off
16	200	off

The CFG1 pin setting defines the V_{OUT} Over Voltage Protection level, Clock Dithering, the 120% input current limit protection (I_{CL_latch}) operation and the power good pin behavior.

Table 2-4. CFG1 Pin Settings

Level	OVP Bit 0	Clock Dithering Mode	I_{CL_latch}	$PGOOD_{OVP\_enable}$
1	0	enabled (DRSS)	disabled	disabled
2	1	enabled (DRSS)	disabled	disabled
3	0	enabled (DRSS)	disabled	enabled
4	1	enabled (DRSS)	disabled	enabled
5	0	enabled (DRSS)	enabled	disabled

Table 2-4. CFG1 Pin Settings (continued)

Level	OVP Bit 0	Clock Dithering Mode	I_{CL_latch}	$PGOOD_{OVP\_enable}$
6	1	enabled (DRSS)	enabled	disabled
7	0	enabled (DRSS)	enabled	enabled
8	1	enabled (DRSS)	enabled	enabled
9	0	disabled	disabled	disabled
10	1	disabled	disabled	disabled
11	0	disabled	disabled	enabled
12	1	disabled	disabled	enabled
13	0	disabled	enabled	disabled
14	1	disabled	enabled	disabled
15	0	disabled	enabled	enabled
16	1	disabled	enabled	enabled

The CFG2 pin defines the V_{OUT} Over Voltage Protection level, if the device uses the internal clock generator or an external clock applied at the SYNCIN pin. The CFG2 pin also configures if the device is a single device or part of a dual device configuration, the SYNCIN and SYNCOUT pin is enabled/disabled accordingly. During clock synchronization the clock dither function is disabled.

Table 2-5. CFG2 Pin Settings

Level	OVP bit 1	Single / Dual Chip	Phase 2 Phase Shift	SYNCIN	SYNCOUT	SYNCOUT Phase Shift	Clock Dithering
1	0	single	180°	off	off	off	CFG1 pin
2	1						
3	0						
4	1	single ext. clock	180°	on	off	off	disabled
5	0						
6	1						
7	0	primary 3-phase	240°	off	on	120°	CFG1 pin
8	1						
9	0	primary 4-phase	180°	off	on	90°	CFG1 pin
10	1						
11	0	primary ext. clock 3-phase	240°	on	on	120°	disabled
12	1						
13	0	primary ext. clock 4-phase	180°	on	on	90°	disabled
14	1						
15	0	secondary	180°	on	off	off	disabled
16	1						

S1 through S6 are 8-bit DIP switches.

- S1 and S2 are for CFG0
  - S1-postion 1 selects Level 1, …, S1-postion 8 selects Level 8
  - S2-postion 1 selects Level 9, …, S2-postion 8 selects Level 16
- S3 and S4 are for CFG1
  - S3-postion 1 selects Level 1, …, S3-postion 8 selects Level 8
  - S4-postion 1 selects Level 9, …, S4-postion 8 selects Level 16
- S5 and S6 are for CFG2
  - S5-postion 1 selects Level 1, …, S5-postion 8 selects Level 8
  - S6-postion 1 selects Level 9, …, S6-postion 8 selects Level 16

Select position 3 for S1 by default to set Level 3 for CFG0:

- Deadtime = 50ns
- 20µA ATRK current source = on

Note

The EVM is susceptible to damage if lower than 50ns deadtime is selected.

Select position 2 for S4 by default to set Level 10 for CFG1:

- OVP bit 0 = 1
- DRSS = disabled
- I_{CL_latch} = disabled
- $PGOOD_{OVP\_enable}$ = disabled

Select position 1 for S5 by default to set Level 1 for CFG2:

- OVP bit 1 = 0
- Single chip
- Phase shift = 180°
- SYNCIN = off
- SYNCOUT = off

2.1.4 Test Points Description

Table 2-6. Test Points Description

Test Point	Name	Description
TP1	SW	Test point for switch node
TP2	GND	Test point for GND
TP3	GND	Test point for GND

3 Easy to Use Features

Output Voltage Tracking

Connect analog tracking voltage signal to J8. A high frequency PWM signal is also acceptable because a two-stage RC filter is inserted.

Set V_{out} to 45V

- Populate R3=0Ω to set V_{out} to 24V (default)
- Populate R4=0Ω to set V_{out} to 45V

Refer to Figure 3-1.

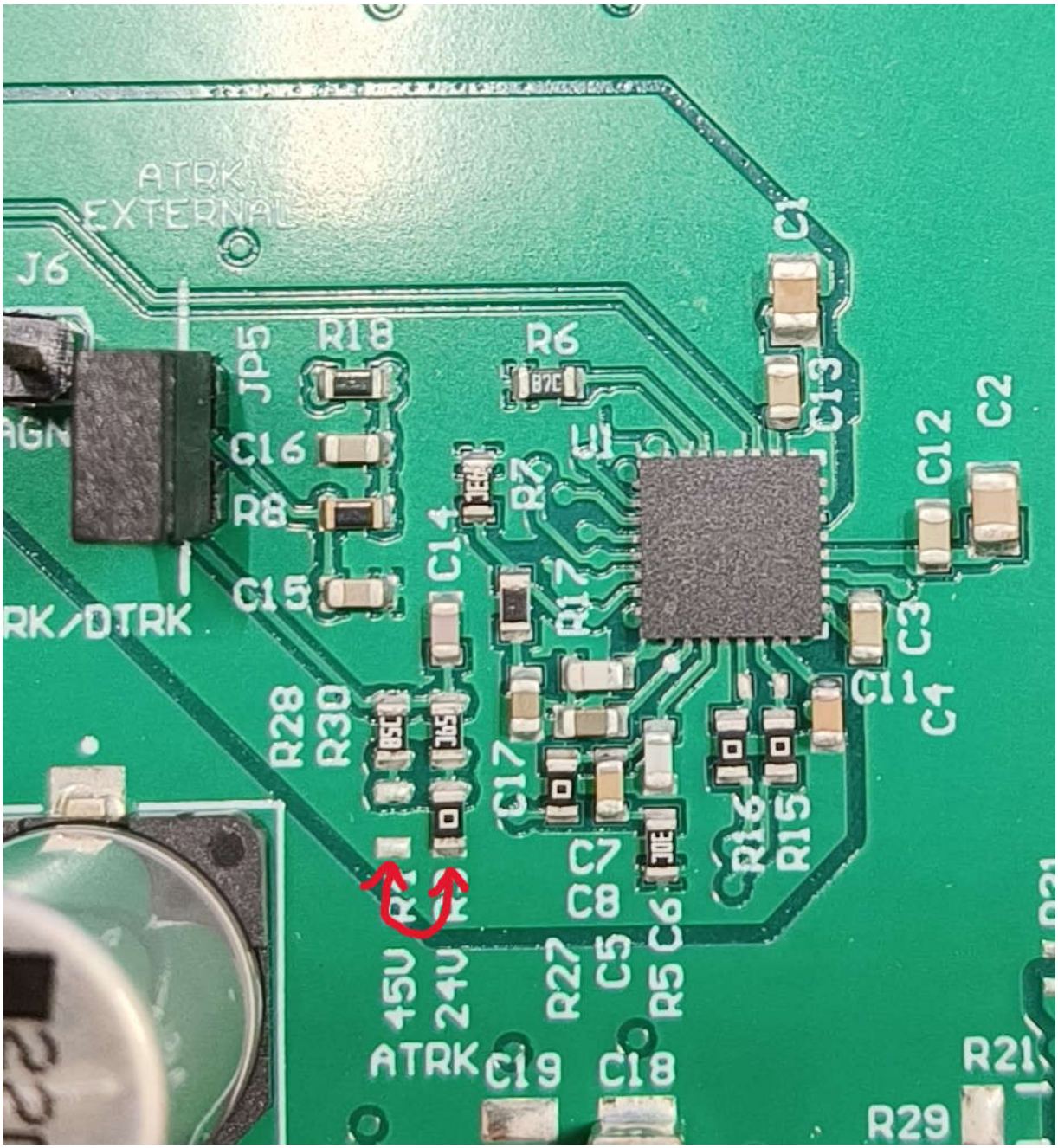


Figure 3-1. Select Between 24V and 45V

Observe the inductor current with current probe

Remove R25 and solder a wire in the plated through holes to observe the current through the inductor. Refer to Figure 3-2.

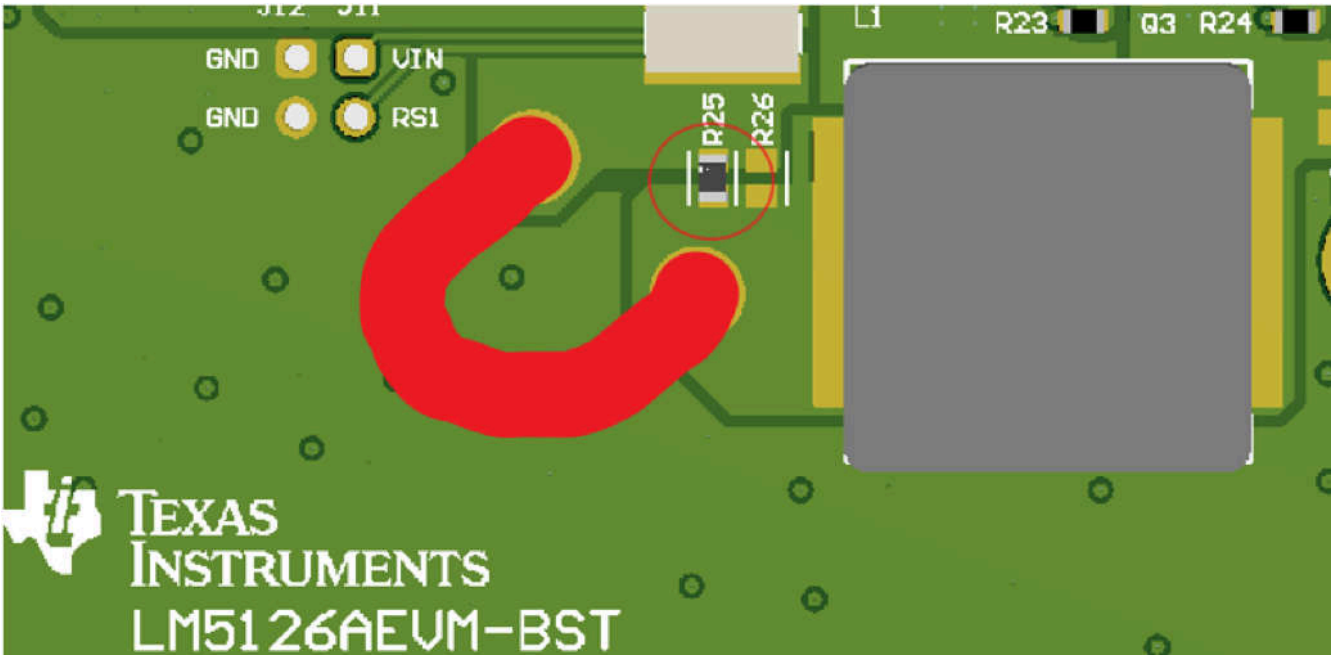


Figure 3-2. Observe the Inductor Current

4 Implementation Results

4.1 Test Setup and Procedure

4.1.1 Test Setup

Figure 4-1 shows the required test setup to evaluate the EVM.

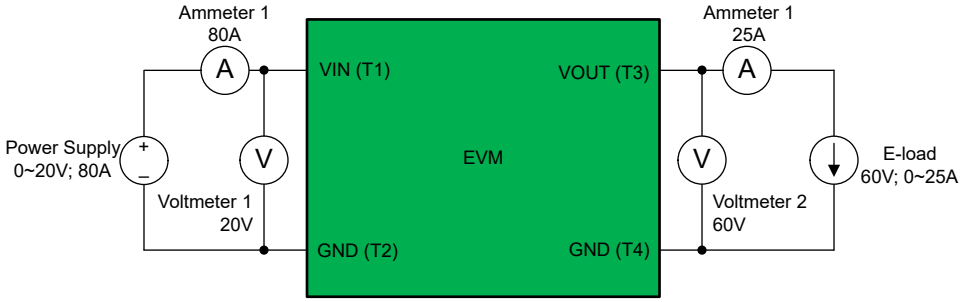


Figure 4-1. EVM Test Setup

The following test equipment is needed:

- Power supply: The power supply needs to support 20V/80A.
- Electronic load: The electronic load needs to sink 500W at 60V.
- Multimeters (optional)
  - Voltmeter 1 (V_{IN}): Capable of measuring input voltage of 20V
  - Voltmeter 2 (V_{OUT}): Capable of measuring output voltage of 60V
  - Ammeter 1 (I_{IN}): Capable of 80A DC measurement.
  - Ammeter 2 (I_{OUT}): Capable of 25A DC measurement
- Oscilloscope: Minimum 200MHz bandwidth

4.1.2 Test Setup for Stacking 2 EVMs

1. Connect VIN, VOUT, GND from two EVMs together with short, thick cables, respectively.
2. Select CFG2=Level 7 for the primary (LM5125AEVM-BST) for 3-phase interleaving operation.
3. Select CFG2=Level 15 for the secondary EVM.
4. Connect J10 of the primary EVM and J9 of the secondary EVM with ribbon cable. Refer to Figure 4-2.

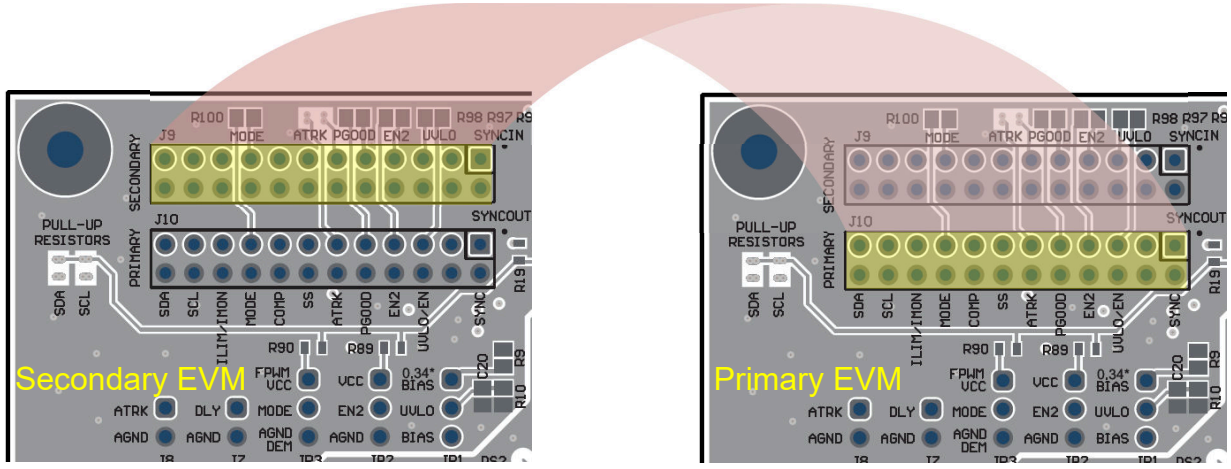


Figure 4-2. Connecting the Primary EVM and Secondary EVM with Ribbon Cable

4.1.3 Test Procedure

1. Make sure the jumpers and DIP switches are set properly.
2. Prepare the setup following Figure 4-1.
3. Set the power supply voltage to 14.4V and the electronic load to 0.1A. The electronic load voltage must be in regulation with a nominal 24V output.
4. Change the load and input voltage as required.

4.1.4 Precautions

	Caution	Caution Hot surface. Contact can cause burns. Do not touch!

5 Application Curves

5.1 Efficiency

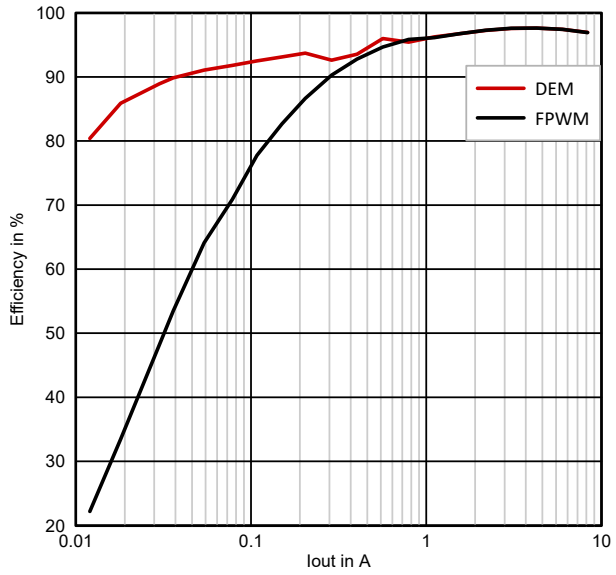


Figure 5-1. Efficiency vs. Output Current, V_{in} = 14.4V, V_{out} = 24V

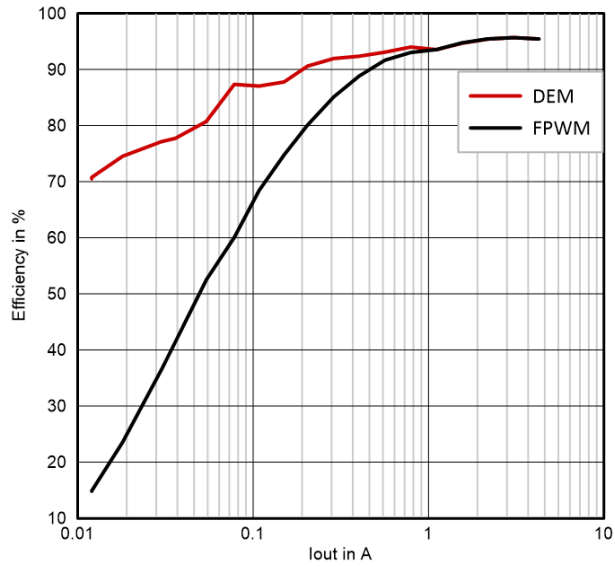


Figure 5-2. Efficiency vs. Output Current, V_{in} = 14.4V, V_{out} = 45V

5.2 Steady State Waveforms

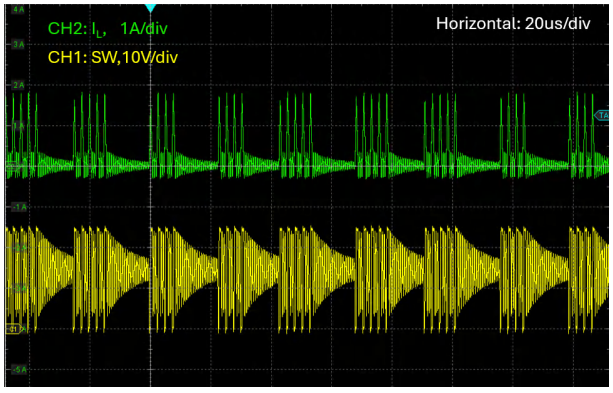


Figure 5-3. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load}= 0.1A

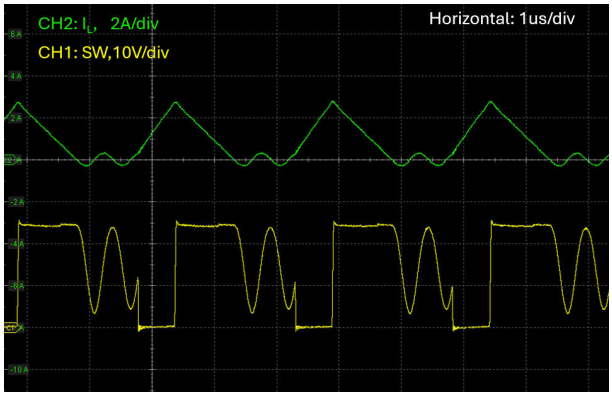


Figure 5-4. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load}= 0.5A

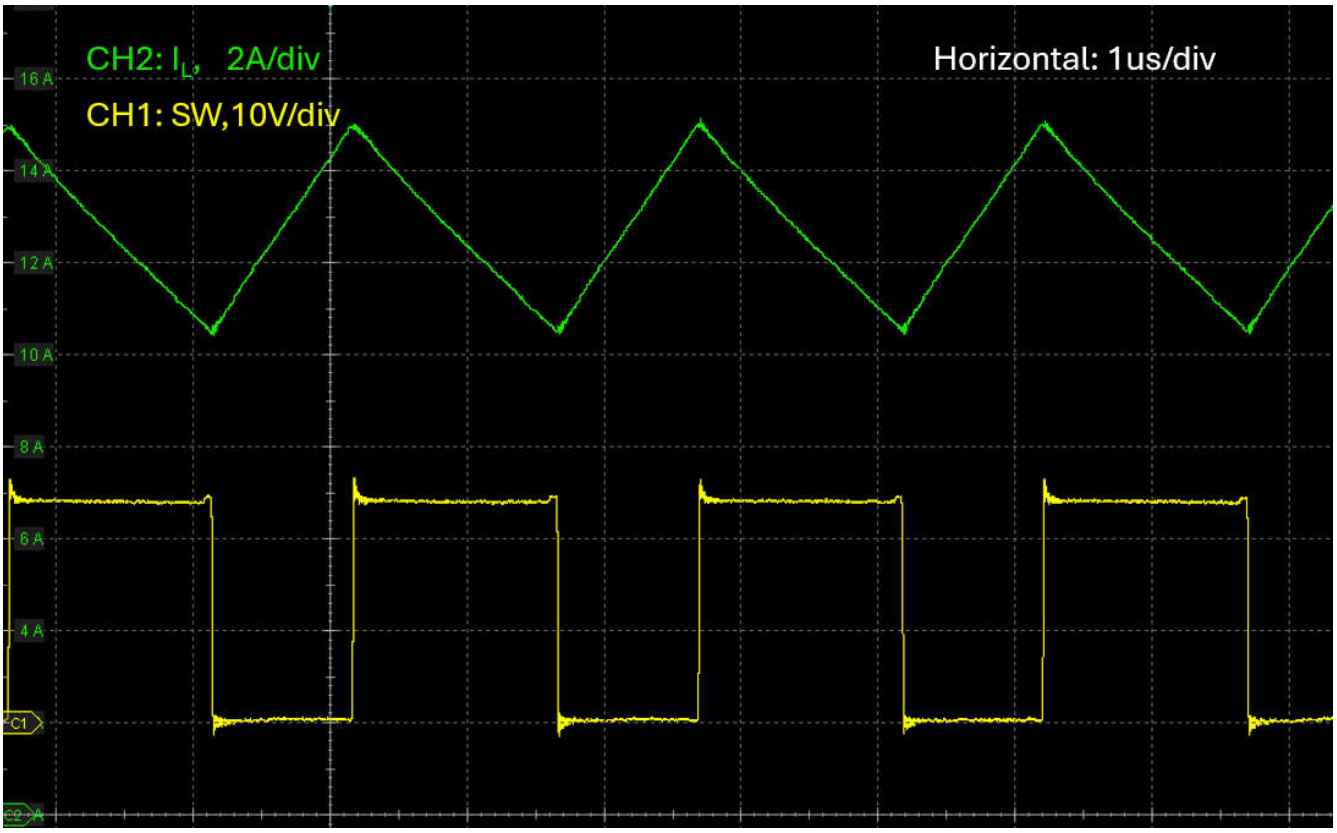


Figure 5-5. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load}= 7.5A

5.3 Step Load Response

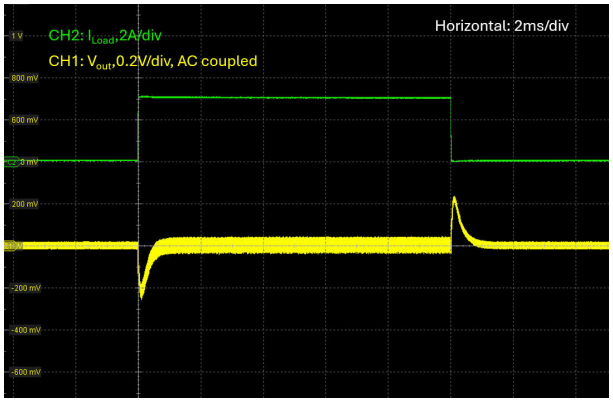


Figure 5-6. Load Transient, V_{in} = 14.4V, V_{out} = 24V, FPWM, I_{load} = 0A to 3.125A at 1A/µs

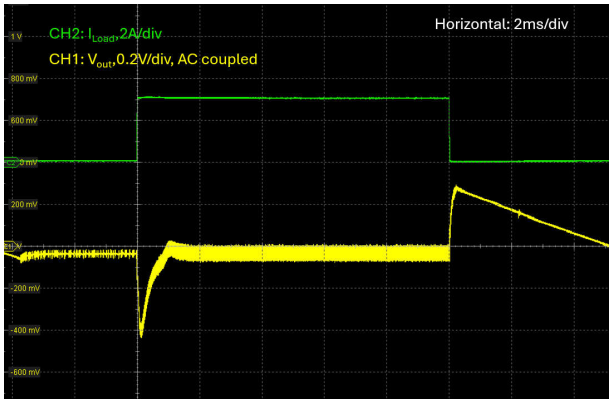


Figure 5-7. Load Transient, V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load} = 0A to 3.125A at 1A/µs

5.4 AC Loop Response Curve

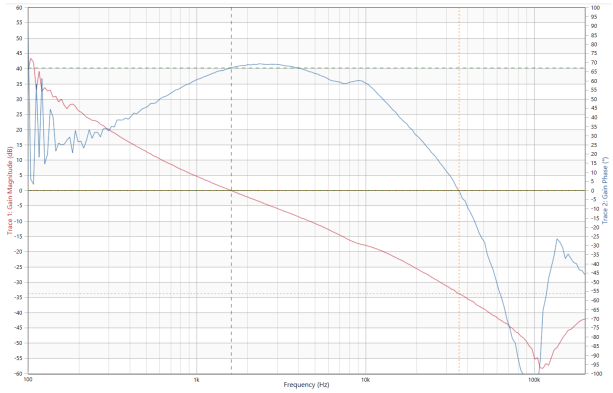


Figure 5-8. Bode Plot, Vin=14.4V, Vout=45V, Iout=3.4A (Average Current Loop Disabled)

5.5 Thermal Performance

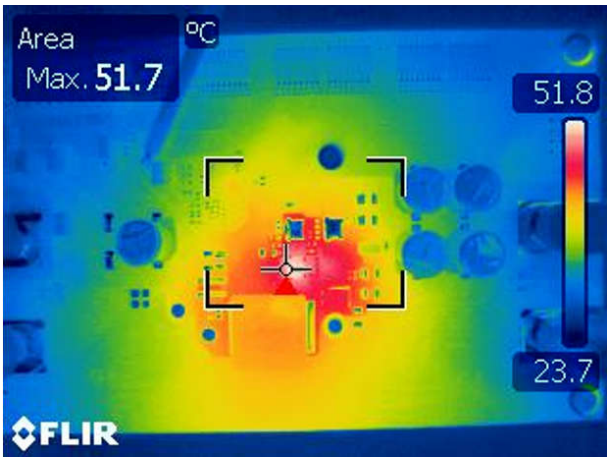


Figure 5-9. V_{in} = 14.4V, V_{out} = 24V, P_{OUT} = 150W, Natural Convection

Figure 5-10. V_{in} = 14.4V, V_{out} = 45V, P_{OUT} = 150W, Natural Convection

6 Hardware Design Files

6.1 Schematic

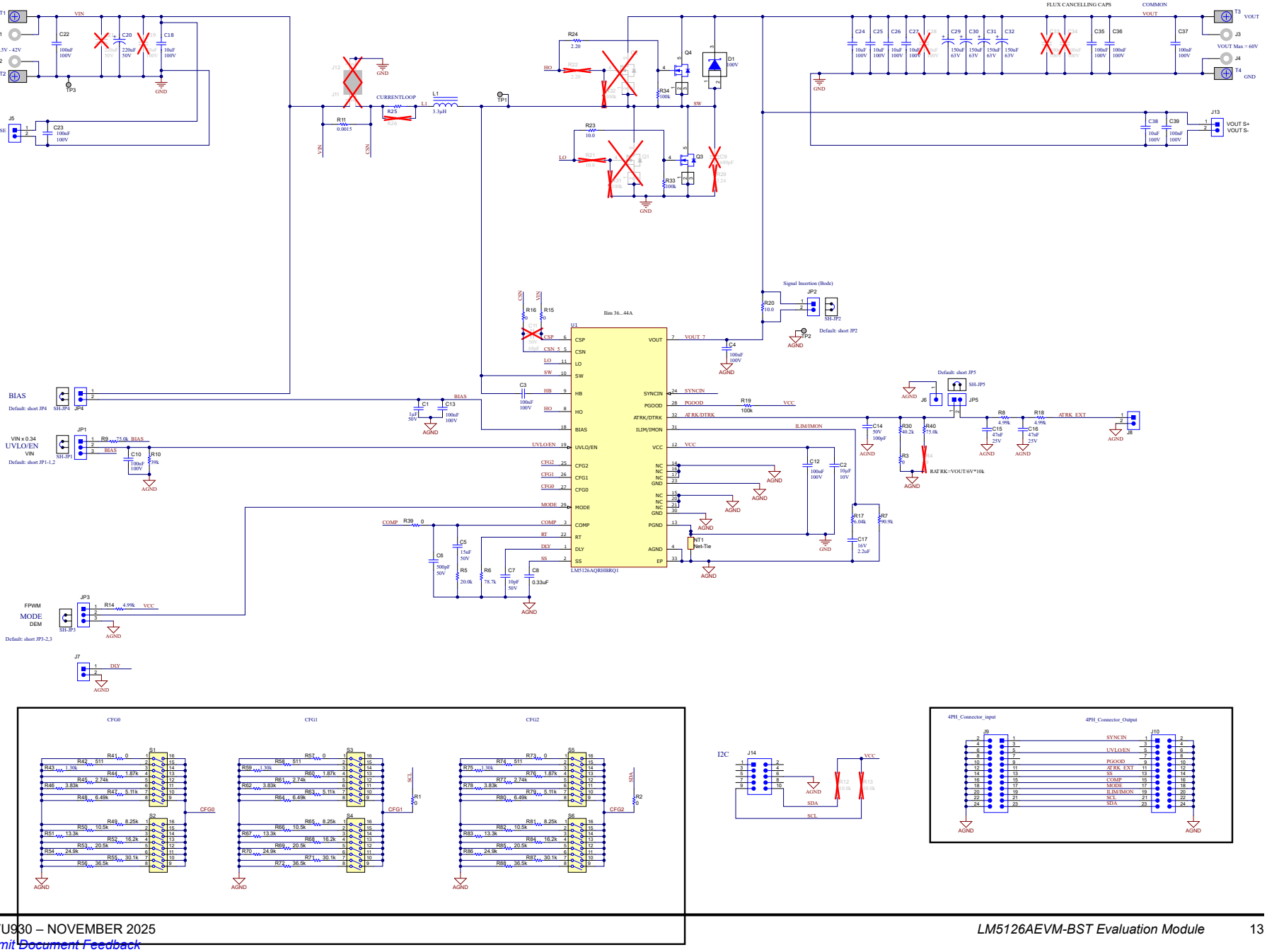


Figure 6-1. Schematic

6.2 PCB Layers

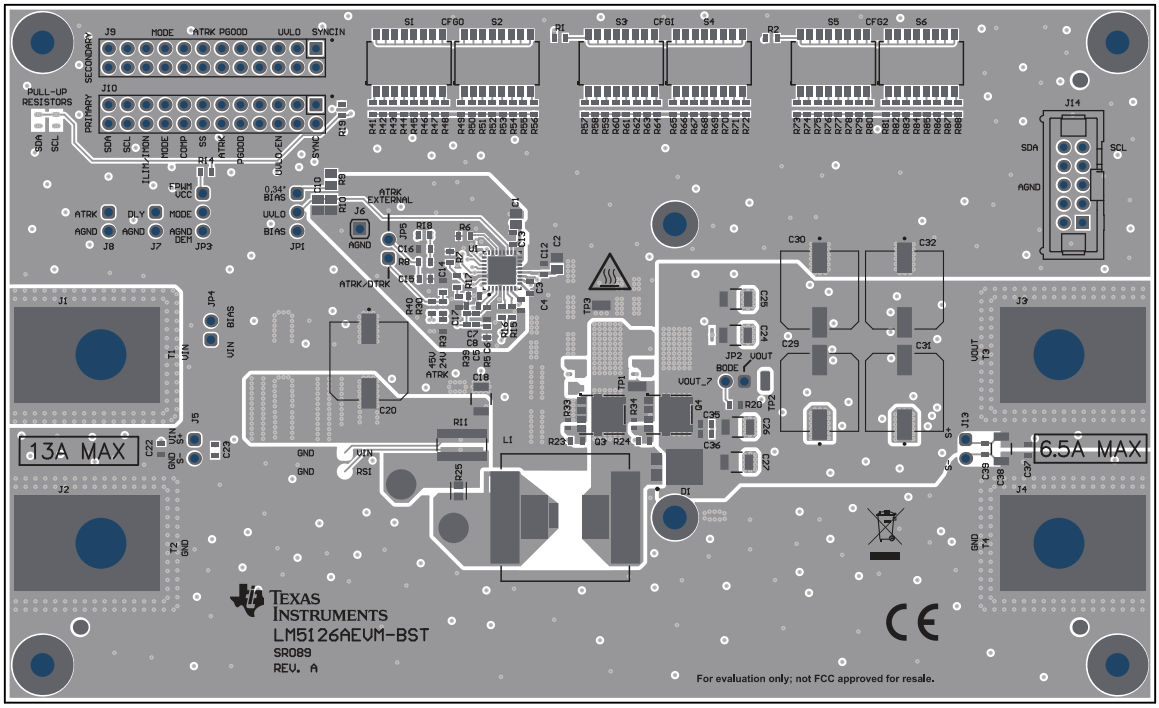


Figure 6-2. Top Silk Screen

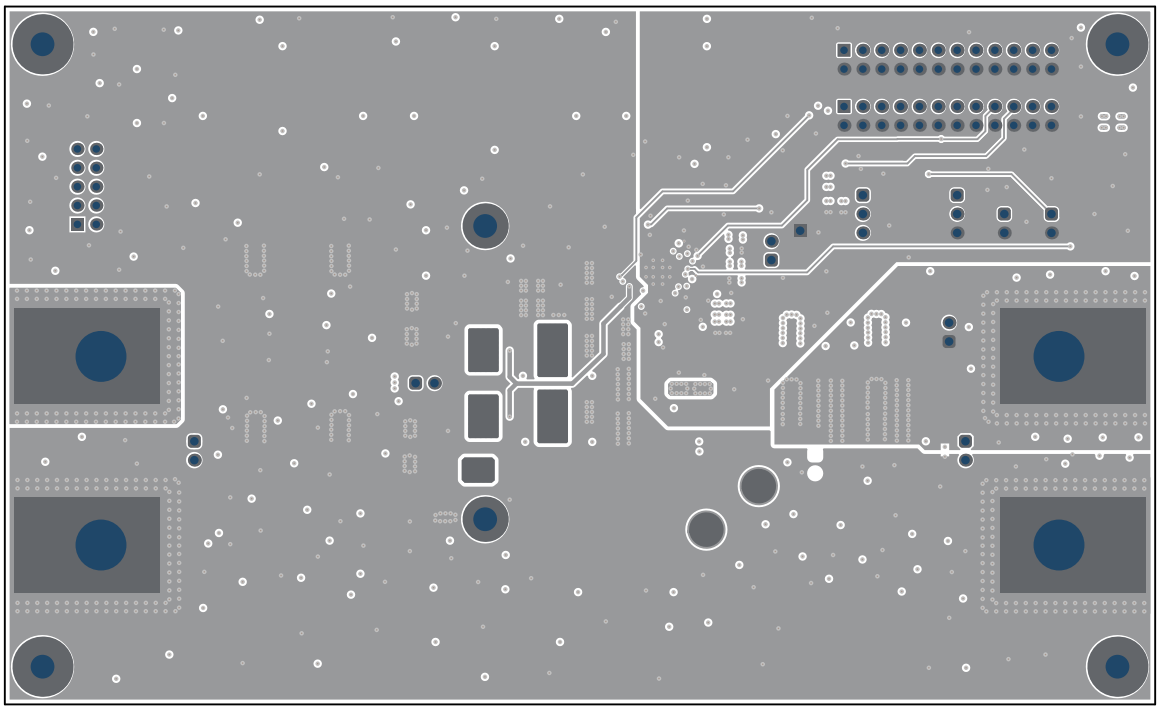


Figure 6-3. Bottom Silk Screen

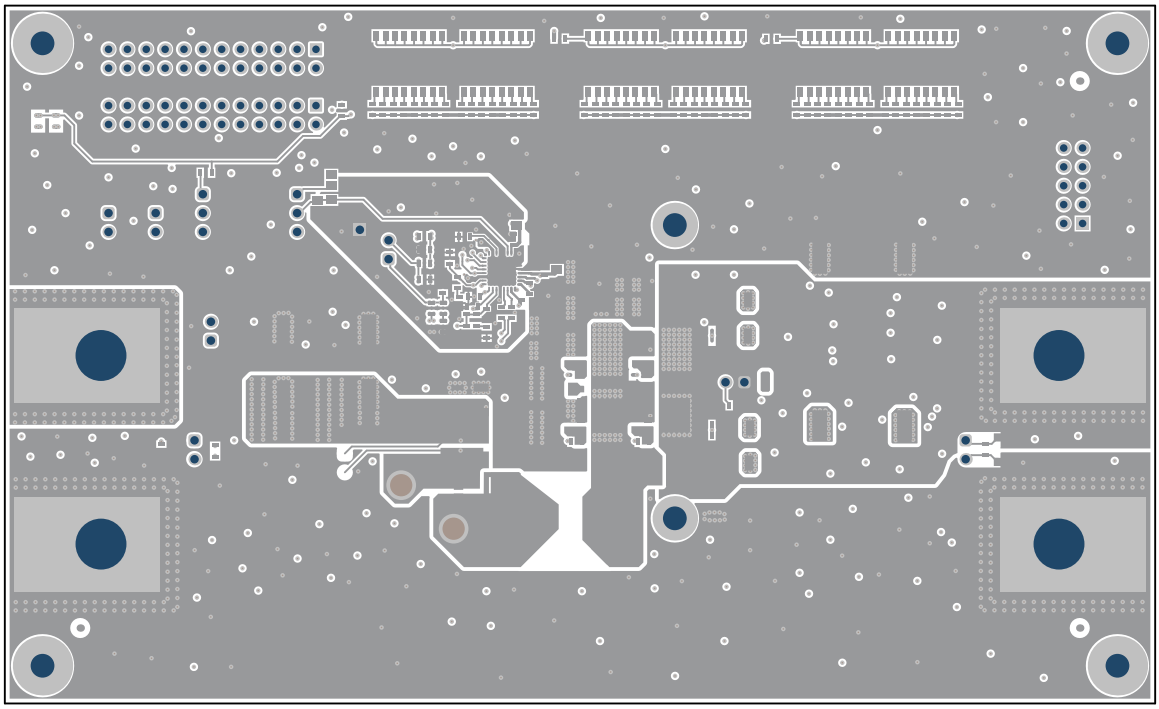


Figure 6-4. Top Layer

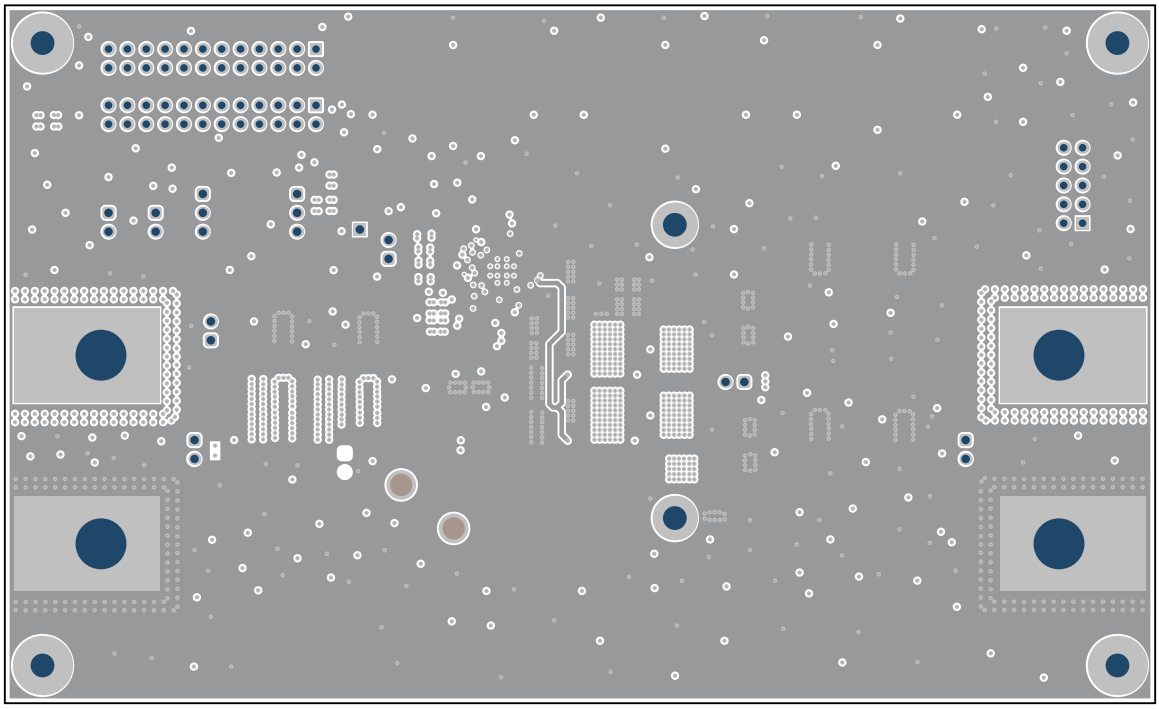


Figure 6-5. Signal Layer 1

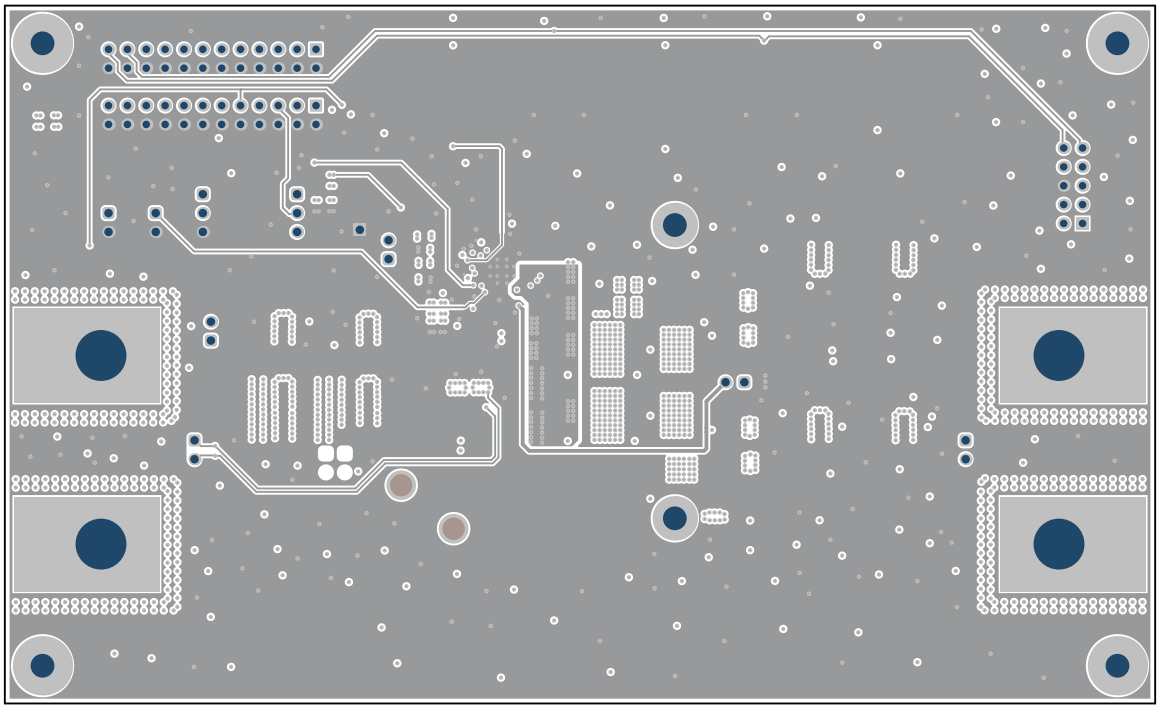


Figure 6-6. Signal Layer 2

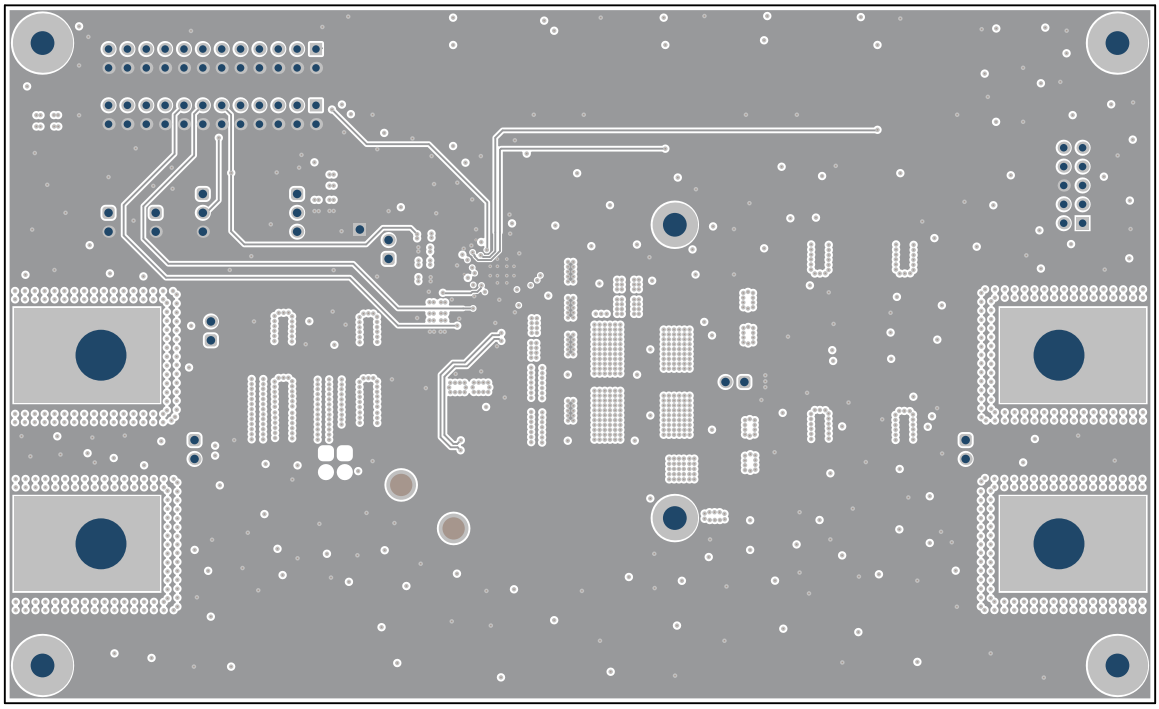


Figure 6-7. Signal Layer 3

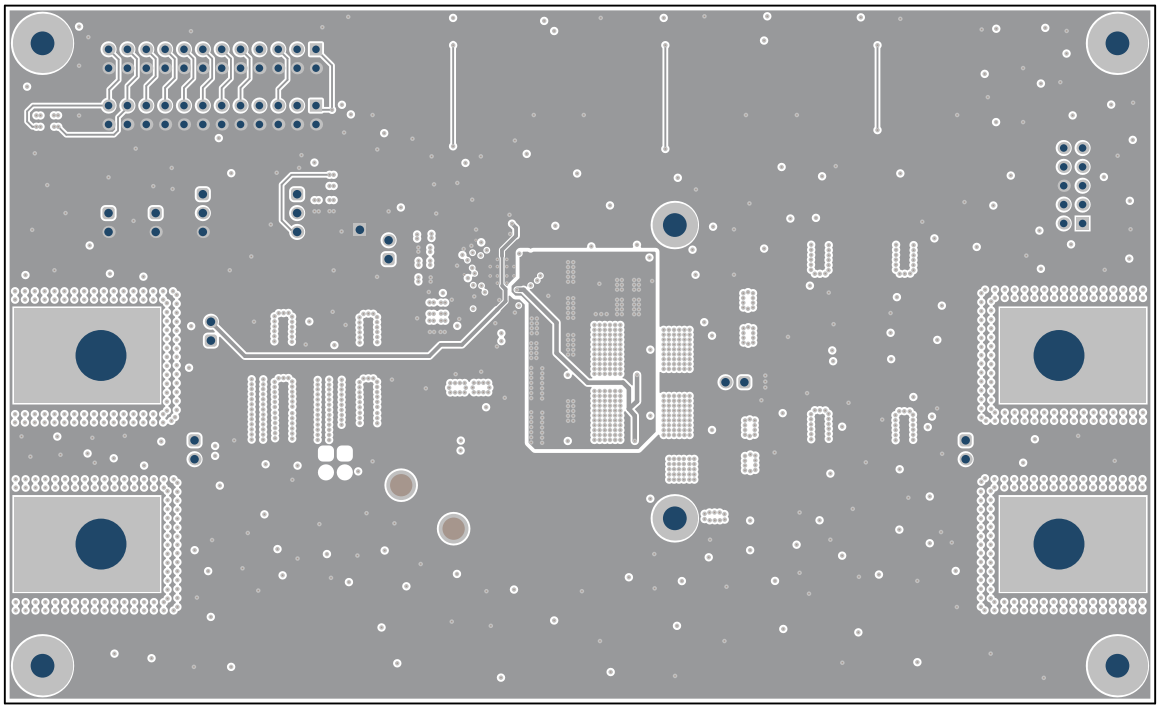


Figure 6-8. Signal Layer 4

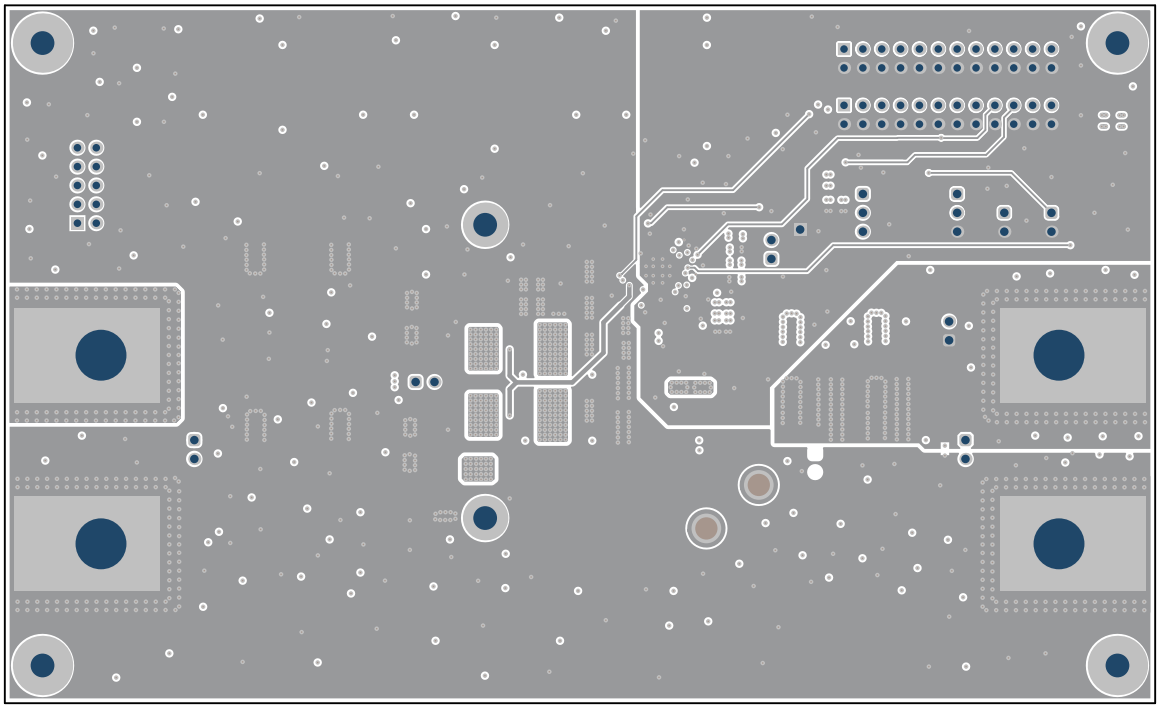


Figure 6-9. Bottom Layer

6.3 Bill of Materials

Table 6-1. Bill of Materials

Designator	Quantity	Value	Part Number	Manufacturer	Description
C1	1	1uF	GCM21BR71H105KA03K	MuRata	CAP, CERM, 1µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805
C2	1	10uF	GCJ21BR71A106KE01L	MuRata	CAP, CERM, 10µF, 10 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805
C3, C4, C12, C13, C22, C23, C35, C36, C37, C39	10	0.1uF	GRM188R72A104KA35D	MuRata	CAP, CERM, 0.1uF, 100 V, +/- 10%, X7R, 0603
C5	1	0.015uF	GRM188R71H153KA01D	MuRata	CAP, CERM, 0.015uF, 50V, +/- 10%, X7R, 0603
C6	1	500pF	CC0603JRNPO9BN501	Yageo America	CAP, CERM, 500pF, 50 V, +/- 5%, C0G/NP0, 0603
C7	1	10pF	GRM1885C1H100JA01D	MuRata	CAP, CERM, 10pF, 50 V, +/- 5%, C0G/NP0, 0603
C8	1	0.33uF	C0603C334K8PACTU	Kemet	CAP, CERM, 0.33uF, 10 V, +/- 10%, X5R, 0603
C10	1	0.1uF	CGA4J2X7R2A104K125AA	TDK	CAP, CERM, 0.1uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805
C14	1	100pF	GRM1885C1H101JA01D	MuRata	CAP, CERM, 100pF, 50 V, +/- 5%, C0G/NP0, 0603
C15, C16	2	0.047uF	GCM188R71E473KA37D	MuRata	CAP, CERM, 0.047uF, 25V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603
C17	1	2.2uF	8.85012E+11	Wurth Elektronik	CAP, CERM, 2.2uF, 16 V, +/- 20%, X5R, 0603
C18, C24, C25, C26, C27, C38	6		GRM32EC72A106KE05L	Murata	10µF ±10% 100V Ceramic Capacitor X7S 1210 (3225 Metric)
C20	1	220µF	EEHZU1H221P	Panasonic	Aluminum Hybrid Polymer Capacitors 220uF 20% 50V Life 4000Hours AEC-Q200 RADIAL SMT

Table 6-1. Bill of Materials (continued)

Designator	Quantity	Value	Part Number	Manufacturer	Description
C29, C30, C31, C32	4	150µF	EEHZU1J151P	Panasonic	Aluminum Hybrid Polymer Capacitors 150uF 20% 63V Life 4000Hours AEC-Q200 RADIAL SMT
D1	1	100V	V12P10M3/86A	Vishay-Semiconductor	Diode, Schottky, 100 V, 12A, AEC-Q101, TO-277A
J1, J2, J3, J4	4		108-0740-001	Cinch Connectivity	Standard Banana Jack, Uninsulated, 15A
J5, J7, J8, J13, JP2, JP4, JP5	7		61300211121	Wurth Elektronik	Header, 2.54mm, 2x1, Gold, TH
J6	1		61300111121	Wurth Elektronik	Header, 2.54mm, 1x1, Gold, TH
J9, J10	2		TSW-112-07G-D	Samtec	Header, 100mil, 12x2, Gold, TH
J14	1		N2510-6002-RB	3M	Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH
JP1, JP3	2		61300311121	Wurth Elektronik	Header, 2.54mm, 3x1, Gold, TH
L1	1	3.3uH	IHLP6767GZER3R3M5A	Vishay-Dale	Inductor, Shielded, 3.3µH, 32.2A, 0.00327ohm, AEC-Q200 Grade 0, SMD
Q3, Q4	2	60V	NTMFS5C670NLT1G	ON Semiconductor	MOSFET, N-CH, 60V, 71 A, SO-8FL
R1, R2, R3, R15, R16, R41, R57, R73	8	0	RMCF0603ZT0R00	Stackpole Electronics Inc	RES, 0, 1%, 0.1W, AEC-Q200 Grade 0, 0603
R5	1	20.0k	CRCW060320K0FKEA	Vishay-Dale	RES, 20.0k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R6	1	78.7k	RT0603BRD0778K7L	Yageo America	RES, 78.7k, 0.1%, 0.1 W, 0603
R7	1	90.9k	CRCW060390K9FKEA	Vishay-Dale	RES, 90.9k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R8, R14, R18	3	4.99k	CRCW06034K99FKEA	Vishay-Dale	RES, 4.99k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603

Table 6-1. Bill of Materials (continued)

Designator	Quantity	Value	Part Number	Manufacturer	Description
R9	1	75.0k	CRCW080575K0FKEA	Vishay-Dale	RES, 75.0k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805
R10	1	39k	CRCW080539K0JNEA	Vishay-Dale	RES, 39k, 5%, 0.125 W, AEC-Q200 Grade 0, 0805
R11	1	0.0015	PML100HZPJV1L5	Rohm	RES, 0.0015, 5%, 2W, 2512 WIDE
R17	1	6.04k	CRCW06036K04FKEA	Vishay-Dale	RES, 6.04k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R19	1	100k	CRCW0603100KFKEA	Vishay-Dale	RES, 100k, 1%, 0.1W, AEC-Q200 Grade 0, 0603
R20, R23	2	10	CRCW060310R0FKEA	Vishay-Dale	RES, 10.0, 1%, 0.1W, AEC-Q200 Grade 0, 0603
R24	1	2.2	ERJ-3RQF2R2V	Panasonic	RES, 2.20, 1%, 0.1W, 0603
R25	1	0	WSL080500000ZEA9	Vishay	0 Ohms Jumper Chip Resistor 0805 (2012 Metric) Metal Element
R30	1	40.2k	CRCW060340K2FKEA	Vishay-Dale	RES, 40.2k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R33, R34	2	100k	CRCW0402100KFKED	Vishay-Dale	RES, 100k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402
R39	1	0	ERJ-3GEY0R00V	Panasonic	RES, 0, 5%, 0.1W, AEC-Q200 Grade 0, 0603
R40	1	75.0k	CRCW060375K0FKEA	Vishay-Dale	RES, 75.0k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R42, R58, R74	3	511	CRCW0603511RFKEA	Vishay-Dale	RES, 511, 1%, 0.1W, AEC-Q200 Grade 0, 0603
R43, R59, R75	3	1.30k	CRCW06031K30FKEA	Vishay-Dale	RES, 1.30k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R44, R60, R76	3	1.87k	CRCW06031K87FKEA	Vishay-Dale	RES, 1.87k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R45, R61, R77	3	2.74k	CRCW06032K74FKEA	Vishay-Dale	RES, 2.74k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603

Table 6-1. Bill of Materials (continued)

Designator	Quantity	Value	Part Number	Manufacturer	Description
R46, R62, R78	3	3.83k	CRCW06033K83FKEA	Vishay-Dale	RES, 3.83k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R47, R63, R79	3	5.11k	CRCW06035K11FKEA	Vishay-Dale	RES, 5.11k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R48, R64, R80	3	6.49k	CRCW06036K49FKEA	Vishay-Dale	RES, 6.49k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R49, R65, R81	3	8.25k	CRCW06038K25FKEA	Vishay-Dale	RES, 8.25k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R50, R66, R82	3	10.5k	CRCW060310K5FKEA	Vishay-Dale	RES, 10.5k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R51, R67, R83	3	13.3k	CRCW060313K3FKEA	Vishay-Dale	RES, 13.3k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R52, R68, R84	3	16.2k	CRCW060316K2FKEA	Vishay-Dale	RES, 16.2k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R53, R69, R85	3	20.5k	CRCW060320K5FKEA	Vishay-Dale	RES, 20.5k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R54, R70, R86	3	24.9k	CRCW060324K9FKEA	Vishay-Dale	RES, 24.9k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R55, R71, R87	3	30.1k	CRCW060330K1FKEA	Vishay-Dale	RES, 30.1k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R56, R72, R88	3	36.5k	CRCW060336K5FKEA	Vishay-Dale	RES, 36.5k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
S1, S2, S3, S4, S5, S6	6		218-8LPST	CTS Electrocomponents	Switch, SPST, 8 Pos, 25mA, 24VDC, SMD
T1, T2, T3, T4	4		CXS70-14C	Panduit	Terminal 70A Lug
TP1, TP2, TP3	3		RCU-0C	TE Connectivity	PC Test Point, SMT
U1	1		LM5126AQRHBRQ1	Texas Instruments	Wide-VIN, 2.2MHz single-phase boost controller with VOUT tracking
C9	0	680pF	C0603C681K5RACTU	Kemet	CAP, CERM, 680pF, 50 V, +/-10%, X7R, 0603
C11	0	68pF	04025A680FAT2A	AVX	CAP, CERM, 68pF, 50 V,+/-1%, C0G/NP0, 0402

Table 6-1. Bill of Materials (continued)

Designator	Quantity	Value	Part Number	Manufacturer	Description
C19, C28	0		GRM32EC72A106KE05L	Murata	10µF ±10% 100V Ceramic Capacitor X7S 1210 (3225 Metric)
C21	0	220µF	EEHZU1H221P	Panasonic	Aluminum Hybrid Polymer Capacitors 220uF 20% 50V Life 4000Hours AEC-Q200 RADIAL SMT
C33, C34	0	0.1uF	GRM188R72A104KA35D	MuRata	CAP, CERM, 0.1uF, 100 V, +/- 10%, X7R, 0603
J11, J12	0		61300211121	Wurth Elektronik	Header, 2.54mm, 2x1, Gold, TH
Q1, Q2	0	60V	NTMFS5C670NLT1G	ON Semiconductor	MOSFET, N-CH, 60V, 71 A, SO-8FL
R4	0	0	RMCF0603ZT0R00	Stackpole Electronics Inc	RES, 0, 1%, 0.1W, AEC-Q200 Grade 0, 0603
R12, R13	0	10.0k	CRCW080510K0FKEA	Vishay-Dale	RES, 10.0k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805
R21	0	10	CRCW060310R0FKEA	Vishay-Dale	RES, 10.0, 1%, 0.1W, AEC-Q200 Grade 0, 0603
R22	0	2.2	ERJ-3RQF2R2V	Panasonic	RES, 2.20, 1%, 0.1W, 0603
R26	0	0	WSL080500000ZEA9	Vishay	0 Ohms Jumper Chip Resistor 0805 (2012 Metric) Metal Element
R29	0	3.24	CRCW12063R24FKEA	Vishay-Dale	RES, 3.24, 1%, 0.25W, AEC-Q200 Grade 0, 1206
R31, R32	0	100k	CRCW0402100KFKED	Vishay-Dale	RES, 100k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402

7 Additional Information

Trademarks

All trademarks are the property of their respective owners.

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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