LP5810 4-Channel RGBW LED Driver Register Map

Technical Reference Manual

Literature Number: SNVU926
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Preface

Read This First

About This Manual

This Technical Reference Manual (TRM) details the register maps of LP5810.

The TRM should not be considered a substitute for the data sheet, rather a companion guide that should be used alongside the device-specific data sheet to understand the details to program the device. The primary purpose of the TRM is to abstract the programming registers of the device from the data manual. This allows the data sheet to outline the high-level features of the device without unnecessary information about register descriptions.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers can be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing nondefault values to the Reserved bits could cause unexpected behavior and should be avoided.

Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

Related Documentation

For a complete listing of related documentation and development-support tools, visit the Texas Instruments website at http://www.ti.com.

SNVSCD0B *LP5810 4-Channel RGBW LED Driver With Autonomous Control* describes the data sheet of the LP5810 device.

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Chapter 1

Introduction/Feature Overview

1.1 Overview

The LP5810 is a 4-Channel RGBW LED driver with autonomous animation engine control. The LP5810 has ultra-low operation current at active mode, consuming 0.4 mA when LED maximum current setting is 25.5 mA. If all LEDs are turned off, the device enters standby state to reduce power consumption with data retained. When 'chip_enable' bit setting is 0, initial state is entered with minimum power consumption to save power.

The LP5810 supports both analog dimming and PWM dimming. In analog dimming, the output current of each LED can be adjusted with 256 steps. In PWM dimming, the integrated 8-bit configurable PWM generator enables smooth brightness dimming control. Optional exponential PWM dimming can be activated for individual LED to achieve a human-eye-friendly visual performance.

The LP5810 integrates autonomous animation engine, with no need for brightness control commands from controller. Each LED has an individual animation engine which can be configured through the related registers. The device can generate a 6 MHz clock signal, which synchronizes the lighting effects among multiple devices.

The LP5810 has 4 different material versions with different I2C chip address. Up to 4 LP581x devices can be connected to the same I2C bus and controlled individually.

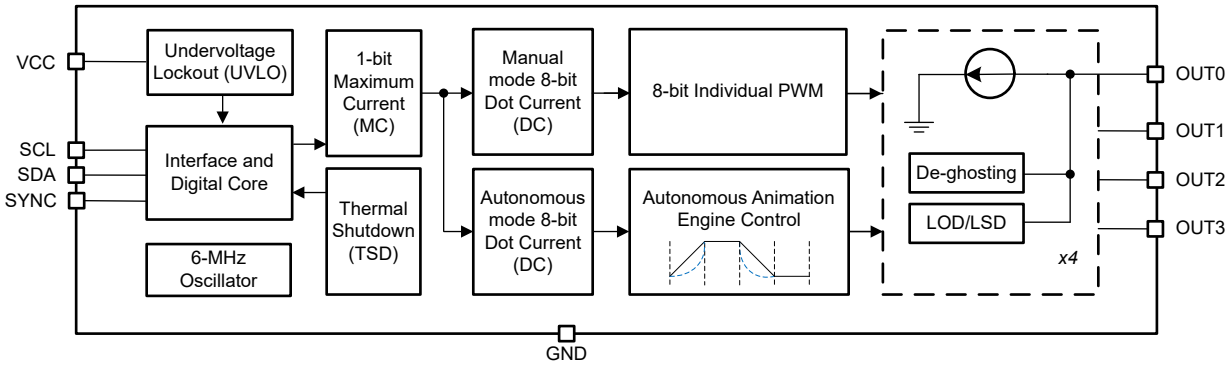

Figure 1-1. Device Block Diagram

Chapter 2

Register Maps

This section shows the detailed register maps of LP5810.

2.1 Register Map Table

This section provides a summary of the register maps.

Table 2-1. Register Section/Block Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0
Write Type		
W	W	Write
W1C	W 1C	W 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Device_Enable Register											
Chip_en	000h	R/W	Reserved							chip_en	00h
Config Registers											
Dev_Config_0	001h	R/W	Reserved							max_current	00h
Dev_Config_1	002h	R/W	pwm_fre	led_mode			Reserved				00h
Dev_Config_2	003h	R/W	Reserved								00h
Dev_Config_3	004h	R/W	Reserved				auto_en_3	auto_en_2	auto_en_1	auto_en_0	00h
Dev_Config_4	005h	R/W	Reserved								00h
Dev_Config_5	006h	R/W	Reserved				exp_en_3	exp_en_2	exp_en_1	exp_en_0	00h
Dev_Config_6	007h	R/W	Reserved								00h
Dev_Config_7	008h	R/W	phase_align_3		phase_align_2		phase_align_1		phase_align_0		00h
Dev_Config_8	009h	R/W	Reserved								00h
Dev_Config_9	00Ah	R/W	Reserved								00h
Dev_Config_10	00Bh	R/W	Reserved								00h
Dev_Config_11	00Ch	R/W	Reserved					vsync_out_en	blank_time		00h
Dev_Config_12	00Dh	R/W	vmid_sel		clamp_sel	clamp_dis	lod_action	lsd_action	lsd_threshold		08h
Command Registers											
CMD_Update	010h	W1C	update_command								00h
CMD_Start	011h	W1C	start_command								00h
CMD_Stop	012h	W1C	stop_command								00h
CMD_Pause	013h	W1C	pause_command								00h
CMD_Continue	014h	W1C	continue_command								00h
led_enable Registers											
led_en_1	020h	R/W	Reserved				led_en_3	led_en_2	led_en_1	led_en_0	00h
Fault_Clear Register											
Fault_Clear	022h	W1C	Reserved					tsd_clear	lsd_clear	lod_clear	00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Reset Register											
Reset	023h	W1C	sw_reset								00h
Manual_DC Registers											
Manual_DC_0	030h	R/W	manual_dc_0								00h
Manual_DC_1	031h	R/W	manual_dc_1								00h
Manual_DC_2	032h	R/W	manual_dc_2								00h
Manual_DC_3	033h	R/W	manual_dc_3								00h
Manual PWM Registers											
Manual_PWM_0	040h	R/W	manual_pwm_0								00h
Manual_PWM_1	041h	R/W	manual_pwm_1								00h
Manual_PWM_2	042h	R/W	manual_pwm_2								00h
Manual_PWM_3	043h	R/W	manual_pwm_3								00h
Autonomous_DC Registers											
Auto_DC_0	050h	R/W	auto_dc_0								00h
Auto_DC_1	051h	R/W	auto_dc_1								00h
Auto_DC_2	052h	R/W	auto_dc_2								00h
Auto_DC_3	053h	R/W	auto_dc_3								00h
LED_0_Autonomous_Animation Registers											
LED_0_Auto_Pause	080h	R/W	led_0_pause_start					led_0_pause_stop			00h
LED_0_Auto_Playback	081h	R/W	Reserved		led_0_aeu_num			LED_0_pt			00h
LED_0_AEU1_PWM_1	082h	R/W	led_0_aeu1_pwm1								00h
LED_0_AEU1_PWM_2	083h	R/W	led_0_aeu1_pwm2								00h
LED_0_AEU1_PWM_3	084h	R/W	led_0_aeu1_pwm3								00h
LED_0_AEU1_PWM_4	085h	R/W	led_0_aeu1_pwm4								00h
LED_0_AEU1_PWM_5	086h	R/W	led_0_aeu1_pwm5								00h
LED_0_AEU1_T12	087h	R/W	led_0_aeu1_t2				led_0_aeu1_t1				00h
LED_0_AEU1_T34	088h	R/W	led_0_aeu1_t4				led_0_aeu1_t3				00h
LED_0_AEU1_Playback	089h	R/W	Reserved						led_0_aeu1_pt		00h
LED_0_AEU2_PWM_1	08Ah	R/W	led_0_aeu2_pwm1								00h
LED_0_AEU2_PWM_2	08Bh	R/W	led_0_aeu2_pwm2								00h
LED_0_AEU2_PWM_3	08Ch	R/W	led_0_aeu2_pwm3								00h
LED_0_AEU2_PWM_4	08Dh	R/W	led_0_aeu2_pwm4								00h
LED_0_AEU2_PWM_5	08Eh	R/W	led_0_aeu2_pwm5								00h
LED_0_AEU2_T12	08Fh	R/W	led_0_aeu2_t2				led_0_aeu2_t1				00h
LED_0_AEU2_T34	090h	R/W	led_0_aeu2_t4				led_0_aeu2_t3				00h
LED_0_AEU2_Playback	091h	R/W	Reserved						led_0_aeu2_pt		00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
LED_0_AEU3_PWM_1	092h	R/W	led_0_aeu3_pwm1								00h
LED_0_AEU3_PWM_2	093h	R/W	led_0_aeu3_pwm2								00h
LED_0_AEU3_PWM_3	094h	R/W	led_0_aeu3_pwm3								00h
LED_0_AEU3_PWM_4	095h	R/W	led_0_aeu3_pwm4								00h
LED_0_AEU3_PWM_5	096h	R/W	led_0_aeu3_pwm5								00h
LED_0_AEU3_T12	097h	R/W	led_0_aeu3_t2				led_0_aeu3_t1				00h
LED_0_AEU3_T34	098h	R/W	led_0_aeu3_t4				led_0_aeu3_t3				00h
LED_0_AEU3_Playback	099h	R/W	Reserved						led_0_aeu3_pt		00h
LED_1 Autonomous Animation Registers											
LED_1_Auto_Pause	09Ah	R/W	led_1_pause_start				led_1_pause_stop				00h
LED_1_Auto_Playback	09Bh	R/W	Reserved		led_1_aeu_num		led_1_pt				00h
LED_1_AEU1_PWM_1	09Ch	R/W	led_1_aeu1_pwm1								00h
LED_1_AEU1_PWM_2	09Dh	R/W	led_1_aeu1_pwm2								00h
LED_1_AEU1_PWM_3	09Eh	R/W	led_1_aeu1_pwm3								00h
LED_1_AEU1_PWM_4	09Fh	R/W	led_1_aeu1_pwm4								00h
LED_1_AEU1_PWM_5	0A0h	R/W	led_1_aeu1_pwm5								00h
LED_1_AEU1_T12	0A1h	R/W	led_1_aeu1_t2				led_1_aeu1_t1				00h
LED_1_AEU1_T34	0A2h	R/W	led_1_aeu1_t4				led_1_aeu1_t3				00h
LED_1_AEU1_Playback	0A3h	R/W	Reserved						led_1_aeu1_pt		00h
LED_1_AEU2_PWM_1	0A4h	R/W	led_1_aeu2_pwm1								00h
LED_1_AEU2_PWM_2	0A5h	R/W	led_1_aeu2_pwm2								00h
LED_1_AEU2_PWM_3	0A6h	R/W	led_1_aeu2_pwm3								00h
LED_1_AEU2_PWM_4	0A7h	R/W	led_1_aeu2_pwm4								00h
LED_1_AEU2_PWM_5	0A8h	R/W	led_1_aeu2_pwm5								00h
LED_1_AEU2_T12	0A9h	R/W	led_1_aeu1_t2				led_1_aeu1_t1				00h
LED_1_AEU2_T34	0AAh	R/W	led_1_aeu1_t4				led_1_aeu1_t3				00h
LED_1_AEU2_Playback	0ABh	R/W	Reserved						led_1_aeu2_pt		00h
LED_1_AEU3_PWM_1	0ACh	R/W	led_1_aeu3_pwm1								00h
LED_1_AEU3_PWM_2	0ADh	R/W	led_1_aeu3_pwm2								00h
LED_1_AEU3_PWM_3	0AEh	R/W	led_1_aeu3_pwm3								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
LED_1_AEU3_PWM_4	0AFh	R/W	led_1_aeu3_pwm4								00h
LED_1_AEU3_PWM_5	0B0h	R/W	led_1_aeu3_pwm5								00h
LED_1_AEU3_T12	0B1h	R/W	led_1_aeu3_t2				led_1_aeu3_t1				00h
LED_1_AEU3_T34	0B2h	R/W	led_1_aeu3_t4				led_1_aeu3_t3				00h
LED_1_AEU3_Playback	0B3h	R/W	Reserved						led_1_aeu3_pt		00h
LED_2 Autonomous Animation Registers											
LED_2_Auto_Pause	0B4h	R/W	led_2_pause_start				led_2_pause_stop				00h
LED_2_Auto_Playback	0B5h	R/W	Reserved		led_2_aeu_num		led_2_pt				00h
LED_2_AEU1_PWM_1	0B6h	R/W	led_2_aeu1_pwm1								00h
LED_2_AEU1_PWM_2	0B7h	R/W	led_2_aeu1_pwm2								00h
LED_2_AEU1_PWM_3	0B7h	R/W	led_2_aeu1_pwm3								00h
LED_2_AEU1_PWM_4	0B9h	R/W	led_2_aeu1_pwm4								00h
LED_2_AEU1_PWM_5	0BAh	R/W	led_2_aeu1_pwm5								00h
LED_2_AEU1_T12	0BBh	R/W	led_2_aeu1_t2				led_2_aeu1_t1				00h
LED_2_AEU1_T34	0BCh	R/W	led_2_aeu1_t4				led_2_aeu1_t3				00h
LED_2_AEU1_Playback	0BDh	R/W	Reserved						led_2_aeu1_pt		00h
LED_2_AEU2_PWM_1	0BEh	R/W	led_2_aeu2_pwm1								00h
LED_2_AEU2_PWM_2	0BFh	R/W	led_2_aeu2_pwm2								00h
LED_2_AEU2_PWM_3	0C0h	R/W	led_2_aeu2_pwm3								00h
LED_2_AEU2_PWM_4	0C1h	R/W	led_2_aeu2_pwm4								00h
LED_2_AEU2_PWM_5	0C2h	R/W	led_2_aeu2_pwm5								00h
LED_2_AEU2_T12	0C3h	R/W	led_2_aeu2_t2				led_2_aeu2_t1				00h
LED_2_AEU2_T34	0C4h	R/W	led_2_aeu2_t4				led_2_aeu2_t3				00h
LED_2_AEU2_Playback	0C5h	R/W	Reserved						led_2_aeu2_pt		00h
LED_2_AEU3_PWM_1	0C6h	R/W	led_2_aeu3_pwm1								00h
LED_2_AEU3_PWM_2	0C7h	R/W	led_2_aeu3_pwm2								00h
LED_2_AEU3_PWM_3	0C8h	R/W	led_2_aeu3_pwm3								00h
LED_2_AEU3_PWM_4	0C9h	R/W	led_2_aeu3_pwm4								00h
LED_2_AEU3_PWM_5	0CAh	R/W	led_2_aeu3_pwm5								00h
LED_2_AEU3_T12	0CBh	R/W	led_2_aeu3_t2				led_2_aeu3_t1				00h
LED_2_AEU3_T34	0CCh	R/W	led_2_aeu3_t4				led_2_aeu3_t3				00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
LED_2_AEU3_Playback	0CDh	R/W	Reserved						led_2_aeu3_pt		00h
LED_3 Autonomous Animation Registers											
LED_3_Auto_Pause	0CEh	R/W	led_3_pause_start				led_3_pause_stop				00h
LED_3_Auto_Playback	0CFh	R/W	Reserved		led_3_aeu_num		led_3_pt				00h
LED_3_AEU1_PWM_1	0D0h	R/W	led_3_aeu1_pwm1								00h
LED_3_AEU1_PWM_2	0D1h	R/W	led_3_aeu1_pwm2								00h
LED_3_AEU1_PWM_3	0D2h	R/W	led_3_aeu1_pwm3								00h
LED_3_AEU1_PWM_4	0D3h	R/W	led_3_aeu1_pwm4								00h
LED_3_AEU1_PWM_5	0D4h	R/W	led_3_aeu1_pwm5								00h
LED_3_AEU1_T12	0D5h	R/W	led_3_aeu1_t2				led_3_aeu1_t1				00h
LED_3_AEU1_T34	0D6h	R/W	led_3_aeu1_t4				led_3_aeu1_t3				00h
LED_3_AEU1_Playback	0D7h	R/W	Reserved						led_3_aeu1_pt		00h
LED_3_AEU2_PWM_1	0D8h	R/W	led_3_aeu2_pwm1								00h
LED_3_AEU2_PWM_2	0D9h	R/W	led_3_aeu2_pwm2								00h
LED_3_AEU2_PWM_3	0DAh	R/W	led_3_aeu2_pwm3								00h
LED_3_AEU2_PWM_4	0DBh	R/W	led_3_aeu2_pwm4								00h
LED_3_AEU2_PWM_5	0DCh	R/W	led_3_aeu2_pwm5								00h
LED_3_AEU2_T12	0DDh	R/W	led_3_aeu2_t2				led_3_aeu2_t1				00h
LED_3_AEU2_T34	0DEh	R/W	led_3_aeu2_t4				led_3_aeu2_t3				00h
LED_3_AEU2_Playback	0DFh	R/W	Reserved						led_3_aeu2_pt		00h
LED_3_AEU3_PWM_1	0E0h	R/W	led_3_aeu3_pwm1								00h
LED_3_AEU3_PWM_2	0E1h	R/W	led_3_aeu3_pwm2								00h
LED_3_AEU3_PWM_3	0E2h	R/W	led_3_aeu3_pwm3								00h
LED_3_AEU3_PWM_4	0E3h	R/W	led_3_aeu3_pwm4								00h
LED_3_AEU3_PWM_5	0E4h	R/W	led_3_aeu3_pwm5								00h
LED_3_AEU3_T12	0E5h	R/W	led_3_aeu3_t2				led_3_aeu3_t1				00h
LED_3_AEU3_T34	0E6h	R/W	led_3_aeu3_t4				led_3_aeu3_t3				00h
LED_3_AEU3_Playback	0E7h	R/W	Reserved						led_3_aeu3_pt		00h
Flag Registers											
TSD_Config_Status	300h	R	Reserved						tsd_Status	config_err_status	00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
LOD_Status_0	301h	R	Reserved				lod_status_3	lod_status_2	lod_status_1	lod_status_0	00h
LOD_Status_1	302h	R	Reserved								00h
LSD_Status_0	303h	R	Reserved				lsd_status_3	lsd_status_2	lsd_status_1	lsd_status_0	00h
LSD_Status_1	304h	R	Reserved								00h
Auto_PWM_0	305h	R	pwm_auto_0								00h
Auto_PWM_1	306h	R	pwm_auto_1								00h
Auto_PWM_2	307h	R	pwm_auto_2								00h
Auto_PWM_3	308h	R	pwm_auto_3								00h
AEP_Status_0	315h	R	Reserved		aep_status_1			aep_status_0			3Fh
AEP_Status_1	316h	R	Reserved		aep_status_3			aep_status_2			3Fh

2.2 Device_Enable Registers

Table 2-2 lists the memory-mapped registers for the Device_Enable registers. All register offset addresses not listed in Table 2-2 should be considered as reserved locations and the register contents should not be modified.

Table 2-2. DEVICE_ENABLE Registers

Offset	Acronym	Register Name	Section
0h	Chip_EN	Enable the internal circuits	Go

Complex bit access types are encoded to fit into small table cells. Table 2-3 shows the codes that are used for access types in this section.

Table 2-3. Device_Enable Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.2.1 Chip_EN Register (Offset = 0h) [Reset = 00h]

Chip_EN is shown in Figure 2-1 and described in Table 2-4.

Return to the Summary Table.

Figure 2-1. Chip_EN Register

7	6	5	4	3	2	1	0
RESERVED							chip_en
R-0h							R/W-0h

Table 2-4. Chip_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	chip_en	R/W	0h	Enable the internal circuits; 0h = Disable; 1h = Enable

2.3 Config Registers

Table 2-5 lists the memory-mapped registers for the Config registers. All register offset addresses not listed in Table 2-5 should be considered as reserved locations and the register contents should not be modified.

Table 2-5. CONFIG Registers

Offset	Acronym	Register Name	Section
1h	Dev_Config_0	Device configuration register 0, including max current sinks current settings	Go
2h	Dev_Config_1	Device configuration register 1, including LED configuration and PWM frequency settings	Go
3h	Dev_Config_2	Device configuration register 2, reserved	
4h	Dev_Config_3	Device configuration register 3, including autonomous enable settings for LED_0 to LED_3	Go
5h	Dev_Config_4	Device configuration register 4, reserved	

Table 2-5. CONFIG Registers (continued)

Offset	Acronym	Register Name	Section
6h	Dev_Config_5	Device configuration register 5, including exponential curve enable settings for LED_0 to LED_3	Go
7h	Dev_Config_6	Device configuration register 6, reserved	
8h	Dev_Config_7	Device configuration register 7, including phase shiftt settings for LED_0 to LED_3	Go
9h	Dev_Config_8	Device configuration register 8, reserved	
Ah	Dev_Config_9	Device configuration register 9, reserved	
Bh	Dev_Config_10	Device configuration register 10, reserved	
Ch	Dev_Config_11	Device configuration register 11, including line change time and VSYNC settings	Go
Dh	Dev_Config_12	Device configuration register 12, including threshold and action settings for LOD, LSD and clamp	Go

Complex bit access types are encoded to fit into small table cells. Table 2-6 shows the codes that are used for access types in this section.

Table 2-6. Config Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.3.1 Dev_Config_0 Register (Offset = 1h) [Reset = 00h]

Dev_Config_0 is shown in Figure 2-2 and described in Table 2-7.

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Figure 2-2. Dev_Config_0 Register

7	6	5	4	3	2	1	0
RESERVED							max_current
R-0h							R/W-0h

Table 2-7. Dev_Config_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	max_current	R/W	0h	Max output current setting; 0h = 25.5mA; 1h = 51mA

2.3.2 Dev_Config_1 Register (Offset = 2h) [Reset = 00h]

Dev_Config_1 is shown in Figure 2-3 and described in Table 2-8.

Return to the Summary Table.

Figure 2-3. Dev_Config_1 Register

7	6	5	4	3	2	1	0

Figure 2-3. Dev_Config_1 Register (continued)

pwm_fre	led_mode	RESERVED
R/W-0h	R/W-0h	R-0h

Table 2-8. Dev_Config_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	pwm_fre	R/W	0h	PWM dimming frequency setting; 0h = 24kHz; 1h = 12kHz
6-4	led_mode	R/W	0h	LED mode configuration; 0h = Direct drive mode;
3-0	RESERVED	R	0h	Reserved

2.3.3 Dev_Config_2 Register (Offset = 3h) [Reset = 00h]

Dev_Config_2 is shown in Figure 2-4 and described in Table 2-9.

Return to the Summary Table.

Figure 2-4. Dev_Config_2 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 2-9. Dev_Config_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

2.3.4 Dev_Config_3 Register (Offset = 4h) [Reset = 00h]

Dev_Config_3 is shown in Figure 2-5 and described in Table 2-10.

Return to the Summary Table.

Figure 2-5. Dev_Config_3 Register

7	6	5	4	3	2	1	0
RESERVED				auto_en_3	auto_en_2	auto_en_1	auto_en_0
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 2-10. Dev_Config_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	auto_en_3	R/W	0h	LED_3 autonomous control enable; 0h = Disabled, LED in manual mode; 1h = Enabled, LED in autonomous mode
2	auto_en_2	R/W	0h	LED_2 autonomous control enable; 0h = Disabled, LED in manual mode; 1h = Enabled, LED in autonomous mode
1	auto_en_1	R/W	0h	LED_1 autonomous control enable; 0h = Disabled, LED in manual mode; 1h = Enabled, LED in autonomous mode
0	auto_en_0	R/W	0h	LED_0 autonomous control enable; 0h = Disabled, LED in manual mode; 1h = Enabled, LED in autonomous mode

2.3.5 Dev_Config_4 Register (Offset = 5h) [Reset = 00h]

Dev_Config_4 is shown in Figure 2-6 and described in Table 2-11.

Return to the Summary Table.

Figure 2-6. Dev_Config_4 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 2-11. Dev_Config_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

2.3.6 Dev_Config_5 Register (Offset = 6h) [Reset = 00h]

Dev_Config_5 is shown in Figure 2-7 and described in Table 2-12.

Return to the Summary Table.

Figure 2-7. Dev_Config_5 Register

7	6	5	4	3	2	1	0
RESERVED				exp_en_3	exp_en_2	exp_en_1	exp_en_0
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 2-12. Dev_Config_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	exp_en_3	R/W	0h	LED_3 exponential dimming enable; 0h = Disabled, LED PWM dimming with linear curve; 1h = Enabled, LED PWM dimming with exponential curve
2	exp_en_2	R/W	0h	LED_2 exponential dimming enable; 0h = Disabled, LED PWM dimming with linear curve; 1h = Enabled, LED PWM dimming with exponential curve
1	exp_en_1	R/W	0h	LED_1 exponential dimming enable; 0h = Disabled, LED PWM dimming with linear curve; 1h = Enabled, LED PWM dimming with exponential curve
0	exp_en_0	R/W	0h	LED_0 exponential dimming enable; 0h = Disabled, LED PWM dimming with linear curve; 1h = Enabled, LED PWM dimming with exponential curve

2.3.7 Dev_Config_6 Register (Offset = 7h) [Reset = 00h]

Dev_Config_6 is shown in Figure 2-8 and described in Table 2-13.

Return to the Summary Table.

Figure 2-8. Dev_Config_6 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Figure 2-8. Dev_Config_6 Register (continued)

Table 2-13. Dev_Config_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

2.3.8 Dev_Config_7 Register (Offset = 8h) [Reset = 00h]

Dev_Config_7 is shown in Figure 2-9 and described in Table 2-14.

Return to the Summary Table.

Figure 2-9. Dev_Config_7 Register

7	6	5	4	3	2	1	0
phase_align_3		phase_align_2		phase_align_1		phase_align_0	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 2-14. Dev_Config_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	phase_align_3	R/W	0h	LED_3 PWM phase align method; 0h = Forward align; 1h = Forward align; 2h = Middle align; 3h = Backward align
5-4	phase_align_2	R/W	0h	LED_2 PWM phase align method; 0h = Forward align; 1h = Forward align; 2h = Middle align; 3h = Backward align
3-2	phase_align_1	R/W	0h	LED_1 PWM phase align method; 0h = Forward align; 1h = Forward align; 2h = Middle align; 3h = Backward align
1-0	phase_align_0	R/W	0h	LED_0 PWM phase align method; 0h = Forward align; 1h = Forward align; 2h = Middle align; 3h = Backward align

2.3.9 Dev_Config_8 Register (Offset = 9h) [Reset = 00h]

Dev_Config_8 is shown in Figure 2-10 and described in Table 2-15.

Return to the Summary Table.

Figure 2-10. Dev_Config_8 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 2-15. Dev_Config_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

2.3.10 Dev_Config_9 Register (Offset = Ah) [Reset = 00h]

Dev_Config_9 is shown in Figure 2-11 and described in Table 2-16.

Return to the Summary Table.

Figure 2-11. Dev_Config_9 Register

7	6	5	4	3	2	1	0

Figure 2-11. Dev_Config_9 Register (continued)

RESERVED
R-0h

Table 2-16. Dev_Config_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

2.3.11 Dev_Config_10 Register (Offset = Bh) [Reset = 00h]

Dev_Config_10 is shown in Figure 2-12 and described in Table 2-17.

Return to the Summary Table.

Figure 2-12. Dev_Config_10 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 2-17. Dev_Config_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

2.3.12 Dev_Config_11 Register (Offset = Ch) [Reset = 00h]

Dev_Config_11 is shown in Figure 2-13 and described in Table 2-18.

Return to the Summary Table.

Figure 2-13. Dev_Config_11 Register

7	6	5	4	3	2	1	0
RESERVED					vsync_out_en	blank_time	
R-0h					R/W-0h	R/W-0h	

Table 2-18. Dev_Config_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	vsync_out_en	R/W	0h	Vsync used as output to export internal oscilator clock; 0h = Vsync is input; 1h = Vsync is output
1-0	blank_time	R/W	0h	Line change time; 0h = 1us; 1h = 1.3us; 2h = 1.7us; 3h = 2us

2.3.13 Dev_Config_12 Register (Offset = Dh) [Reset = 08h]

Dev_Config_12 is shown in Figure 2-14 and described in Table 2-19.

Return to the Summary Table.

Figure 2-14. Dev_Config_12 Register

7	6	5	4	3	2	1	0
vmid_sel		clamp_sel	clamp_dis	lod_action	lsd_action	lsd_threshold	
R/W-0h		R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	

Table 2-19. Dev_Config_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	vmid_sel	R/W	0h	Clamp voltage selection; 0h = VOUT-1.1V; 1h = VOUT-1.3V; 2h = VOUT-1.5V; 3h = VOUT-1.7V
5	clamp_sel	R/W	0h	Clamp behavior selection; 0h = Clamp the OUTs only during line change time; 1h = Clamp the OUTs once current sink turns off
4	clamp_dis	R/W	0h	Clamp behavior disable; 0h = Enale clamp; 1h = Disable clamp
3	lod_action	R/W	1h	Action when LED open fault happens; 0h = No action; 1h = Shutdown current sink
2	lsd_action	R/W	0h	Action when LED short fault happens; 0h = No action; 1h = All OUTs shut down
1-0	lsd_threshold	R/W	0h	LSD threshold; 0h = 0.35 * VOUT; 1h = 0.45 * VOUT; 2h = 0.55 * VOUT; 3h = 0.65 * VOUT

2.4 Command Registers

Table 2-20 lists the memory-mapped registers for the Command registers. All register offset addresses not listed in Table 2-20 should be considered as reserved locations and the register contents should not be modified.

Table 2-20. COMMAND Registers

Offset	Acronym	Register Name	Section
10h	CMD_Update	Configuration update command	Go
11h	CMD_Start	Autonomous animation start command	Go
12h	CMD_Stop	Autonomous animation stop command	Go
13h	CMD_Pause	Autonomous animation pause command	Go
14h	CMD_Continue	Autonomous animation continue command	Go

Complex bit access types are encoded to fit into small table cells. Table 2-21 shows the codes that are used for access types in this section.

Table 2-21. Command Access Type Codes

Access Type	Code	Description
Write Type		
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

2.4.1 CMD_Update Register (Offset = 10h) [Reset = 00h]

CMD_Update is shown in Figure 2-15 and described in Table 2-22.

Return to the Summary Table.

Figure 2-15. CMD_Update Register

7	6	5	4	3	2	1	0
update_cmd							
W1C-0h							

Table 2-22. CMD_Update Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	update_cmd	W1C	0h	Configuration update command: registers001h to 00Bh will **ONLY** be effective by sending this command; **Write 55h to send this command**

2.4.2 CMD_Start Register (Offset = 11h) [Reset = 00h]

CMD_Start is shown in Figure 2-16 and described in Table 2-23.

Return to the Summary Table.

Figure 2-16. CMD_Start Register

7	6	5	4	3	2	1	0
start_cmd							
W1C-0h							

Table 2-23. CMD_Start Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	start_cmd	W1C	0h	Send start_command to start autonomous control or restart with the latest setting; **Write FFh to send this command**

2.4.3 CMD_Stop Register (Offset = 12h) [Reset = 00h]

CMD_Stop is shown in Figure 2-17 and described in Table 2-24.

Return to the Summary Table.

Figure 2-17. CMD_Stop Register

7	6	5	4	3	2	1	0
stop_cmd							
W1C-0h							

Table 2-24. CMD_Stop Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	stop_cmd	W1C	0h	Stop LED current status immediately, and go back to **INITIAL** state; **Write AAh to send this command**

2.4.4 CMD_Pause Register (Offset = 13h) [Reset = 00h]

CMD_Pause is shown in Figure 2-18 and described in Table 2-25.

Return to the Summary Table.

Figure 2-18. CMD_Pause Register

7	6	5	4	3	2	1	0
pause_cmd							
W1C-0h							

Table 2-25. CMD_Pause Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	pause_cmd	W1C	0h	Pause autonomous control at the current state, keep Internal sloper register unchanged, but the scan keeps going-on using the previous calculated pwm data; **Write 33h to send this command**

2.4.5 CMD_Continue Register (Offset = 14h) [Reset = 00h]

CMD_Continue is shown in Figure 2-19 and described in Table 2-26.

Return to the Summary Table.

Figure 2-19. CMD_Continue Register

7	6	5	4	3	2	1	0
continue_cmd							
W1C-0h							

Table 2-26. CMD_Continue Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	continue_cmd	W1C	0h	Continue autonomous control; **Write CCh to send this command**

2.5 LED_Enable Registers

Table 2-27 lists the memory-mapped registers for the LED_Enable registers. All register offset addresses not listed in Table 2-27 should be considered as reserved locations and the register contents should not be modified.

Table 2-27. LED_ENABLE Registers

Offset	Acronym	Register Name	Section
20h	LED_EN_1	Enable the LEDs of LED_0 to LED_3	Go

Complex bit access types are encoded to fit into small table cells. Table 2-28 shows the codes that are used for access types in this section.

Table 2-28. LED_Enable Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.5.1 LED_EN_1 Register (Offset = 20h) [Reset = 00h]

LED_EN_1 is shown in Figure 2-20 and described in Table 2-29.

Return to the Summary Table.

Figure 2-20. LED_EN_1 Register

7	6	5	4	3	2	1	0
RESERVED				led_en_3	led_en_2	led_en_1	led_en_0

Figure 2-20. LED_EN_1 Register (continued)

R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 2-29. LED_EN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	led_en_3	R/W	0h	LED_3 Enable; 0h = Disabled; 1h = Enabled
2	led_en_2	R/W	0h	LED_2 Enable; 0h = Disabled; 1h = Enabled
1	led_en_1	R/W	0h	LED_1 Enable; 0h = Disabled; 1h = Enabled
0	led_en_0	R/W	0h	LED_0 Enable; 0h = Disabled; 1h = Enabled

2.6 Fault_Clear Registers

Table 2-30 lists the memory-mapped registers for the Fault_Clear registers. All register offset addresses not listed in Table 2-30 should be considered as reserved locations and the register contents should not be modified.

Table 2-30. FAULT_CLEAR Registers

Offset	Acronym	Register Name	Section
22h	Fault_Clear	Clear the LOD/LSD/TSD flats	Go

Complex bit access types are encoded to fit into small table cells. Table 2-31 shows the codes that are used for access types in this section.

Table 2-31. Fault_Clear Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

2.6.1 Fault_Clear Register (Offset = 22h) [Reset = 00h]

Fault_Clear is shown in Figure 2-21 and described in Table 2-32.

Return to the Summary Table.

Figure 2-21. Fault_Clear Register

7	6	5	4	3	2	1	0
RESERVED					tsd_clear	lsd_clear	lod_clear
R-0h					W1C-0h	W1C-0h	W1C-0h

Table 2-32. Fault_Clear Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	tsd_clear	W1C	0h	TSD Fault Status Clear; **Write 1 to clear and read back 0**
1	lsd_clear	W1C	0h	LSD Fault Status Clear; **Write 1 to clear and read back 0**

Table 2-32. Fault_Clear Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	lod_clear	W1C	0h	LOD Fault Status Clear; **Write 1 to clear and read back 0**

2.7 Reset Registers

Table 2-33 lists the memory-mapped registers for the Reset registers. All register offset addresses not listed in Table 2-33 should be considered as reserved locations and the register contents should not be modified.

Table 2-33. RESET Registers

Offset	Acronym	Register Name	Section
23h	Reset	Software reset	Go

Complex bit access types are encoded to fit into small table cells. Table 2-34 shows the codes that are used for access types in this section.

Table 2-34. Reset Access Type Codes

Access Type	Code	Description
Write Type		
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

2.7.1 Reset Register (Offset = 23h) [Reset = 00h]

Reset is shown in Figure 2-22 and described in Table 2-35.

Return to the Summary Table.

Figure 2-22. Reset Register

7	6	5	4	3	2	1	0
sw_reset							
W1C-0h							

Table 2-35. Reset Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	sw_reset	W1C	0h	Software reset; **Write 66h to reset**

2.8 Manual_DC Registers

Table 2-36 lists the memory-mapped registers for the Manual_DC registers. All register offset addresses not listed in Table 2-36 should be considered as reserved locations and the register contents should not be modified.

Table 2-36. MANUAL_DC Registers

Offset	Acronym	Register Name	Section
30h	Manual_DC_0	LED_0 current setting in manual mode	Go
31h	Manual_DC_1	LED_1 current setting in manual mode	Go
32h	Manual_DC_2	LED_2 current setting in manual mode	Go
33h	Manual_DC_3	LED_3 current setting in manual mode	Go

Complex bit access types are encoded to fit into small table cells. Table 2-37 shows the codes that are used for access types in this section.

Table 2-37. Manual_DC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.8.1 Manual_DC_0 Register (Offset = 30h) [Reset = 00h]

Manual_DC_0 is shown in Figure 2-23 and described in Table 2-38.

Return to the Summary Table.

Figure 2-23. Manual_DC_0 Register

7	6	5	4	3	2	1	0
manual_dc_0							
R/W-0h							

Table 2-38. Manual_DC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	manual_dc_0	R/W	0h	LED_0 current setting in manual mode; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.8.2 Manual_DC_1 Register (Offset = 31h) [Reset = 00h]

Manual_DC_1 is shown in Figure 2-24 and described in Table 2-39.

Return to the Summary Table.

Figure 2-24. Manual_DC_1 Register

7	6	5	4	3	2	1	0
manual_dc_1							
R/W-0h							

Table 2-39. Manual_DC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	manual_dc_1	R/W	0h	LED_1 current setting in manual mode; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.8.3 Manual_DC_2 Register (Offset = 32h) [Reset = 00h]

Manual_DC_2 is shown in Figure 2-25 and described in Table 2-40.

Return to the Summary Table.

Figure 2-25. Manual_DC_2 Register

7	6	5	4	3	2	1	0
manual_dc_2							
R/W-0h							

Table 2-40. Manual_DC_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	manual_dc_2	R/W	0h	LED_2 current setting in manual mode; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.8.4 Manual_DC_3 Register (Offset = 33h) [Reset = 00h]

Manual_DC_3 is shown in Figure 2-26 and described in Table 2-41.

Return to the Summary Table.

Figure 2-26. Manual_DC_3 Register

7	6	5	4	3	2	1	0
manual_dc_3							
R/W-0h							

Table 2-41. Manual_DC_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	manual_dc_3	R/W	0h	LED_3 current setting in manual mode; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.9 Manual_PWM Registers

Table 2-42 lists the memory-mapped registers for the Manual_PWM registers. All register offset addresses not listed in Table 2-42 should be considered as reserved locations and the register contents should not be modified.

Table 2-42. MANUAL_PWM Registers

Offset	Acronym	Register Name	Section
40h	Manual_PWM_0	LED_0 PWM setting in manual mode	Go
41h	Manual_PWM_1	LED_1 PWM setting in manual mode	Go
42h	Manual_PWM_2	LED_2 PWM setting in manual mode	Go
43h	Manual_PWM_3	LED_3 PWM setting in manual mode	Go

Complex bit access types are encoded to fit into small table cells. Table 2-43 shows the codes that are used for access types in this section.

Table 2-43. Manual_PWM Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		

Table 2-43. Manual_PWM Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

2.9.1 Manual_PWM_0 Register (Offset = 40h) [Reset = 00h]

Manual_PWM_0 is shown in Figure 2-27 and described in Table 2-44.

Return to the Summary Table.

Figure 2-27. Manual_PWM_0 Register

7	6	5	4	3	2	1	0
manual_pwm_0							
R/W-0h							

Table 2-44. Manual_PWM_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	manual_pwm_0	R/W	0h	LED_0 PWM setting in manual mode; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.9.2 Manual_PWM_1 Register (Offset = 41h) [Reset = 00h]

Manual_PWM_1 is shown in Figure 2-28 and described in Table 2-45.

Return to the Summary Table.

Figure 2-28. Manual_PWM_1 Register

7	6	5	4	3	2	1	0
manual_pwm_1							
R/W-0h							

Table 2-45. Manual_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	manual_pwm_1	R/W	0h	LED_1 PWM setting in manual mode; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.9.3 Manual_PWM_2 Register (Offset = 42h) [Reset = 00h]

Manual_PWM_2 is shown in Figure 2-29 and described in Table 2-46.

Return to the Summary Table.

Figure 2-29. Manual_PWM_2 Register

7	6	5	4	3	2	1	0
manual_pwm_2							
R/W-0h							

Table 2-46. Manual_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	manual_pwm_2	R/W	0h	LED_2 PWM setting in manual mode; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.9.4 Manual_PWM_3 Register (Offset = 43h) [Reset = 00h]

Manual_PWM_3 is shown in Figure 2-30 and described in Table 2-47.

Return to the Summary Table.

Figure 2-30. Manual_PWM_3 Register

7	6	5	4	3	2	1	0
manual_pwm_3							
R/W-0h							

Table 2-47. Manual_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	manual_pwm_3	R/W	0h	LED_3 PWM setting in manual mode; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.10 Autonomous_DC Registers

Table 2-48 lists the memory-mapped registers for the Autonomous_DC registers. All register offset addresses not listed in Table 2-48 should be considered as reserved locations and the register contents should not be modified.

Table 2-48. AUTONOMOUS_DC Registers

Offset	Acronym	Register Name	Section
50h	Auto_DC_0	LED_0 current setting in autonomous mode	Go
51h	Auto_DC_1	LED_1 current setting in autonomous mode	Go
52h	Auto_DC_2	LED_2 current setting in autonomous mode	Go
53h	Auto_DC_3	LED_3 current setting in autonomous mode	Go

Complex bit access types are encoded to fit into small table cells. Table 2-49 shows the codes that are used for access types in this section.

Table 2-49. Autonomous_DC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.10.1 Auto_DC_0 Register (Offset = 50h) [Reset = 00h]

Auto_DC_0 is shown in Figure 2-31 and described in Table 2-50.

Return to the Summary Table.

Figure 2-31. Auto_DC_0 Register

7	6	5	4	3	2	1	0
auto_dc_0							
R/W-0h							

Table 2-50. Auto_DC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	auto_dc_0	R/W	0h	LED_0 current setting in autonomous mode; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.10.2 Auto_DC_1 Register (Offset = 51h) [Reset = 00h]

Auto_DC_1 is shown in Figure 2-32 and described in Table 2-51.

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Figure 2-32. Auto_DC_1 Register

7	6	5	4	3	2	1	0
auto_dc_1							
R/W-0h							

Table 2-51. Auto_DC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	auto_dc_1	R/W	0h	LED_1 current setting in autonomous mode;; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.10.3 Auto_DC_2 Register (Offset = 52h) [Reset = 00h]

Auto_DC_2 is shown in Figure 2-33 and described in Table 2-52.

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Figure 2-33. Auto_DC_2 Register

7	6	5	4	3	2	1	0
auto_dc_2							
R/W-0h							

Table 2-52. Auto_DC_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	auto_dc_2	R/W	0h	LED_2 current setting in autonomous mode; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.10.4 Auto_DC_3 Register (Offset = 53h) [Reset = 00h]

Auto_DC_3 is shown in Figure 2-34 and described in Table 2-53.

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Figure 2-34. Auto_DC_3 Register

7	6	5	4	3	2	1	0
auto_dc_3							
R/W-0h							

Table 2-53. Auto_DC_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	auto_dc_3	R/W	0h	LED_3 current setting in autonomous mode; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11 LED_0_Autonomous_Animation Registers

Table 2-54 lists the memory-mapped registers for the LED_0_Autonomous_Animation registers. All register offset addresses not listed in Table 2-54 should be considered as reserved locations and the register contents should not be modified.

Table 2-54. LED_0_AUTONOMOUS_ANIMATION Registers

Offset	Acronym	Register Name	Section
80h	LED_0_Auto_Pause	Animation pause time at the start and the end of LED_0	Go
81h	LED_0_Auto_Playback	Animation pattern playback times of LED_0 and active AEU number setting	Go
82h	LED_0_AEU1_PWM_1	PWM setting of LED_0 AEU1_PWM1	Go
83h	LED_0_AEU1_PWM_2	PWM setting of LED_0 AEU1_PWM2	Go
84h	LED_0_AEU1_PWM_3	PWM setting of LED_0 AEU1_PWM3	Go
85h	LED_0_AEU1_PWM_4	PWM setting of LED_0 AEU1_PWM4	Go
86h	LED_0_AEU1_PWM_5	PWM setting of LED_0 AEU1_PWM5	Go
87h	LED_0_AEU1_T12	Slope time setting of LED_0 AEU1_T1 and AEU1_T2	Go
88h	LED_0_AEU1_T34	Slope time setting of LED_0 AEU1_T3 and AEU1_T4	Go
89h	LED_0_AEU1_Playback	AEU1 pattern playback times of LED_0	Go
8Ah	LED_0_AEU2_PWM_1	PWM setting of LED_0 AEU2_PWM1	Go
8Bh	LED_0_AEU2_PWM_2	PWM setting of LED_0 AEU2_PWM2	Go
8Ch	LED_0_AEU2_PWM_3	PWM setting of LED_0 AEU2_PWM3	Go
8Dh	LED_0_AEU2_PWM_4	PWM setting of LED_0 AEU2_PWM4	Go
8Eh	LED_0_AEU2_PWM_5	PWM setting of LED_0 AEU2_PWM5	Go
8Fh	LED_0_AEU2_T12	Slope time setting of LED_0 AEU2_T1 and AEU2_T2	Go
90h	LED_0_AEU2_T34	Slope time setting of LED_0 AEU2_T3 and AEU2_T4	Go
91h	LED_0_AEU2_Playback	AEU2 pattern playback times of LED_0	Go
92h	LED_0_AEU3_PWM_1	PWM setting of LED_0 AEU3_PWM1	Go
93h	LED_0_AEU3_PWM_2	PWM setting of LED_0 AEU3_PWM2	Go
94h	LED_0_AEU3_PWM_3	PWM setting of LED_0 AEU3_PWM3	Go
95h	LED_0_AEU3_PWM_4	PWM setting of LED_0 AEU3_PWM4	Go
96h	LED_0_AEU3_PWM_5	PWM setting of LED_0 AEU3_PWM5	Go
97h	LED_0_AEU3_T12	Slope time setting of LED_0 AEU3_T1 and AEU3_T2	Go
98h	LED_0_AEU3_T34	Slope time setting of LED_0 AEU3_T3 and AEU3_T4	Go
99h	LED_0_AEU3_Playback	AEU3 pattern playback times of LED_0	Go

Complex bit access types are encoded to fit into small table cells. Table 2-55 shows the codes that are used for access types in this section.

Table 2-55. LED_0_Autonomous_Animation Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.11.1 LED_0_Auto_Pause Register (Offset = 80h) [Reset = 00h]

LED_0_Auto_Pause is shown in Figure 2-35 and described in Table 2-56.

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Figure 2-35. LED_0_Auto_Pause Register

7	6	5	4	3	2	1	0
led_0_tp_ts				led_0_tp_te			
R/W-0h				R/W-0h			

Table 2-56. LED_0_Auto_Pause Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_0_tp_ts	R/W	0h	Animation pause time at the start of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_0_tp_te	R/W	0h	Animation pause time at the end of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.11.2 LED_0_Auto_Playback Register (Offset = 81h) [Reset = 00h]

LED_0_Auto_Playback is shown in Figure 2-36 and described in Table 2-57.

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Figure 2-36. LED_0_Auto_Playback Register

7	6	5	4	3	2	1	0
RESERVED		led_0_aeu_num		led_0_pt			
R-0h		R/W-0h		R/W-0h			

Table 2-57. LED_0_Auto_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	led_0_aeu_num	R/W	0h	Active AEU number of LED_0 selection; 0h = only use AEU1; 1h = use AEU1 and AEU2; 2h = use AEU1, AEU2 and AEU3; 3h = use AEU1, AEU2 and AEU3 (the same as 2h)
3-0	led_0_pt	R/W	0h	Animation pattern playback times of LED_0; 0h = 0 times; 1h = 1 times; 2h = 2 times; 3h = 3 times; 4h = 4 times; 5h = 5 times; 6h = 6 times; 7h = 7 times; 8h = 8 times; 9h = 9 times; Ah = 10 times; Bh = 11 times; Ch = 12 times; Dh = 13 times; Eh = 14 times; Fh = infinite times

2.11.3 LED_0_AEU1_PWM_1 Register (Offset = 82h) [Reset = 00h]

LED_0_AEU1_PWM_1 is shown in Figure 2-37 and described in Table 2-58.

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Figure 2-37. LED_0_AEU1_PWM_1 Register

7	6	5	4	3	2	1	0
led_0_aeu1_pwm1							
R/W-0h							

Table 2-58. LED_0_AEU1_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu1_pwm1	R/W	0h	AEU1_PWM1 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.4 LED_0_AEU1_PWM_2 Register (Offset = 83h) [Reset = 00h]

LED_0_AEU1_PWM_2 is shown in Figure 2-38 and described in Table 2-59.

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Figure 2-38. LED_0_AEU1_PWM_2 Register

7	6	5	4	3	2	1	0
led_0_aeu1_pwm2							
R/W-0h							

Table 2-59. LED_0_AEU1_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu1_pwm2	R/W	0h	AEU1_PWM2 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.5 LED_0_AEU1_PWM_3 Register (Offset = 84h) [Reset = 00h]

LED_0_AEU1_PWM_3 is shown in Figure 2-39 and described in Table 2-60.

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Figure 2-39. LED_0_AEU1_PWM_3 Register

7	6	5	4	3	2	1	0
led_0_aeu1_pwm3							
R/W-0h							

Table 2-60. LED_0_AEU1_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu1_pwm3	R/W	0h	AEU1_PWM3 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.6 LED_0_AEU1_PWM_4 Register (Offset = 85h) [Reset = 00h]

LED_0_AEU1_PWM_4 is shown in Figure 2-40 and described in Table 2-61.

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Figure 2-40. LED_0_AEU1_PWM_4 Register

7	6	5	4	3	2	1	0
led_0_aeu1_pwm4							
R/W-0h							

Table 2-61. LED_0_AEU1_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu1_pwm4	R/W	0h	AEU1_PWM4 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.7 LED_0_AEU1_PWM_5 Register (Offset = 86h) [Reset = 00h]

LED_0_AEU1_PWM_5 is shown in Figure 2-41 and described in Table 2-62.

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Figure 2-41. LED_0_AEU1_PWM_5 Register

7	6	5	4	3	2	1	0
led_0_aeu1_pwm5							
R/W-0h							

Table 2-62. LED_0_AEU1_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu1_pwm5	R/W	0h	AEU1_PWM5 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.8 LED_0_AEU1_T12 Register (Offset = 87h) [Reset = 00h]

LED_0_AEU1_T12 is shown in Figure 2-42 and described in Table 2-63.

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Figure 2-42. LED_0_AEU1_T12 Register

7	6	5	4	3	2	1	0
led_0_aeu1_t2				led_0_aeu1_t1			
R/W-0h				R/W-0h			

Table 2-63. LED_0_AEU1_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_0_aeu1_t2	R/W	0h	AEU1_T2 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_0_aeu1_t1	R/W	0h	AEU1_T1 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.11.9 LED_0_AEU1_T34 Register (Offset = 88h) [Reset = 00h]

LED_0_AEU1_T34 is shown in Figure 2-43 and described in Table 2-64.

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Figure 2-43. LED_0_AEU1_T34 Register

7	6	5	4	3	2	1	0
led_0_aeu1_t4				led_0_aeu1_t3			
R/W-0h				R/W-0h			

Table 2-64. LED_0_AEU1_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_0_aeu1_t4	R/W	0h	AEU1_T4 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_0_aeu1_t3	R/W	0h	AEU1_T3 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.11.10 LED_0_AEU1_Playback Register (Offset = 89h) [Reset = 00h]

LED_0_AEU1_Playback is shown in Figure 2-44 and described in Table 2-65.

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Figure 2-44. LED_0_AEU1_Playback Register

7	6	5	4	3	2	1	0
RESERVED						led_0_aeu1_pt	
R-0h						R/W-0h	

Table 2-65. LED_0_AEU1_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	led_0_aeu1_pt	R/W	0h	AEU1 pattern playback times of LED_0; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.11.11 LED_0_AEU2_PWM_1 Register (Offset = 8Ah) [Reset = 00h]

LED_0_AEU2_PWM_1 is shown in Figure 2-45 and described in Table 2-66.

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Figure 2-45. LED_0_AEU2_PWM_1 Register

7	6	5	4	3	2	1	0
led_0_aeu2_pwm1							
R/W-0h							

Table 2-66. LED_0_AEU2_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu2_pwm1	R/W	0h	AEU2_PWM1 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.12 LED_0_AEU2_PWM_2 Register (Offset = 8Bh) [Reset = 00h]

LED_0_AEU2_PWM_2 is shown in Figure 2-46 and described in Table 2-67.

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Figure 2-46. LED_0_AEU2_PWM_2 Register

7	6	5	4	3	2	1	0
led_0_aeu2_pwm2							
R/W-0h							

Table 2-67. LED_0_AEU2_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu2_pwm2	R/W	0h	AEU2_PWM2 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.13 LED_0_AEU2_PWM_3 Register (Offset = 8Ch) [Reset = 00h]

LED_0_AEU2_PWM_3 is shown in Figure 2-47 and described in Table 2-68.

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Figure 2-47. LED_0_AEU2_PWM_3 Register

7	6	5	4	3	2	1	0
led_0_aeu2_pwm3							
R/W-0h							

Table 2-68. LED_0_AEU2_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu2_pwm3	R/W	0h	AEU2_PWM3 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.14 LED_0_AEU2_PWM_4 Register (Offset = 8Dh) [Reset = 00h]

LED_0_AEU2_PWM_4 is shown in Figure 2-48 and described in Table 2-69.

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Figure 2-48. LED_0_AEU2_PWM_4 Register

7	6	5	4	3	2	1	0
led_0_aeu2_pwm4							
R/W-0h							

Table 2-69. LED_0_AEU2_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu2_pwm4	R/W	0h	AEU2_PWM4 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.15 LED_0_AEU2_PWM_5 Register (Offset = 8Eh) [Reset = 00h]

LED_0_AEU2_PWM_5 is shown in Figure 2-49 and described in Table 2-70.

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Figure 2-49. LED_0_AEU2_PWM_5 Register

7	6	5	4	3	2	1	0
led_0_aeu2_pwm5							
R/W-0h							

Table 2-70. LED_0_AEU2_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu2_pwm5	R/W	0h	AEU2_PWM5 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.16 LED_0_AEU2_T12 Register (Offset = 8Fh) [Reset = 00h]

LED_0_AEU2_T12 is shown in Figure 2-50 and described in Table 2-71.

Return to the Summary Table.

Figure 2-50. LED_0_AEU2_T12 Register

7	6	5	4	3	2	1	0
led_0_aeu2_t2				led_0_aeu2_t1			
R/W-0h				R/W-0h			

Table 2-71. LED_0_AEU2_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_0_aeu2_t2	R/W	0h	AEU2_T2 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_0_aeu2_t1	R/W	0h	AEU2_T1 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.11.17 LED_0_AEU2_T34 Register (Offset = 90h) [Reset = 00h]

LED_0_AEU2_T34 is shown in Figure 2-51 and described in Table 2-72.

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Figure 2-51. LED_0_AEU2_T34 Register

7	6	5	4	3	2	1	0
led_0_aeu2_t4				led_0_aeu2_t3			
R/W-0h				R/W-0h			

Table 2-72. LED_0_AEU2_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_0_aeu2_t4	R/W	0h	AEU2_T4 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_0_aeu2_t3	R/W	0h	AEU2_T3 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.11.18 LED_0_AEU2_Playback Register (Offset = 91h) [Reset = 00h]

LED_0_AEU2_Playback is shown in Figure 2-52 and described in Table 2-73.

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Figure 2-52. LED_0_AEU2_Playback Register

7	6	5	4	3	2	1	0
RESERVED						led_0_aeu2_pt	
R-0h						R/W-0h	

Table 2-73. LED_0_AEU2_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	led_0_aeu2_pt	R/W	0h	AEU2 pattern playback times of LED_0; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.11.19 LED_0_AEU3_PWM_1 Register (Offset = 92h) [Reset = 00h]

LED_0_AEU3_PWM_1 is shown in Figure 2-53 and described in Table 2-74.

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Figure 2-53. LED_0_AEU3_PWM_1 Register

7	6	5	4	3	2	1	0
led_0_aeu3_pwm1							
R/W-0h							

Table 2-74. LED_0_AEU3_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu3_pwm1	R/W	0h	AEU3_PWM1 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.20 LED_0_AEU3_PWM_2 Register (Offset = 93h) [Reset = 00h]

LED_0_AEU3_PWM_2 is shown in Figure 2-54 and described in Table 2-75.

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Figure 2-54. LED_0_AEU3_PWM_2 Register

7	6	5	4	3	2	1	0
led_0_aeu3_pwm2							
R/W-0h							

Table 2-75. LED_0_AEU3_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu3_pwm2	R/W	0h	AEU3_PWM2 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.21 LED_0_AEU3_PWM_3 Register (Offset = 94h) [Reset = 00h]

LED_0_AEU3_PWM_3 is shown in Figure 2-55 and described in Table 2-76.

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Figure 2-55. LED_0_AEU3_PWM_3 Register

7	6	5	4	3	2	1	0
led_0_aeu3_pwm3							
R/W-0h							

Table 2-76. LED_0_AEU3_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu3_pwm3	R/W	0h	AEU3_PWM3 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.22 LED_0_AEU3_PWM_4 Register (Offset = 95h) [Reset = 00h]

LED_0_AEU3_PWM_4 is shown in Figure 2-56 and described in Table 2-77.

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Figure 2-56. LED_0_AEU3_PWM_4 Register

7	6	5	4	3	2	1	0
led_0_aeu3_pwm4							
R/W-0h							

Table 2-77. LED_0_AEU3_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu3_pwm4	R/W	0h	AEU3_PWM4 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.23 LED_0_AEU3_PWM_5 Register (Offset = 96h) [Reset = 00h]

LED_0_AEU3_PWM_5 is shown in Figure 2-57 and described in Table 2-78.

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Figure 2-57. LED_0_AEU3_PWM_5 Register

7	6	5	4	3	2	1	0
led_0_aeu3_pwm5							
R/W-0h							

Table 2-78. LED_0_AEU3_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_0_aeu3_pwm5	R/W	0h	AEU3_PWM5 setting of LED_0; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.11.24 LED_0_AEU3_T12 Register (Offset = 97h) [Reset = 00h]

LED_0_AEU3_T12 is shown in Figure 2-58 and described in Table 2-79.

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Figure 2-58. LED_0_AEU3_T12 Register

7	6	5	4	3	2	1	0
led_0_aeu3_t2				led_0_aeu3_t1			
R/W-0h				R/W-0h			

Table 2-79. LED_0_AEU3_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_0_aeu3_t2	R/W	0h	AEU3_T2 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_0_aeu3_t1	R/W	0h	AEU3_T1 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.11.25 LED_0_AEU3_T34 Register (Offset = 98h) [Reset = 00h]

LED_0_AEU3_T34 is shown in Figure 2-59 and described in Table 2-80.

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Figure 2-59. LED_0_AEU3_T34 Register

7	6	5	4	3	2	1	0
led_0_aeu3_t4				led_0_aeu3_t3			
R/W-0h				R/W-0h			

Table 2-80. LED_0_AEU3_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_0_aeu3_t4	R/W	0h	AEU3_T4 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_0_aeu3_t3	R/W	0h	AEU3_T3 slope time setting of LED_0; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.11.26 LED_0_AEU3_Playback Register (Offset = 99h) [Reset = 00h]

LED_0_AEU3_Playback is shown in Figure 2-60 and described in Table 2-81.

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Figure 2-60. LED_0_AEU3_Playback Register

7	6	5	4	3	2	1	0
RESERVED						led_0_aeu3_pt	
R-0h						R/W-0h	

Table 2-81. LED_0_AEU3_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	led_0_aeu3_pt	R/W	0h	AEU3 pattern playback times of LED_0; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.12 LED_1_Autonomous_Animation Registers

Table 2-82 lists the memory-mapped registers for the LED_1_Autonomous_Animation registers. All register offset addresses not listed in Table 2-82 should be considered as reserved locations and the register contents should not be modified.

Table 2-82. LED_1_AUTONOMOUS_ANIMATION Registers

Offset	Acronym	Register Name	Section
9Ah	LED_1_Auto_Pause	Animation pause time at the start and the end of LED_1	Go
9Bh	LED_1_Auto_Playback	Animation pattern playback times of LED_1 and active AEU number setting	Go
9Ch	LED_1_AEU1_PWM_1	PWM setting of LED_1 AEU1_PWM1	Go
9Dh	LED_1_AEU1_PWM_2	PWM setting of LED_1 AEU1_PWM2	Go
9Eh	LED_1_AEU1_PWM_3	PWM setting of LED_1 AEU1_PWM3	Go
9Fh	LED_1_AEU1_PWM_4	PWM setting of LED_1 AEU1_PWM4	Go
A0h	LED_1_AEU1_PWM_5	PWM setting of LED_1 AEU1_PWM5	Go
A1h	LED_1_AEU1_T12	Slope time setting of LED_1 AEU1_T1 and AEU1_T2	Go
A2h	LED_1_AEU1_T34	Slope time setting of LED_1 AEU1_T3 and AEU1_T4	Go
A3h	LED_1_AEU1_Playback	AEU1 pattern playback times of LED_1	Go
A4h	LED_1_AEU2_PWM_1	PWM setting of LED_1 AEU2_PWM1	Go
A5h	LED_1_AEU2_PWM_2	PWM setting of LED_1 AEU2_PWM2	Go
A6h	LED_1_AEU2_PWM_3	PWM setting of LED_1 AEU2_PWM3	Go
A7h	LED_1_AEU2_PWM_4	PWM setting of LED_1 AEU2_PWM4	Go
A8h	LED_1_AEU2_PWM_5	PWM setting of LED_1 AEU2_PWM5	Go
A9h	LED_1_AEU2_T12	Slope time setting of LED_1 AEU2_T1 and AEU2_T2	Go
AAh	LED_1_AEU2_T34	Slope time setting of LED_1 AEU2_T3 and AEU2_T4	Go
ABh	LED_1_AEU2_Playback	AEU2 pattern playback times of LED_1	Go
ACh	LED_1_AEU3_PWM_1	PWM setting of LED_1 AEU3_PWM1	Go
ADh	LED_1_AEU3_PWM_2	PWM setting of LED_1 AEU3_PWM2	Go
AEh	LED_1_AEU3_PWM_3	PWM setting of LED_1 AEU3_PWM3	Go
AFh	LED_1_AEU3_PWM_4	PWM setting of LED_1 AEU3_PWM4	Go
B0h	LED_1_AEU3_PWM_5	PWM setting of LED_1 AEU3_PWM5	Go
B1h	LED_1_AEU3_T12	Slope time setting of LED_1 AEU3_T1 and AEU3_T2	Go
B2h	LED_1_AEU3_T34	Slope time setting of LED_1 AEU3_T3 and AEU3_T4	Go

Table 2-82. LED_1_AUTONOMOUS_ANIMATION Registers (continued)

Offset	Acronym	Register Name	Section
B3h	LED_1_AEU3_Playback	AEU3 pattern playback times of LED_1	Go

Complex bit access types are encoded to fit into small table cells. Table 2-83 shows the codes that are used for access types in this section.

Table 2-83. LED_1_Autonomous_Animation Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.12.1 LED_1_Auto_Pause Register (Offset = 9Ah) [Reset = 00h]

LED_1_Auto_Pause is shown in Figure 2-61 and described in Table 2-84.

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Figure 2-61. LED_1_Auto_Pause Register

7	6	5	4	3	2	1	0
led_1_tp_ts				led_1_tp_te			
R/W-0h				R/W-0h			

Table 2-84. LED_1_Auto_Pause Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_1_tp_ts	R/W	0h	Animation pause time at the start of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_1_tp_te	R/W	0h	Animation pause time at the end of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.12.2 LED_1_Auto_Playback Register (Offset = 9Bh) [Reset = 00h]

LED_1_Auto_Playback is shown in Figure 2-62 and described in Table 2-85.

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Figure 2-62. LED_1_Auto_Playback Register

7	6	5	4	3	2	1	0
RESERVED		led_1_aeu_num		led_1_pt			
R-0h		R/W-0h		R/W-0h			

Table 2-85. LED_1_Auto_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	led_1_aeu_num	R/W	0h	Active AEU number of LED_1 selection; 0h = only use AEU1; 1h = use AEU1 and AEU2; 2h = use AEU1, AEU2 and AEU3; 3h = use AEU1, AEU2 and AEU3 (the same as 2h)
3-0	led_1_pt	R/W	0h	Animation pattern playback times of LED_1; 0h = 0 times; 1h = 1 times; 2h = 2 times; 3h = 3 times; 4h = 4 times; 5h = 5 times; 6h = 6 times; 7h = 7 times; 8h = 8 times; 9h = 9 times; Ah = 10 times; Bh = 11 times; Ch = 12 times; Dh = 13 times; Eh = 14 times; Fh = infinite times

2.12.3 LED_1_AEU1_PWM_1 Register (Offset = 9Ch) [Reset = 00h]

LED_1_AEU1_PWM_1 is shown in Figure 2-63 and described in Table 2-86.

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Figure 2-63. LED_1_AEU1_PWM_1 Register

7	6	5	4	3	2	1	0
led_1_aeu1_pwm1							
R/W-0h							

Table 2-86. LED_1_AEU1_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu1_pwm1	R/W	0h	AEU1_PWM1 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.4 LED_1_AEU1_PWM_2 Register (Offset = 9Dh) [Reset = 00h]

LED_1_AEU1_PWM_2 is shown in Figure 2-64 and described in Table 2-87.

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Figure 2-64. LED_1_AEU1_PWM_2 Register

7	6	5	4	3	2	1	0
led_1_aeu1_pwm2							
R/W-0h							

Table 2-87. LED_1_AEU1_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu1_pwm2	R/W	0h	AEU1_PWM2 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.5 LED_1_AEU1_PWM_3 Register (Offset = 9Eh) [Reset = 00h]

LED_1_AEU1_PWM_3 is shown in Figure 2-65 and described in Table 2-88.

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Figure 2-65. LED_1_AEU1_PWM_3 Register

7	6	5	4	3	2	1	0
led_1_aeu1_pwm3							
R/W-0h							

Table 2-88. LED_1_AEU1_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu1_pwm3	R/W	0h	AEU1_PWM3 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.6 LED_1_AEU1_PWM_4 Register (Offset = 9Fh) [Reset = 00h]

LED_1_AEU1_PWM_4 is shown in Figure 2-66 and described in Table 2-89.

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Figure 2-66. LED_1_AEU1_PWM_4 Register

7	6	5	4	3	2	1	0
led_1_aeu1_pwm4							
R/W-0h							

Table 2-89. LED_1_AEU1_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu1_pwm4	R/W	0h	AEU1_PWM4 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.7 LED_1_AEU1_PWM_5 Register (Offset = A0h) [Reset = 00h]

LED_1_AEU1_PWM_5 is shown in Figure 2-67 and described in Table 2-90.

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Figure 2-67. LED_1_AEU1_PWM_5 Register

7	6	5	4	3	2	1	0
led_1_aeu1_pwm5							
R/W-0h							

Table 2-90. LED_1_AEU1_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu1_pwm5	R/W	0h	AEU1_PWM5 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.8 LED_1_AEU1_T12 Register (Offset = A1h) [Reset = 00h]

LED_1_AEU1_T12 is shown in Figure 2-68 and described in Table 2-91.

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Figure 2-68. LED_1_AEU1_T12 Register

7	6	5	4	3	2	1	0
led_1_aeu1_t2				led_1_aeu1_t1			
R/W-0h				R/W-0h			

Table 2-91. LED_1_AEU1_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_1_aeu1_t2	R/W	0h	AEU1_T2 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_1_aeu1_t1	R/W	0h	AEU1_T1 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.12.9 LED_1_AEU1_T34 Register (Offset = A2h) [Reset = 00h]

LED_1_AEU1_T34 is shown in Figure 2-69 and described in Table 2-92.

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Figure 2-69. LED_1_AEU1_T34 Register

7	6	5	4	3	2	1	0
led_1_aeu1_t4				led_1_aeu1_t3			
R/W-0h				R/W-0h			

Table 2-92. LED_1_AEU1_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_1_aeu1_t4	R/W	0h	AEU1_T4 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_1_aeu1_t3	R/W	0h	AEU1_T3 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.12.10 LED_1_AEU1_Playback Register (Offset = A3h) [Reset = 00h]

LED_1_AEU1_Playback is shown in Figure 2-70 and described in Table 2-93.

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Figure 2-70. LED_1_AEU1_Playback Register

7	6	5	4	3	2	1	0
RESERVED						led_1_aeu1_pt	
R-0h						R/W-0h	

Table 2-93. LED_1_AEU1_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved

Table 2-93. LED_1_AEU1_Playback Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	led_1_aeu1_pt	R/W	0h	AEU1 pattern playback times of LED_1; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.12.11 LED_1_AEU2_PWM_1 Register (Offset = A4h) [Reset = 00h]

LED_1_AEU2_PWM_1 is shown in Figure 2-71 and described in Table 2-94.

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Figure 2-71. LED_1_AEU2_PWM_1 Register

7	6	5	4	3	2	1	0
led_1_aeu2_pwm1							
R/W-0h							

Table 2-94. LED_1_AEU2_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu2_pwm1	R/W	0h	AEU2_PWM1 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.12 LED_1_AEU2_PWM_2 Register (Offset = A5h) [Reset = 00h]

LED_1_AEU2_PWM_2 is shown in Figure 2-72 and described in Table 2-95.

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Figure 2-72. LED_1_AEU2_PWM_2 Register

7	6	5	4	3	2	1	0
led_1_aeu2_pwm2							
R/W-0h							

Table 2-95. LED_1_AEU2_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu2_pwm2	R/W	0h	AEU2_PWM2 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.13 LED_1_AEU2_PWM_3 Register (Offset = A6h) [Reset = 00h]

LED_1_AEU2_PWM_3 is shown in Figure 2-73 and described in Table 2-96.

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Figure 2-73. LED_1_AEU2_PWM_3 Register

7	6	5	4	3	2	1	0
led_1_aeu2_pwm3							
R/W-0h							

Table 2-96. LED_1_AEU2_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu2_pwm3	R/W	0h	AEU2_PWM3 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.14 LED_1_AEU2_PWM_4 Register (Offset = A7h) [Reset = 00h]

LED_1_AEU2_PWM_4 is shown in Figure 2-74 and described in Table 2-97.

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Figure 2-74. LED_1_AEU2_PWM_4 Register

7	6	5	4	3	2	1	0
led_1_aeu2_pwm4							
R/W-0h							

Table 2-97. LED_1_AEU2_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu2_pwm4	R/W	0h	AEU2_PWM4 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.15 LED_1_AEU2_PWM_5 Register (Offset = A8h) [Reset = 00h]

LED_1_AEU2_PWM_5 is shown in Figure 2-75 and described in Table 2-98.

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Figure 2-75. LED_1_AEU2_PWM_5 Register

7	6	5	4	3	2	1	0
led_1_aeu2_pwm5							
R/W-0h							

Table 2-98. LED_1_AEU2_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu2_pwm5	R/W	0h	AEU2_PWM5 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.16 LED_1_AEU2_T12 Register (Offset = A9h) [Reset = 00h]

LED_1_AEU2_T12 is shown in Figure 2-76 and described in Table 2-99.

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Figure 2-76. LED_1_AEU2_T12 Register

7	6	5	4	3	2	1	0
led_1_aeu2_t2				led_1_aeu2_t1			
R/W-0h				R/W-0h			

Table 2-99. LED_1_AEU2_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_1_aeu2_t2	R/W	0h	AEU2_T2 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_1_aeu2_t1	R/W	0h	AEU2_T1 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.12.17 LED_1_AEU2_T34 Register (Offset = AAh) [Reset = 00h]

LED_1_AEU2_T34 is shown in Figure 2-77 and described in Table 2-100.

Return to the Summary Table.

Figure 2-77. LED_1_AEU2_T34 Register

7	6	5	4	3	2	1	0
led_1_aeu2_t4				led_1_aeu2_t3			
R/W-0h				R/W-0h			

Table 2-100. LED_1_AEU2_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_1_aeu2_t4	R/W	0h	AEU2_T4 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_1_aeu2_t3	R/W	0h	AEU2_T3 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.12.18 LED_1_AEU2_Playback Register (Offset = ABh) [Reset = 00h]

LED_1_AEU2_Playback is shown in Figure 2-78 and described in Table 2-101.

Return to the Summary Table.

Figure 2-78. LED_1_AEU2_Playback Register

7	6	5	4	3	2	1	0
RESERVED						led_1_aeu2_pt	
R-0h						R/W-0h	

Table 2-101. LED_1_AEU2_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	led_1_aeu2_pt	R/W	0h	AEU2 pattern playback times of LED_1; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.12.19 LED_1_AEU3_PWM_1 Register (Offset = ACh) [Reset = 00h]

LED_1_AEU3_PWM_1 is shown in Figure 2-79 and described in Table 2-102.

Return to the Summary Table.

Figure 2-79. LED_1_AEU3_PWM_1 Register

7	6	5	4	3	2	1	0
led_1_aeu3_pwm1							
R/W-0h							

Table 2-102. LED_1_AEU3_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu3_pwm1	R/W	0h	AEU3_PWM1 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.20 LED_1_AEU3_PWM_2 Register (Offset = ADh) [Reset = 00h]

LED_1_AEU3_PWM_2 is shown in Figure 2-80 and described in Table 2-103.

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Figure 2-80. LED_1_AEU3_PWM_2 Register

7	6	5	4	3	2	1	0
led_1_aeu3_pwm2							
R/W-0h							

Table 2-103. LED_1_AEU3_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu3_pwm2	R/W	0h	AEU3_PWM2 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.21 LED_1_AEU3_PWM_3 Register (Offset = AEh) [Reset = 00h]

LED_1_AEU3_PWM_3 is shown in Figure 2-81 and described in Table 2-104.

Return to the Summary Table.

Figure 2-81. LED_1_AEU3_PWM_3 Register

7	6	5	4	3	2	1	0
led_1_aeu3_pwm3							
R/W-0h							

Table 2-104. LED_1_AEU3_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu3_pwm3	R/W	0h	AEU3_PWM3 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.22 LED_1_AEU3_PWM_4 Register (Offset = AFh) [Reset = 00h]

LED_1_AEU3_PWM_4 is shown in Figure 2-82 and described in Table 2-105.

Return to the Summary Table.

Figure 2-82. LED_1_AEU3_PWM_4 Register

7	6	5	4	3	2	1	0
led_1_aeu3_pwm4							
R/W-0h							

Table 2-105. LED_1_AEU3_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu3_pwm4	R/W	0h	AEU3_PWM4 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.23 LED_1_AEU3_PWM_5 Register (Offset = B0h) [Reset = 00h]

LED_1_AEU3_PWM_5 is shown in Figure 2-83 and described in Table 2-106.

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Figure 2-83. LED_1_AEU3_PWM_5 Register

7	6	5	4	3	2	1	0
led_1_aeu3_pwm5							
R/W-0h							

Table 2-106. LED_1_AEU3_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_1_aeu3_pwm5	R/W	0h	AEU3_PWM5 setting of LED_1; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.12.24 LED_1_AEU3_T12 Register (Offset = B1h) [Reset = 00h]

LED_1_AEU3_T12 is shown in Figure 2-84 and described in Table 2-107.

Return to the Summary Table.

Figure 2-84. LED_1_AEU3_T12 Register

7	6	5	4	3	2	1	0
led_1_aeu3_t2				led_1_aeu3_t1			
R/W-0h				R/W-0h			

Table 2-107. LED_1_AEU3_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_1_aeu3_t2	R/W	0h	AEU3_T2 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

Table 2-107. LED_1_AEU3_T12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	led_1_aeu3_t1	R/W	0h	AEU3_T1 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.12.25 LED_1_AEU3_T34 Register (Offset = B2h) [Reset = 00h]

LED_1_AEU3_T34 is shown in Figure 2-85 and described in Table 2-108.

Return to the Summary Table.

Figure 2-85. LED_1_AEU3_T34 Register

7	6	5	4	3	2	1	0
led_1_aeu3_t4				led_1_aeu3_t3			
R/W-0h				R/W-0h			

Table 2-108. LED_1_AEU3_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_1_aeu3_t4	R/W	0h	AEU3_T4 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_1_aeu3_t3	R/W	0h	AEU3_T3 slope time setting of LED_1; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.12.26 LED_1_AEU3_Playback Register (Offset = B3h) [Reset = 00h]

LED_1_AEU3_Playback is shown in Figure 2-86 and described in Table 2-109.

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Figure 2-86. LED_1_AEU3_Playback Register

7	6	5	4	3	2	1	0
RESERVED						led_1_aeu3_pt	
R-0h						R/W-0h	

Table 2-109. LED_1_AEU3_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	led_1_aeu3_pt	R/W	0h	AEU3 pattern playback times of LED_1; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.13 LED_2_Autonomous_Animation Registers

Table 2-110 lists the memory-mapped registers for the LED_2_Autonomous_Animation registers. All register offset addresses not listed in Table 2-110 should be considered as reserved locations and the register contents should not be modified.

Table 2-110. LED_2_AUTONOMOUS_ANIMATION Registers

Offset	Acronym	Register Name	Section
B4h	LED_2_Auto_Pause	Animation pause time at the start and the end of LED_2	Go
B5h	LED_2_Auto_Playback	Animation pattern playback times of LED_2 and active AEU number setting	Go
B6h	LED_2_AEU1_PWM_1	PWM setting of LED_2 AEU1_PWM1	Go
B7h	LED_2_AEU1_PWM_2	PWM setting of LED_2 AEU1_PWM2	Go
B8h	LED_2_AEU1_PWM_3	PWM setting of LED_2 AEU1_PWM3	Go
B9h	LED_2_AEU1_PWM_4	PWM setting of LED_2 AEU1_PWM4	Go
BAh	LED_2_AEU1_PWM_5	PWM setting of LED_2 AEU1_PWM5	Go
BBh	LED_2_AEU1_T12	Slope time setting of LED_2 AEU1_T1 and AEU1_T2	Go
BCh	LED_2_AEU1_T34	Slope time setting of LED_2 AEU1_T3 and AEU1_T4	Go
BDh	LED_2_AEU1_Playback	AEU1 pattern playback times of LED_2	Go
BEh	LED_2_AEU2_PWM_1	PWM setting of LED_2 AEU2_PWM1	Go
BFh	LED_2_AEU2_PWM_2	PWM setting of LED_2 AEU2_PWM2	Go
C0h	LED_2_AEU2_PWM_3	PWM setting of LED_2 AEU2_PWM3	Go
C1h	LED_2_AEU2_PWM_4	PWM setting of LED_2 AEU2_PWM4	Go
C2h	LED_2_AEU2_PWM_5	PWM setting of LED_2 AEU2_PWM5	Go
C3h	LED_2_AEU2_T12	Slope time setting of LED_2 AEU2_T1 and AEU2_T2	Go
C4h	LED_2_AEU2_T34	Slope time setting of LED_2 AEU2_T3 and AEU2_T4	Go
C5h	LED_2_AEU2_Playback	AEU2 pattern playback times of LED_2	Go
C6h	LED_2_AEU3_PWM_1	PWM setting of LED_2 AEU3_PWM1	Go
C7h	LED_2_AEU3_PWM_2	PWM setting of LED_2 AEU3_PWM2	Go
C8h	LED_2_AEU3_PWM_3	PWM setting of LED_2 AEU3_PWM3	Go
C9h	LED_2_AEU3_PWM_4	PWM setting of LED_2 AEU3_PWM4	Go
CAh	LED_2_AEU3_PWM_5	PWM setting of LED_2 AEU3_PWM5	Go
CBh	LED_2_AEU3_T12	Slope time setting of LED_2 AEU3_T1 and AEU3_T2	Go
CCh	LED_2_AEU3_T34	Slope time setting of LED_2 AEU3_T3 and AEU3_T4	Go
CDh	LED_2_AEU3_Playback	AEU3 pattern playback times of LED_2	Go

Complex bit access types are encoded to fit into small table cells. Table 2-111 shows the codes that are used for access types in this section.

Table 2-111. LED_2_Autonomous_Animation Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.13.1 LED_2_Auto_Pause Register (Offset = B4h) [Reset = 00h]

LED_2_Auto_Pause is shown in Figure 2-87 and described in Table 2-112.

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Figure 2-87. LED_2_Auto_Pause Register

7	6	5	4	3	2	1	0
led_2_tp_ts				led_2_tp_te			
R/W-0h				R/W-0h			

Table 2-112. LED_2_Auto_Pause Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_2_tp_ts	R/W	0h	Animation pause time at the start of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_2_tp_te	R/W	0h	Animation pause time at the end of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.13.2 LED_2_Auto_Playback Register (Offset = B5h) [Reset = 00h]

LED_2_Auto_Playback is shown in Figure 2-88 and described in Table 2-113.

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Figure 2-88. LED_2_Auto_Playback Register

7	6	5	4	3	2	1	0
RESERVED		led_2_aeu_num		led_2_pt			
R-0h		R/W-0h		R/W-0h			

Table 2-113. LED_2_Auto_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	led_2_aeu_num	R/W	0h	Active AEU number of LED_2 selection; 0h = only use AEU1; 1h = use AEU1 and AEU2; 2h = use AEU1, AEU2 and AEU3; 3h = use AEU1, AEU2 and AEU3 (the same as 2h)
3-0	led_2_pt	R/W	0h	Animation pattern playback times of LED_2; 0h = 0 times; 1h = 1 times; 2h = 2 times; 3h = 3 times; 4h = 4 times; 5h = 5 times; 6h = 6 times; 7h = 7 times; 8h = 8 times; 9h = 9 times; Ah = 10 times; Bh = 11 times; Ch = 12 times; Dh = 13 times; Eh = 14 times; Fh = infinite times

2.13.3 LED_2_AEU1_PWM_1 Register (Offset = B6h) [Reset = 00h]

LED_2_AEU1_PWM_1 is shown in Figure 2-89 and described in Table 2-114.

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Figure 2-89. LED_2_AEU1_PWM_1 Register

7	6	5	4	3	2	1	0
led_2_aeu1_pwm1							
R/W-0h							

Table 2-114. LED_2_AEU1_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu1_pwm1	R/W	0h	AEU1_PWM1 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.4 LED_2_AEU1_PWM_2 Register (Offset = B7h) [Reset = 00h]

LED_2_AEU1_PWM_2 is shown in Figure 2-90 and described in Table 2-115.

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Figure 2-90. LED_2_AEU1_PWM_2 Register

7	6	5	4	3	2	1	0
led_2_aeu1_pwm2							
R/W-0h							

Table 2-115. LED_2_AEU1_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu1_pwm2	R/W	0h	AEU1_PWM2 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.5 LED_2_AEU1_PWM_3 Register (Offset = B8h) [Reset = 00h]

LED_2_AEU1_PWM_3 is shown in Figure 2-91 and described in Table 2-116.

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Figure 2-91. LED_2_AEU1_PWM_3 Register

7	6	5	4	3	2	1	0
led_2_aeu1_pwm3							
R/W-0h							

Table 2-116. LED_2_AEU1_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu1_pwm3	R/W	0h	AEU1_PWM3 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.6 LED_2_AEU1_PWM_4 Register (Offset = B9h) [Reset = 00h]

LED_2_AEU1_PWM_4 is shown in Figure 2-92 and described in Table 2-117.

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Figure 2-92. LED_2_AEU1_PWM_4 Register

7	6	5	4	3	2	1	0
led_2_aeu1_pwm4							
R/W-0h							

Table 2-117. LED_2_AEU1_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu1_pwm4	R/W	0h	AEU1_PWM4 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.7 LED_2_AEU1_PWM_5 Register (Offset = BAh) [Reset = 00h]

LED_2_AEU1_PWM_5 is shown in Figure 2-93 and described in Table 2-118.

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Figure 2-93. LED_2_AEU1_PWM_5 Register

7	6	5	4	3	2	1	0
led_2_aeu1_pwm5							
R/W-0h							

Table 2-118. LED_2_AEU1_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu1_pwm5	R/W	0h	AEU1_PWM5 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.8 LED_2_AEU1_T12 Register (Offset = BBh) [Reset = 00h]

LED_2_AEU1_T12 is shown in Figure 2-94 and described in Table 2-119.

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Figure 2-94. LED_2_AEU1_T12 Register

7	6	5	4	3	2	1	0
led_2_aeu1_t2				led_2_aeu1_t1			
R/W-0h				R/W-0h			

Table 2-119. LED_2_AEU1_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_2_aeu1_t2	R/W	0h	AEU1_T2 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_2_aeu1_t1	R/W	0h	AEU1_T1 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.13.9 LED_2_AEU1_T34 Register (Offset = BCh) [Reset = 00h]

LED_2_AEU1_T34 is shown in Figure 2-95 and described in Table 2-120.

Return to the Summary Table.

Figure 2-95. LED_2_AEU1_T34 Register

7	6	5	4	3	2	1	0
led_2_aeu1_t4				led_2_aeu1_t3			
R/W-0h				R/W-0h			

Table 2-120. LED_2_AEU1_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_2_aeu1_t4	R/W	0h	AEU1_T4 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_2_aeu1_t3	R/W	0h	AEU1_T3 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.13.10 LED_2_AEU1_Playback Register (Offset = BDh) [Reset = 00h]

LED_2_AEU1_Playback is shown in Figure 2-96 and described in Table 2-121.

Return to the Summary Table.

Figure 2-96. LED_2_AEU1_Playback Register

7	6	5	4	3	2	1	0
RESERVED						led_2_aeu1_pt	
R-0h						R/W-0h	

Table 2-121. LED_2_AEU1_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	led_2_aeu1_pt	R/W	0h	AEU1 pattern playback times of LED_2; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.13.11 LED_2_AEU2_PWM_1 Register (Offset = BEh) [Reset = 00h]

LED_2_AEU2_PWM_1 is shown in Figure 2-97 and described in Table 2-122.

Return to the Summary Table.

Figure 2-97. LED_2_AEU2_PWM_1 Register

7	6	5	4	3	2	1	0
led_2_aeu2_pwm1							
R/W-0h							

Table 2-122. LED_2_AEU2_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu2_pwm1	R/W	0h	AEU2_PWM1 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.12 LED_2_AEU2_PWM_2 Register (Offset = BFh) [Reset = 00h]

LED_2_AEU2_PWM_2 is shown in Figure 2-98 and described in Table 2-123.

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Figure 2-98. LED_2_AEU2_PWM_2 Register

7	6	5	4	3	2	1	0
led_2_aeu2_pwm2							
R/W-0h							

Table 2-123. LED_2_AEU2_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu2_pwm2	R/W	0h	AEU2_PWM2 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.13 LED_2_AEU2_PWM_3 Register (Offset = C0h) [Reset = 00h]

LED_2_AEU2_PWM_3 is shown in Figure 2-99 and described in Table 2-124.

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Figure 2-99. LED_2_AEU2_PWM_3 Register

7	6	5	4	3	2	1	0
led_2_aeu2_pwm3							
R/W-0h							

Table 2-124. LED_2_AEU2_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu2_pwm3	R/W	0h	AEU2_PWM3 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.14 LED_2_AEU2_PWM_4 Register (Offset = C1h) [Reset = 00h]

LED_2_AEU2_PWM_4 is shown in Figure 2-100 and described in Table 2-125.

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Figure 2-100. LED_2_AEU2_PWM_4 Register

7	6	5	4	3	2	1	0
led_2_aeu2_pwm4							
R/W-0h							

Table 2-125. LED_2_AEU2_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu2_pwm4	R/W	0h	AEU2_PWM4 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.15 LED_2_AEU2_PWM_5 Register (Offset = C2h) [Reset = 00h]

LED_2_AEU2_PWM_5 is shown in Figure 2-101 and described in Table 2-126.

Return to the Summary Table.

Figure 2-101. LED_2_AEU2_PWM_5 Register

7	6	5	4	3	2	1	0
led_2_aeu2_pwm5							
R/W-0h							

Table 2-126. LED_2_AEU2_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu2_pwm5	R/W	0h	AEU2_PWM5 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.16 LED_2_AEU2_T12 Register (Offset = C3h) [Reset = 00h]

LED_2_AEU2_T12 is shown in Figure 2-102 and described in Table 2-127.

Return to the Summary Table.

Figure 2-102. LED_2_AEU2_T12 Register

7	6	5	4	3	2	1	0
led_2_aeu2_t2				led_2_aeu2_t1			
R/W-0h				R/W-0h			

Table 2-127. LED_2_AEU2_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_2_aeu2_t2	R/W	0h	AEU2_T2 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_2_aeu2_t1	R/W	0h	AEU2_T1 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.13.17 LED_2_AEU2_T34 Register (Offset = C4h) [Reset = 00h]

LED_2_AEU2_T34 is shown in Figure 2-103 and described in Table 2-128.

Return to the Summary Table.

Figure 2-103. LED_2_AEU2_T34 Register

7	6	5	4	3	2	1	0
led_2_aeu2_t4				led_2_aeu2_t3			
R/W-0h				R/W-0h			

Table 2-128. LED_2_AEU2_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_2_aeu2_t4	R/W	0h	AEU2_T4 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_2_aeu2_t3	R/W	0h	AEU2_T3 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.13.18 LED_2_AEU2_Playback Register (Offset = C5h) [Reset = 00h]

LED_2_AEU2_Playback is shown in Figure 2-104 and described in Table 2-129.

Return to the Summary Table.

Figure 2-104. LED_2_AEU2_Playback Register

7	6	5	4	3	2	1	0
RESERVED						led_2_aeu2_pt	
R-0h						R/W-0h	

Table 2-129. LED_2_AEU2_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	led_2_aeu2_pt	R/W	0h	AEU2 pattern playback times of LED_2; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.13.19 LED_2_AEU3_PWM_1 Register (Offset = C6h) [Reset = 00h]

LED_2_AEU3_PWM_1 is shown in Figure 2-105 and described in Table 2-130.

Return to the Summary Table.

Figure 2-105. LED_2_AEU3_PWM_1 Register

7	6	5	4	3	2	1	0
led_2_aeu3_pwm1							
R/W-0h							

Table 2-130. LED_2_AEU3_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu3_pwm1	R/W	0h	AEU3_PWM1 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.20 LED_2_AEU3_PWM_2 Register (Offset = C7h) [Reset = 00h]

LED_2_AEU3_PWM_2 is shown in Figure 2-106 and described in Table 2-131.

Return to the Summary Table.

Figure 2-106. LED_2_AEU3_PWM_2 Register

7	6	5	4	3	2	1	0
led_2_aeu3_pwm2							
R/W-0h							

Table 2-131. LED_2_AEU3_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu3_pwm2	R/W	0h	AEU3_PWM2 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.21 LED_2_AEU3_PWM_3 Register (Offset = C8h) [Reset = 00h]

LED_2_AEU3_PWM_3 is shown in Figure 2-107 and described in Table 2-132.

Return to the Summary Table.

Figure 2-107. LED_2_AEU3_PWM_3 Register

7	6	5	4	3	2	1	0
led_2_aeu3_pwm3							
R/W-0h							

Table 2-132. LED_2_AEU3_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu3_pwm3	R/W	0h	AEU3_PWM3 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.22 LED_2_AEU3_PWM_4 Register (Offset = C9h) [Reset = 00h]

LED_2_AEU3_PWM_4 is shown in Figure 2-108 and described in Table 2-133.

Return to the Summary Table.

Figure 2-108. LED_2_AEU3_PWM_4 Register

7	6	5	4	3	2	1	0
led_2_aeu3_pwm4							
R/W-0h							

Table 2-133. LED_2_AEU3_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu3_pwm4	R/W	0h	AEU3_PWM4 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.23 LED_2_AEU3_PWM_5 Register (Offset = CAh) [Reset = 00h]

LED_2_AEU3_PWM_5 is shown in Figure 2-109 and described in Table 2-134.

Return to the Summary Table.

Figure 2-109. LED_2_AEU3_PWM_5 Register

7	6	5	4	3	2	1	0
led_2_aeu3_pwm5							
R/W-0h							

Table 2-134. LED_2_AEU3_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_2_aeu3_pwm5	R/W	0h	AEU3_PWM5 setting of LED_2; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.13.24 LED_2_AEU3_T12 Register (Offset = CBh) [Reset = 00h]

LED_2_AEU3_T12 is shown in Figure 2-110 and described in Table 2-135.

Return to the Summary Table.

Figure 2-110. LED_2_AEU3_T12 Register

7	6	5	4	3	2	1	0
led_2_aeu3_t2				led_2_aeu3_t1			
R/W-0h				R/W-0h			

Table 2-135. LED_2_AEU3_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_2_aeu3_t2	R/W	0h	AEU3_T2 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_2_aeu3_t1	R/W	0h	AEU3_T1 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.13.25 LED_2_AEU3_T34 Register (Offset = CCh) [Reset = 00h]

LED_2_AEU3_T34 is shown in Figure 2-111 and described in Table 2-136.

Return to the Summary Table.

Figure 2-111. LED_2_AEU3_T34 Register

7	6	5	4	3	2	1	0
led_2_aeu3_t4				led_2_aeu3_t3			
R/W-0h				R/W-0h			

Table 2-136. LED_2_AEU3_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_2_aeu3_t4	R/W	0h	AEU3_T4 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

Table 2-136. LED_2_AEU3_T34 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	led_2_aeu3_t3	R/W	0h	AEU3_T3 slope time setting of LED_2; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.13.26 LED_2_AEU3_Playback Register (Offset = CDh) [Reset = 00h]

LED_2_AEU3_Playback is shown in Figure 2-112 and described in Table 2-137.

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Figure 2-112. LED_2_AEU3_Playback Register

7	6	5	4	3	2	1	0
RESERVED						led_2_aeu3_pt	
R-0h						R/W-0h	

Table 2-137. LED_2_AEU3_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	led_2_aeu3_pt	R/W	0h	AEU3 pattern playback times of LED_2; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.14 LED_3_Autonomous_Animation Registers

Table 2-138 lists the memory-mapped registers for the LED_3_Autonomous_Animation registers. All register offset addresses not listed in Table 2-138 should be considered as reserved locations and the register contents should not be modified.

Table 2-138. LED_3_AUTONOMOUS_ANIMATION Registers

Offset	Acronym	Register Name	Section
CEh	LED_3_Auto_Pause	Animation pause time at the start and the end of LED_3	Go
CFh	LED_3_Auto_Playback	Animation pattern playback times of LED_3 and active AEU number setting	Go
D0h	LED_3_AEU1_PWM_1	PWM setting of LED_3 AEU1_PWM1	Go
D1h	LED_3_AEU1_PWM_2	PWM setting of LED_3 AEU1_PWM2	Go
D2h	LED_3_AEU1_PWM_3	PWM setting of LED_3 AEU1_PWM3	Go
D3h	LED_3_AEU1_PWM_4	PWM setting of LED_3 AEU1_PWM4	Go
D4h	LED_3_AEU1_PWM_5	PWM setting of LED_3 AEU1_PWM5	Go
D5h	LED_3_AEU1_T12	Slope time setting of LED_3 AEU1_T1 and AEU1_T2	Go
D6h	LED_3_AEU1_T34	Slope time setting of LED_3 AEU1_T3 and AEU1_T4	Go
D7h	LED_3_AEU1_Playback	AEU1 pattern playback times of LED_3	Go
D8h	LED_3_AEU2_PWM_1	PWM setting of LED_3 AEU2_PWM1	Go
D9h	LED_3_AEU2_PWM_2	PWM setting of LED_3 AEU2_PWM2	Go
DAh	LED_3_AEU2_PWM_3	PWM setting of LED_3 AEU2_PWM3	Go
DBh	LED_3_AEU2_PWM_4	PWM setting of LED_3 AEU2_PWM4	Go
DCh	LED_3_AEU2_PWM_5	PWM setting of LED_3 AEU2_PWM5	Go
DDh	LED_3_AEU2_T12	Slope time setting of LED_3 AEU2_T1 and AEU2_T2	Go
DEh	LED_3_AEU2_T34	Slope time setting of LED_3 AEU2_T3 and AEU2_T4	Go
DFh	LED_3_AEU2_Playback	AEU2 pattern playback times of LED_3	Go

Table 2-138. LED_3_AUTONOMOUS_ANIMATION Registers (continued)

Offset	Acronym	Register Name	Section
E0h	LED_3_AEU3_PWM_1	PWM setting of LED_3 AEU3_PWM1	Go
E1h	LED_3_AEU3_PWM_2	PWM setting of LED_3 AEU3_PWM2	Go
E2h	LED_3_AEU3_PWM_3	PWM setting of LED_3 AEU3_PWM3	Go
E3h	LED_3_AEU3_PWM_4	PWM setting of LED_3 AEU3_PWM4	Go
E4h	LED_3_AEU3_PWM_5	PWM setting of LED_3 AEU3_PWM5	Go
E5h	LED_3_AEU3_T12	Slope time setting of LED_3 AEU3_T1 and AEU3_T2	Go
E6h	LED_3_AEU3_T34	Slope time setting of LED_3 AEU3_T3 and AEU3_T4	Go
E7h	LED_3_AEU3_Playback	AEU3 pattern playback times of LED_3	Go

Complex bit access types are encoded to fit into small table cells. Table 2-139 shows the codes that are used for access types in this section.

Table 2-139. LED_3_Autonomous_Animation Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.14.1 LED_3_Auto_Pause Register (Offset = CEh) [Reset = 00h]

LED_3_Auto_Pause is shown in Figure 2-113 and described in Table 2-140.

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Figure 2-113. LED_3_Auto_Pause Register

7	6	5	4	3	2	1	0
led_3_tp_ts				led_3_tp_te			
R/W-0h				R/W-0h			

Table 2-140. LED_3_Auto_Pause Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_3_tp_ts	R/W	0h	Animation pause time at the start of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_3_tp_te	R/W	0h	Animation pause time at the end of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.14.2 LED_3_Auto_Playback Register (Offset = CFh) [Reset = 00h]

LED_3_Auto_Playback is shown in Figure 2-114 and described in Table 2-141.

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Figure 2-114. LED_3_Auto_Playback Register

7	6	5	4	3	2	1	0
RESERVED		led_3_aeu_num		led_3_pt			
R-0h		R/W-0h		R/W-0h			

Table 2-141. LED_3_Auto_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	led_3_aeu_num	R/W	0h	Active AEU number of LED_3 selection; 0h = only use AEU1; 1h = use AEU1 and AEU2; 2h = use AEU1, AEU2 and AEU3; 3h = use AEU1, AEU2 and AEU3 (the same as 2h)
3-0	led_3_pt	R/W	0h	Animation pattern playback times of LED_3; 0h = 0 times; 1h = 1 times; 2h = 2 times; 3h = 3 times; 4h = 4 times; 5h = 5 times; 6h = 6 times; 7h = 7 times; 8h = 8 times; 9h = 9 times; Ah = 10 times; Bh = 11 times; Ch = 12 times; Dh = 13 times; Eh = 14 times; Fh = infinite times

2.14.3 LED_3_AEU1_PWM_1 Register (Offset = D0h) [Reset = 00h]

LED_3_AEU1_PWM_1 is shown in Figure 2-115 and described in Table 2-142.

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Figure 2-115. LED_3_AEU1_PWM_1 Register

7	6	5	4	3	2	1	0
led_3_aeu1_pwm1							
R/W-0h							

Table 2-142. LED_3_AEU1_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu1_pwm1	R/W	0h	AEU1_PWM1 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.4 LED_3_AEU1_PWM_2 Register (Offset = D1h) [Reset = 00h]

LED_3_AEU1_PWM_2 is shown in Figure 2-116 and described in Table 2-143.

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Figure 2-116. LED_3_AEU1_PWM_2 Register

7	6	5	4	3	2	1	0
led_3_aeu1_pwm2							
R/W-0h							

Table 2-143. LED_3_AEU1_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu1_pwm2	R/W	0h	AEU1_PWM2 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.5 LED_3_AEU1_PWM_3 Register (Offset = D2h) [Reset = 00h]

LED_3_AEU1_PWM_3 is shown in Figure 2-117 and described in Table 2-144.

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Figure 2-117. LED_3_AEU1_PWM_3 Register

7	6	5	4	3	2	1	0
led_3_aeu1_pwm3							
R/W-0h							

Table 2-144. LED_3_AEU1_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu1_pwm3	R/W	0h	AEU1_PWM3 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.6 LED_3_AEU1_PWM_4 Register (Offset = D3h) [Reset = 00h]

LED_3_AEU1_PWM_4 is shown in Figure 2-118 and described in Table 2-145.

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Figure 2-118. LED_3_AEU1_PWM_4 Register

7	6	5	4	3	2	1	0
led_3_aeu1_pwm4							
R/W-0h							

Table 2-145. LED_3_AEU1_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu1_pwm4	R/W	0h	AEU1_PWM4 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.7 LED_3_AEU1_PWM_5 Register (Offset = D4h) [Reset = 00h]

LED_3_AEU1_PWM_5 is shown in Figure 2-119 and described in Table 2-146.

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Figure 2-119. LED_3_AEU1_PWM_5 Register

7	6	5	4	3	2	1	0
led_3_aeu1_pwm5							
R/W-0h							

Table 2-146. LED_3_AEU1_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu1_pwm5	R/W	0h	AEU1_PWM5 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.8 LED_3_AEU1_T12 Register (Offset = D5h) [Reset = 00h]

LED_3_AEU1_T12 is shown in Figure 2-120 and described in Table 2-147.

Return to the Summary Table.

Figure 2-120. LED_3_AEU1_T12 Register

7	6	5	4	3	2	1	0
led_3_aeu1_t2				led_3_aeu1_t1			
R/W-0h				R/W-0h			

Table 2-147. LED_3_AEU1_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_3_aeu1_t2	R/W	0h	AEU1_T2 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_3_aeu1_t1	R/W	0h	AEU1_T1 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.14.9 LED_3_AEU1_T34 Register (Offset = D6h) [Reset = 00h]

LED_3_AEU1_T34 is shown in Figure 2-121 and described in Table 2-148.

Return to the Summary Table.

Figure 2-121. LED_3_AEU1_T34 Register

7	6	5	4	3	2	1	0
led_3_aeu1_t4				led_3_aeu1_t3			
R/W-0h				R/W-0h			

Table 2-148. LED_3_AEU1_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_3_aeu1_t4	R/W	0h	AEU1_T4 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_3_aeu1_t3	R/W	0h	AEU1_T3 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.14.10 LED_3_AEU1_Playback Register (Offset = D7h) [Reset = 00h]

LED_3_AEU1_Playback is shown in Figure 2-122 and described in Table 2-149.

Return to the Summary Table.

Figure 2-122. LED_3_AEU1_Playback Register

7	6	5	4	3	2	1	0
RESERVED						led_3_aeu1_pt	
R-0h						R/W-0h	

Table 2-149. LED_3_AEU1_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	led_3_aeu1_pt	R/W	0h	AEU1 pattern playback times of LED_3; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.14.11 LED_3_AEU2_PWM_1 Register (Offset = D8h) [Reset = 00h]

LED_3_AEU2_PWM_1 is shown in Figure 2-123 and described in Table 2-150.

Return to the Summary Table.

Figure 2-123. LED_3_AEU2_PWM_1 Register

7	6	5	4	3	2	1	0
led_3_aeu2_pwm1							
R/W-0h							

Table 2-150. LED_3_AEU2_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu2_pwm1	R/W	0h	AEU2_PWM1 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.12 LED_3_AEU2_PWM_2 Register (Offset = D9h) [Reset = 00h]

LED_3_AEU2_PWM_2 is shown in Figure 2-124 and described in Table 2-151.

Return to the Summary Table.

Figure 2-124. LED_3_AEU2_PWM_2 Register

7	6	5	4	3	2	1	0
led_3_aeu2_pwm2							
R/W-0h							

Table 2-151. LED_3_AEU2_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu2_pwm2	R/W	0h	AEU2_PWM2 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.13 LED_3_AEU2_PWM_3 Register (Offset = DAh) [Reset = 00h]

LED_3_AEU2_PWM_3 is shown in Figure 2-125 and described in Table 2-152.

Return to the Summary Table.

Figure 2-125. LED_3_AEU2_PWM_3 Register

7	6	5	4	3	2	1	0
led_3_aeu2_pwm3							
R/W-0h							

Table 2-152. LED_3_AEU2_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu2_pwm3	R/W	0h	AEU2_PWM3 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.14 LED_3_AEU2_PWM_4 Register (Offset = DBh) [Reset = 00h]

LED_3_AEU2_PWM_4 is shown in Figure 2-126 and described in Table 2-153.

Return to the Summary Table.

Figure 2-126. LED_3_AEU2_PWM_4 Register

7	6	5	4	3	2	1	0
led_3_aeu2_pwm4							
R/W-0h							

Table 2-153. LED_3_AEU2_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu2_pwm4	R/W	0h	AEU2_PWM4 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.15 LED_3_AEU2_PWM_5 Register (Offset = DCh) [Reset = 00h]

LED_3_AEU2_PWM_5 is shown in Figure 2-127 and described in Table 2-154.

Return to the Summary Table.

Figure 2-127. LED_3_AEU2_PWM_5 Register

7	6	5	4	3	2	1	0
led_3_aeu2_pwm5							
R/W-0h							

Table 2-154. LED_3_AEU2_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu2_pwm5	R/W	0h	AEU2_PWM5 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.16 LED_3_AEU2_T12 Register (Offset = DDh) [Reset = 00h]

LED_3_AEU2_T12 is shown in Figure 2-128 and described in Table 2-155.

Return to the Summary Table.

Figure 2-128. LED_3_AEU2_T12 Register

7	6	5	4	3	2	1	0
led_3_aeu2_t2				led_3_aeu2_t1			
R/W-0h				R/W-0h			

Table 2-155. LED_3_AEU2_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_3_aeu2_t2	R/W	0h	AEU2_T2 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_3_aeu2_t1	R/W	0h	AEU2_T1 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.14.17 LED_3_AEU2_T34 Register (Offset = DEh) [Reset = 00h]

LED_3_AEU2_T34 is shown in Figure 2-129 and described in Table 2-156.

Return to the Summary Table.

Figure 2-129. LED_3_AEU2_T34 Register

7	6	5	4	3	2	1	0
led_3_aeu2_t4				led_3_aeu2_t3			
R/W-0h				R/W-0h			

Table 2-156. LED_3_AEU2_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_3_aeu2_t4	R/W	0h	AEU2_T4 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_3_aeu2_t3	R/W	0h	AEU2_T3 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.14.18 LED_3_AEU2_Playback Register (Offset = DFh) [Reset = 00h]

LED_3_AEU2_Playback is shown in Figure 2-130 and described in Table 2-157.

Return to the Summary Table.

Figure 2-130. LED_3_AEU2_Playback Register

7	6	5	4	3	2	1	0
RESERVED							led_3_aeu2_pt
R-0h							R/W-0h

Figure 2-130. LED_3_AEU2_Playback Register (continued)

Table 2-157. LED_3_AEU2_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	led_3_aeu2_pt	R/W	0h	AEU2 pattern playback times of LED_3; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.14.19 LED_3_AEU3_PWM_1 Register (Offset = E0h) [Reset = 00h]

LED_3_AEU3_PWM_1 is shown in Figure 2-131 and described in Table 2-158.

Return to the Summary Table.

Figure 2-131. LED_3_AEU3_PWM_1 Register

7	6	5	4	3	2	1	0
led_3_aeu3_pwm1							
R/W-0h							

Table 2-158. LED_3_AEU3_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu3_pwm1	R/W	0h	AEU3_PWM1 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.20 LED_3_AEU3_PWM_2 Register (Offset = E1h) [Reset = 00h]

LED_3_AEU3_PWM_2 is shown in Figure 2-132 and described in Table 2-159.

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Figure 2-132. LED_3_AEU3_PWM_2 Register

7	6	5	4	3	2	1	0
led_3_aeu3_pwm2							
R/W-0h							

Table 2-159. LED_3_AEU3_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu3_pwm2	R/W	0h	AEU3_PWM2 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.21 LED_3_AEU3_PWM_3 Register (Offset = E2h) [Reset = 00h]

LED_3_AEU3_PWM_3 is shown in Figure 2-133 and described in Table 2-160.

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Figure 2-133. LED_3_AEU3_PWM_3 Register

7	6	5	4	3	2	1	0
led_3_aeu3_pwm3							
R/W-0h							

Figure 2-133. LED_3_AEU3_PWM_3 Register (continued)

Table 2-160. LED_3_AEU3_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu3_pwm3	R/W	0h	AEU3_PWM3 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.22 LED_3_AEU3_PWM_4 Register (Offset = E3h) [Reset = 00h]

LED_3_AEU3_PWM_4 is shown in Figure 2-134 and described in Table 2-161.

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Figure 2-134. LED_3_AEU3_PWM_4 Register

7	6	5	4	3	2	1	0
led_3_aeu3_pwm4							
R/W-0h							

Table 2-161. LED_3_AEU3_PWM_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu3_pwm4	R/W	0h	AEU3_PWM4 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.23 LED_3_AEU3_PWM_5 Register (Offset = E4h) [Reset = 00h]

LED_3_AEU3_PWM_5 is shown in Figure 2-135 and described in Table 2-162.

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Figure 2-135. LED_3_AEU3_PWM_5 Register

7	6	5	4	3	2	1	0
led_3_aeu3_pwm5							
R/W-0h							

Table 2-162. LED_3_AEU3_PWM_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	led_3_aeu3_pwm5	R/W	0h	AEU3_PWM5 setting of LED_3; 0h = 0; 1h = 0.39%; 2h = 0.78%; ... 80h = 50.2%; ... FDh = 99.2%; FEh = 99.6%; FFh = 100%

2.14.24 LED_3_AEU3_T12 Register (Offset = E5h) [Reset = 00h]

LED_3_AEU3_T12 is shown in Figure 2-136 and described in Table 2-163.

Return to the Summary Table.

Figure 2-136. LED_3_AEU3_T12 Register

7	6	5	4	3	2	1	0
led_3_aeu3_t2				led_3_aeu3_t1			
R/W-0h				R/W-0h			

Figure 2-136. LED_3_AEU3_T12 Register (continued)

Table 2-163. LED_3_AEU3_T12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_3_aeu3_t2	R/W	0h	AEU3_T2 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_3_aeu3_t1	R/W	0h	AEU3_T1 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.14.25 LED_3_AEU3_T34 Register (Offset = E6h) [Reset = 00h]

LED_3_AEU3_T34 is shown in Figure 2-137 and described in Table 2-164.

Return to the Summary Table.

Figure 2-137. LED_3_AEU3_T34 Register

7	6	5	4	3	2	1	0
led_3_aeu3_t4				led_3_aeu3_t3			
R/W-0h				R/W-0h			

Table 2-164. LED_3_AEU3_T34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	led_3_aeu3_t4	R/W	0h	AEU3_T4 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;
3-0	led_3_aeu3_t3	R/W	0h	AEU3_T3 slope time setting of LED_3; 0h = no pause time; 1h = 0.09s; 2h = 0.18s; 3h = 0.36s; 4h = 0.54s; 5h = 0.80s; 6h = 1.07s; 7h = 1.52s; 8h = 2.06s; 9h = 2.50s; Ah = 3.04s; Bh = 4.02s; Ch = 5.01s; Dh = 5.99s; Eh = 7.06s; Fh = 8.05s;

2.14.26 LED_3_AEU3_Playback Register (Offset = E7h) [Reset = 00h]

LED_3_AEU3_Playback is shown in Figure 2-138 and described in Table 2-165.

Return to the Summary Table.

Figure 2-138. LED_3_AEU3_Playback Register

7	6	5	4	3	2	1	0
RESERVED						led_3_aeu3_pt	
R-0h						R/W-0h	

Table 2-165. LED_3_AEU3_Playback Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	led_3_aeu3_pt	R/W	0h	AEU3 pattern playback times of LED_3; 0h = 0 time; 1h = 1 time; 2h = 2 times; 3h = Infinite times

2.15 Flag Registers

Table 2-166 lists the memory-mapped registers for the Flag registers. All register offset addresses not listed in Table 2-166 should be considered as reserved locations and the register contents should not be modified.

Table 2-166. FLAG Registers

Offset	Acronym	Register Name	Section
300h	TSD_Config_Status	Configuration fault and TSD flags	Go
301h	LOD_Status_0	LOD flags of LED_0 to LED_3	Go
302h	LOD_Status_1	Reserved	
303h	LSD_Status_0	LSD flags of LED_0 to LED_3	Go
304h	LSD_Status_1	Reserved	
305h	Auto_PWM_0	PWM value in autonomous mode of LED_0	Go
306h	Auto_PWM_1	PWM value in autonomous mode of LED_1	Go
307h	Auto_PWM_2	PWM value in autonomous mode of LED_2	Go
308h	Auto_PWM_3	PWM value in autonomous mode of LED_3	Go
315h	AEP_Status_0	Autonomous engine pattern status of LED_0 and LED_1	Go
316h	AEP_Status_1	Autonomous engine pattern status of LED_2 and LED_3	Go

Complex bit access types are encoded to fit into small table cells. Table 2-167 shows the codes that are used for access types in this section.

Table 2-167. Flag Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

2.15.1 TSD_Config_Status Register (Offset = 300h) [Reset = 00h]

TSD_Config_Status is shown in Figure 2-139 and described in Table 2-168.

Return to the Summary Table.

Figure 2-139. TSD_Config_Status Register

7	6	5	4	3	2	1	0
RESERVED						tsd_status	config_err_status
R-0h						R-0h	R-0h

Table 2-168. TSD_Config_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	tsd_status	R	0h	Boost/Linear TSD fault flag; 0h = Boost/Linear TSD are not detected; 1h = Boost/Linear TSD are detected
0	config_err_status	R	0h	Configuration fault flag; 0h = LED_CONFIG and SCAN_ORDERx registers are properly set; 1h = LED_CONFIG and SCAN_ORDERx registers are improperly set

2.15.2 LOD_Status_0 Register (Offset = 301h) [Reset = 00h]

LOD_Status_0 is shown in Figure 2-140 and described in Table 2-169.

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Figure 2-140. LOD_Status_0 Register

7	6	5	4	3	2	1	0
RESERVED				lod_status_3	lod_status_2	lod_status_1	lod_status_0
R-0h				R-0h	R-0h	R-0h	R-0h

Table 2-169. LOD_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	lod_status_3	R	0h	LED_3 LOD status flag; 0h = LOD fault is not detected; 1h = LOD fault is detected
2	lod_status_2	R	0h	LED_2 LOD status flag; 0h = LOD fault is not detected; 1h = LOD fault is detected
1	lod_status_1	R	0h	LED_1 LOD status flag; 0h = LOD fault is not detected; 1h = LOD fault is detected
0	lod_status_0	R	0h	LED_0 LOD status flag; 0h = LOD fault is not detected; 1h = LOD fault is detected

2.15.3 LOD_Status_1 Register (Offset = 302h) [Reset = 00h]

LOD_Status_1 is shown in Figure 2-141 and described in Table 2-170.

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Figure 2-141. LOD_Status_1 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 2-170. LOD_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

2.15.4 LSD_Status_0 Register (Offset = 303h) [Reset = 00h]

LSD_Status_0 is shown in Figure 2-142 and described in Table 2-171.

Return to the Summary Table.

Figure 2-142. LSD_Status_0 Register

7	6	5	4	3	2	1	0
RESERVED				lsd_status_3	lsd_status_2	lsd_status_1	lsd_status_0
R-0h				R-0h	R-0h	R-0h	R-0h

Table 2-171. LSD_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	lsd_status_3	R	0h	LED_3 LSD status flag; 0h = LSD fault is not detected; 1h = LSD fault is detected

Table 2-171. LSD_Status_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	lsd_status_2	R	0h	LED_2 LSD status flag; 0h = LSD fault is not detected; 1h = LSD fault is detected
1	lsd_status_1	R	0h	LED_1 LSD status flag; 0h = LSD fault is not detected; 1h = LSD fault is detected
0	lsd_status_0	R	0h	LED_0 LSD status flag; 0h = LSD fault is not detected; 1h = LSD fault is detected

2.15.5 LSD_Status_1 Register (Offset = 304h) [Reset = 00h]

LSD_Status_1 is shown in Figure 2-143 and described in Table 2-172.

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Figure 2-143. LSD_Status_1 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 2-172. LSD_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

2.15.6 Auto_PWM_0 Register (Offset = 305h) [Reset = 00h]

Auto_PWM_0 is shown in Figure 2-144 and described in Table 2-173.

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Figure 2-144. Auto_PWM_0 Register

7	6	5	4	3	2	1	0
pwm_auto_0							
R-0h							

Table 2-173. Auto_PWM_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	pwm_auto_0	R	0h	PWM value in autonomous mode of LED_0, precise when pause the animation

2.15.7 Auto_PWM_1 Register (Offset = 306h) [Reset = 00h]

Auto_PWM_1 is shown in Figure 2-145 and described in Table 2-174.

Return to the Summary Table.

Figure 2-145. Auto_PWM_1 Register

7	6	5	4	3	2	1	0
pwm_auto_1							
R-0h							

Table 2-174. Auto_PWM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	pwm_auto_1	R	0h	PWM value in autonomous mode of LED_1, precise when pause the animation

2.15.8 Auto_PWM_2 Register (Offset = 307h) [Reset = 00h]

Auto_PWM_2 is shown in Figure 2-146 and described in Table 2-175.

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Figure 2-146. Auto_PWM_2 Register

7	6	5	4	3	2	1	0
pwm_auto_2							
R-0h							

Table 2-175. Auto_PWM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	pwm_auto_2	R	0h	PWM value in autonomous mode of LED_2, precise when pause the animation

2.15.9 Auto_PWM_3 Register (Offset = 308h) [Reset = 00h]

Auto_PWM_3 is shown in Figure 2-147 and described in Table 2-176.

Return to the Summary Table.

Figure 2-147. Auto_PWM_3 Register

7	6	5	4	3	2	1	0
pwm_auto_3							
R-0h							

Table 2-176. Auto_PWM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	pwm_auto_3	R	0h	PWM value in autonomous mode of LED_3, precise when pause the animation

2.15.10 AEP_Status_0 Register (Offset = 315h) [Reset = 3Fh]

AEP_Status_0 is shown in Figure 2-148 and described in Table 2-177.

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Figure 2-148. AEP_Status_0 Register

7	6	5	4	3	2	1	0
RESERVED		aep_status_1			aep_status_0		
R-0h		R-7h			R-7h		

Table 2-177. AEP_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved

Table 2-177. AEP_Status_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	aep_status_1	R	7h	Autonomous engine pattern status of LED_1; 0h = During APU1; 1h = During AEU1; 2h = During AEU2; 3h = During AEU3; 4h = During APU2; 5/6/7h = Error
2-0	aep_status_0	R	7h	Autonomous engine pattern status of LED_0; 0h = During APU1; 1h = During AEU1; 2h = During AEU2; 3h = During AEU3; 4h = During APU2; 5/6/7h = Error

2.15.11 AEP_Status_1 Register (Offset = 316h) [Reset = 3Fh]

AEP_Status_1 is shown in Figure 2-149 and described in Table 2-178.

Return to the Summary Table.

Figure 2-149. AEP_Status_1 Register

7	6	5	4	3	2	1	0
RESERVED		aep_status_3			aep_status_2		
R-0h		R-7h			R-7h		

Table 2-178. AEP_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-3	aep_status_3	R	7h	Autonomous engine pattern status of LED_3; 0h = During APU1; 1h = During AEU1; 2h = During AEU2; 3h = During AEU3; 4h = During APU2; 5/6/7h = Error
2-0	aep_status_2	R	7h	Autonomous engine pattern status of LED_2; 0h = During APU1; 1h = During AEU1; 2h = During AEU2; 3h = During AEU3; 4h = During APU2; 5/6/7h = Error

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2024	*	Initial Release

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