EVM User's Guide: TPS371KEVM

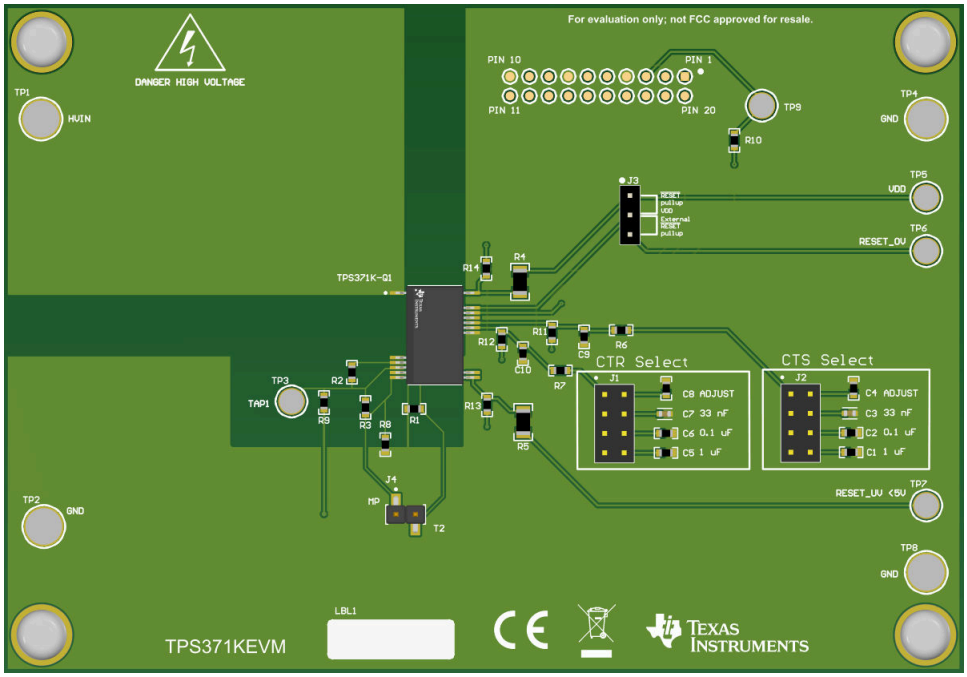
TPS371K Evaluation Module

Description

The TPS371KEVM is an evaluation module (EVM) for the TPS371K-Q1 family of voltage supervisors. The purpose of the this EVM is to provide a sample design and test point for all input and output pins of the TPS371K-Q1 device to capture measurements and gain familiarity with the device.

Features

- Functional Safety-Compliant
  - Developed for functional safety applications
- Wide input voltage range of 0V to 1500V
- Built-in self-test
- Output latching



TPS371KEVM

1 Evaluation Module Overview

1.1 Introduction

The TPS371KEVM is an evaluation module (EVM) for the TPS371K-Q1 voltage supervisor. This family is an automotive-grade device with support for undervoltage and overvoltage supervisor and Built-In Self-Test functionality. The TPS371KEVM offers connections to all input and output pins. Test points are provided to give the user access to an extra connection if needed for oscilloscope or multimeter measurements.

This user's guide describes the characteristics, operation, and use of the TPS371KEVM. Included in this user's guide are setup and operating instructions, printed-circuit board (PCB) layout, schematic diagram, and bill of materials (BOM). Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the TPS371KEVM.

1.2 Kit Contents

The TPS371KEVM circuit board comes pre-installed with a PTPS371KVM5DFXRQ1 900V OV only device for functionality testing of the TPS371K-Q1 family of devices. The TPS371KEVM circuit board comes packaged in a moisture barrier bag.

Table 1-1. Kit Contents

Item	Quantity
TPS371KEVM	1

1.3 Specification

		MIN	MAX	UNIT
Voltage	V_{SENSE}	0	1500	V
Voltage	V_{DD}, $V_{OUT\ OV}$, $V_{OUT\ UV}$, V_{ADJOV}, V_{ADJUV}, V_{CTS}, V_{CTR}, V_{BIST}, V_{BIST_EN}	0	5.5	V
Voltage	V_{TAP1}	0	5.5	V
Current	I_{BIST}	0	±5	mA
Current	$I_{OUT\ OV}$, $I_{OUT\ UV}$	0	10	mA
Temperature	Operating junction temperature, T_J	–40	150	°C

1.4 Device Information

The TPS371KEVM circuit board comes pre-installed with a PTPS371KVM5DFXRQ1 900V OV only device for functionality testing of the TPS371K-Q1 family of devices. The TPS371K-Q1 family has built-in self-test functionality and supports voltages up to 1500V. The device also includes an optional output latching feature.

1.5 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within the recommended electrical rated voltage and power limits. Always use electrical safety precautions to help verify your personal safety and those working around you. Contact TI's Product Information Center http://ti.com/customer support for further information.

Save all warnings and instructions for future reference.

> **WARNING**
>
> Failure to follow warnings and instructions can result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. This is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitably qualified, you must immediately stop from further use of the HV EVM.

1. Work Area Safety:
   a. Keep work area clean and orderly.
   b. Qualified observers must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and the interface electronics are energized, indicating operation of accessible high voltages can be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non-conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety:
   a. As a precautionary measure, a good engineering practice is to assume that the entire EVM can have fully accessible and active high voltages.
   b. De-energize the TI HV EVM and all the inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   c. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   d. Once EVM readiness is complete, energize the EVM as intended.

   > **WARNING**
   >
   > While the EVM is energized, never touch the EVM or the electrical circuits, as the EVM or the electrical circuits can be at high voltages capable of causing electrical shock hazard.
3. Personal Safety
   a. Wear personal protective equipment e.g. latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit. Do not leave EVM powered when unattended.

2 Hardware

2.1 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM.

2.1.1 EVM Jumpers

Table 2-1 lists the default jumper connections and functional description for the device configuration.

Table 2-1. Pinout and Onboard Jumpers

PIN NUMBER or PIN NAME	JUMPER CONNECTION	DEFAULT CONNECTION	DESCRIPTION
Pin 10, CTR	J1	Open	Jumper J1 configures the CTR pin. Connect a shunt jumper to: pins 1 and 2 to connect to C8, pins 3 and 4 to connect to C7, pins 5 and 6 to connect to C6, pins 7 and 8 to connect to C5. Refer to **TPS371K-Q1 data sheet** for capacitor values and sense delay timings.
Pin 11, CTS	J2	Open	Jumper J2 configures the CTS pin. Connect a shunt jumper to: pins 1 and 2 to connect to C4, pins 3 and 4 to connect to C3, pins 5 and 6 to connect to C2, pins 7 and 8 to connect to C1. Refer to **TPS371K-Q1 data sheet** for capacitor values and sense delay timings.
Pin 14, OUT OV	J3	Open	Jumper J3 configures the OUT OV pin. Connect a shunt jumper to pins 1 and 2 to connect to VDD or pins 2 and 3 to connect to TP6.
N/A	J4	Open	Leave jumper J4 open.

2.1.2 EVM Test Points

Table 2-2 lists the test point connections and functional description for the device configuration. Test points are placed throughout the board to verify pin functionality.

Table 2-2. Test Points

PIN NUMBER / NAME	Test Point	Description
Pin 1 / SENSE	TP1	Test point TP1 connects to SENSE.
Pin 3 /Pin 5 / Pin 6 / Pin 9 / GND	TP2	Test point TP2 connects to GND.
Pin 4 / TAP1	TP3	Test point TP3 connects to TAP1.
Pin 3 /Pin 5 / Pin 6 / Pin 9 / GND	TP4	Test point TP4 connects to GND.
Pin 15 / VDD	TP5	Test point TP5 connects to VDD.
Pin 14 / OUT OV	TP6	Test point TP6 connects to J3 pin 3. If a shunt jumper is connected to pins 2 & 3 of J3, then TP6 connects to OUT OV pullup (Used to set OUT OV pull-up voltage).
Pin 7 / OUT UV	TP7	Test point TP7 connects to OUT UV pullup (Used to set OUT UV pull-up voltage).
Pin 3 /Pin 5 / Pin 6 / Pin 9 / GND	TP8	Test point TP8 connects to GND.
N/A	TP9	Test point TP9 is not to be connected.

2.2 EVM Setup and Operation

This section describes the functionality and operation of the TPS371KEVM. This EVM comes with the a custom TPS371K-Q1 device installed.

2.2.1 Input Supply Voltage (V_{DD})

The input supply voltage (V_{DD}) is connected through TP5 on the board. The input supply voltage range is 2.7V to 5.5V.

2.2.2 SENSE

The SENSE is connected through TP1 on the board. The sense voltage range is 0V to 1500V.

2.2.3 TAP1

The TAP1 pin is the high voltage resistor divided input that goes into the OV and UV comparators. The TAP1 is connected through TP3 on the board and can be externally connected to a buffer and ADC.

2.2.4 OUT OV

The OUT OV is connected through J3 pin 2 on the board. The OUT OV output on the device asserts on SENSE going outside the supervisor overvoltage threshold. The device on the TPS371KEVM is a 900V OV only TPS371K-Q1 device, these devices have an active-low open-drain output topology on OUT OV.

2.2.5 OUT UV

The OUT UV is connected through TP7 on the board. The OUT UV output on the device asserts on SENSE going outside the supervisor undervoltage threshold. The device on the TPS371KEVM is a 900V OV only TPS371K-Q1 device, this device does not have OUT UV. The TPS371K-Q1 has an active-low open-drain output topology on OUT UV.

2.2.6 Reset Time Delay (CTR)

The TPS371K-Q1 family of devices contain an adjustable reset time delay pin that controls the time with which the OUT OV and OUT UV pins de-assert after reaching the valid condition. The user can adjust the configuration of this pin via the jumper located at J1. Refer to Section 2.1.1 for jumper connections.

2.2.7 Sense Time Delay (CTS)

The TPS371K-Q1 family of devices contain an adjustable sense time delay pin that controls the time with which the OUT OV and OUT UV pins assert after reaching the invalid condition. The user can adjust the configuration of this pin via the jumper located at J2. Refer to Section 2.1.1 for jumper connections.

3 Implementation Results

3.1 EVM Performance Results

The following measurements are taken using the default TPS371KEVM with a custom TPS371K-Q1 device.

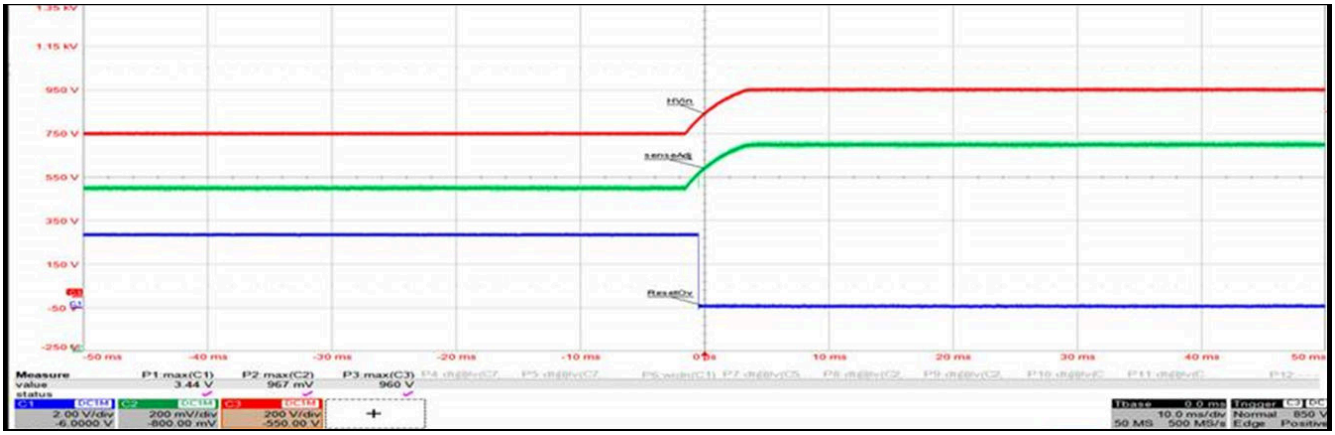


Figure 3-1. OUT OV Assertion waveform

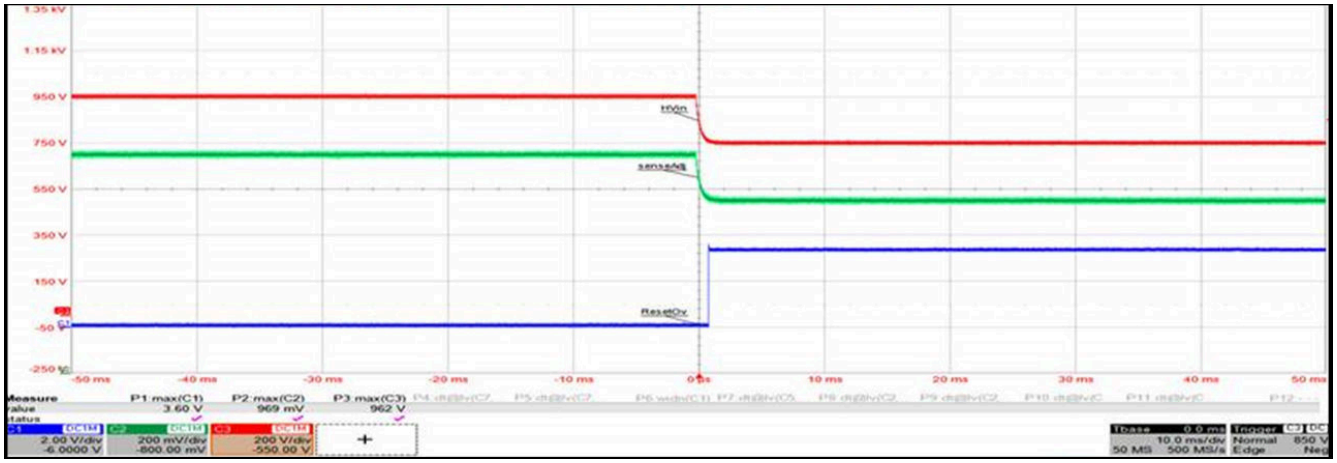


Figure 3-2. OUT OV Deassertion waveform

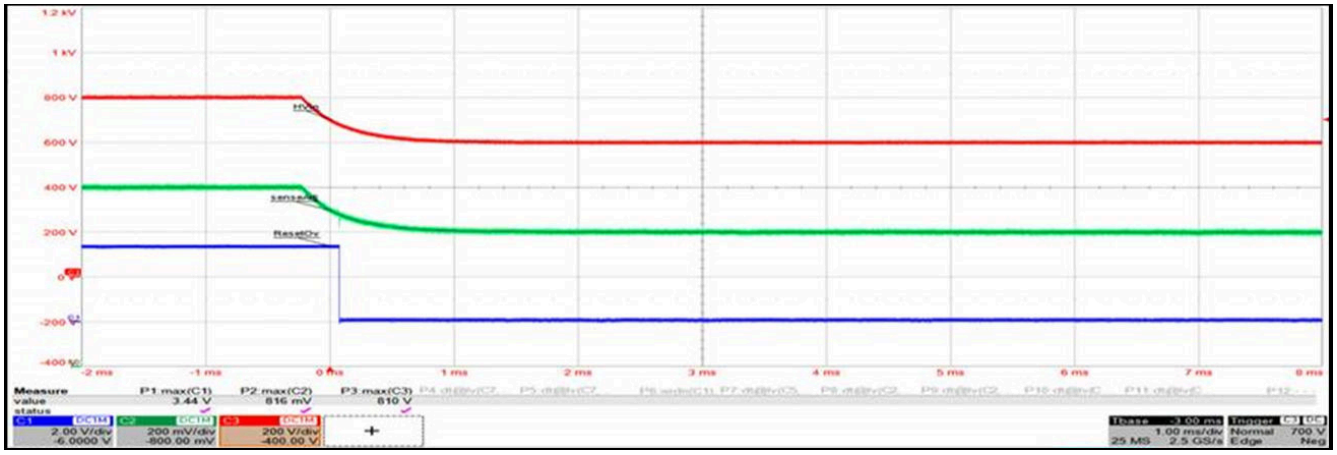


Figure 3-3. OUT UV Assertion waveform

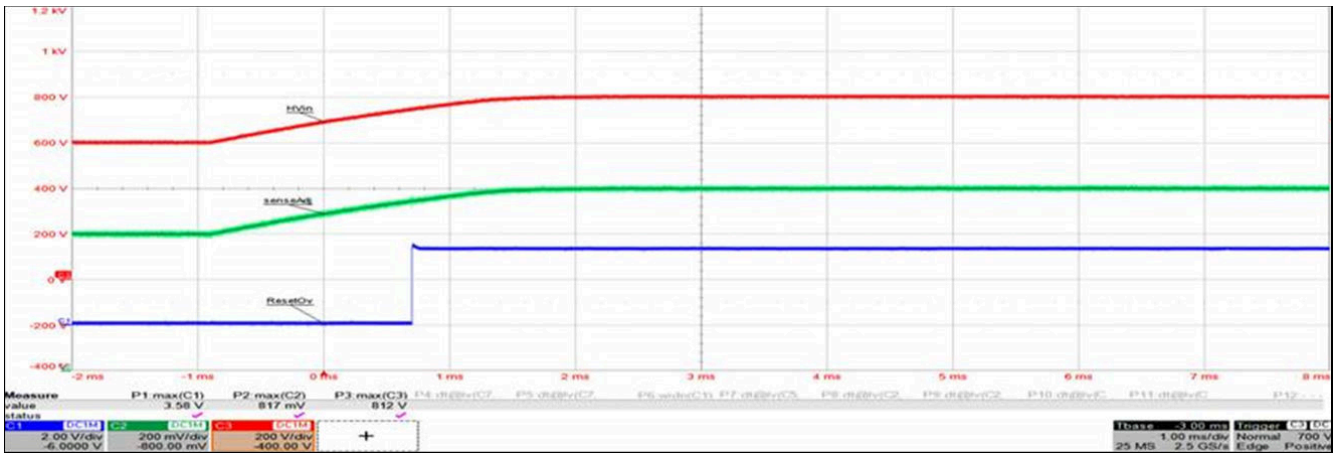


Figure 3-4. OUT UV Deassertion waveform

4 Hardware Design Files

4.1 Schematics

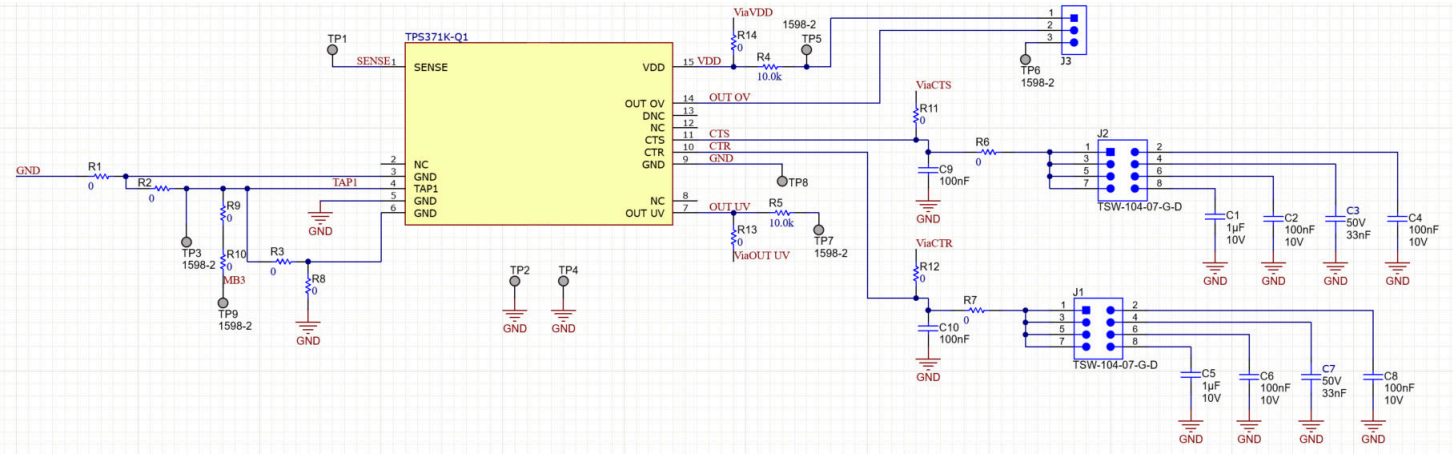


Figure 4-1. TPS371KEVM Schematic

4.2 PCB Layout

Figure 4-2 and Figure 4-3 show the top and bottom assemblies of the printed circuit board (PCB) to display the component placement of the EVM.

Figure 4-4 and Figure 4-5 show the top and bottom layouts, Figure 4-6 and Figure 4-7 show the top and bottom layers, and Figure 4-8 shows the top solder mask of the EVM.

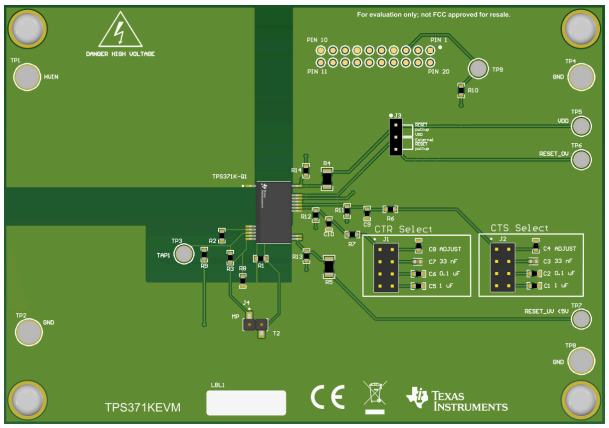


Figure 4-2. Component Placement - Top Assembly

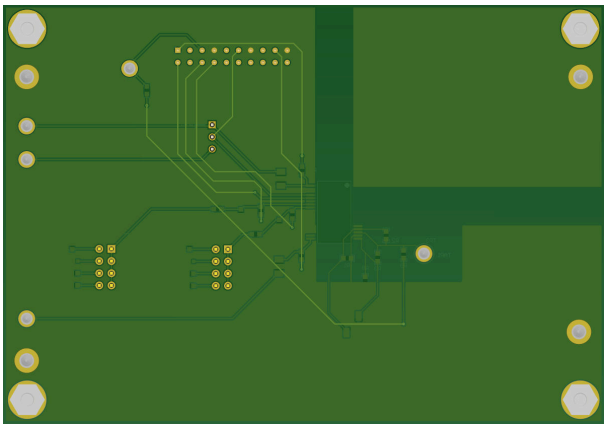


Figure 4-3. Component Placement - Bottom Assembly

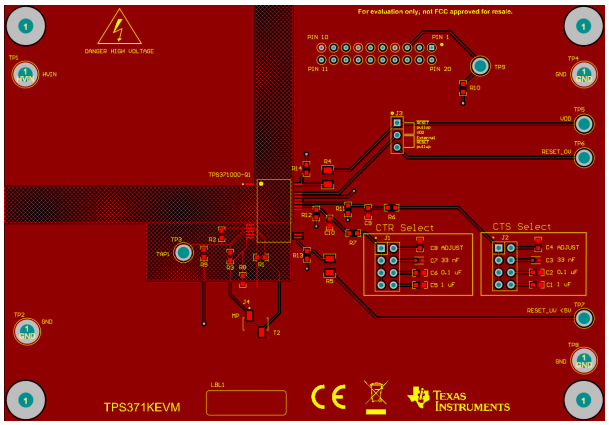


Figure 4-4. Layout - Top

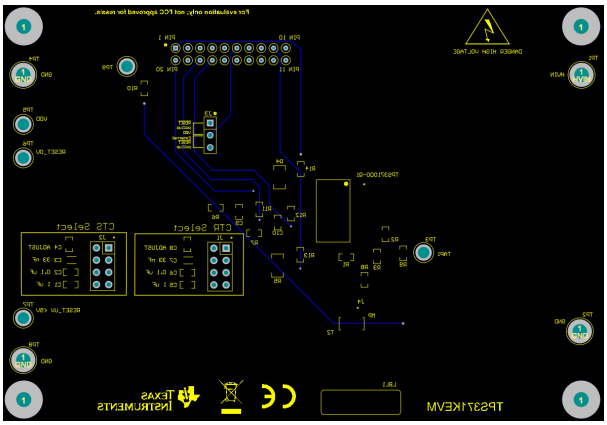


Figure 4-5. Layout - Bottom

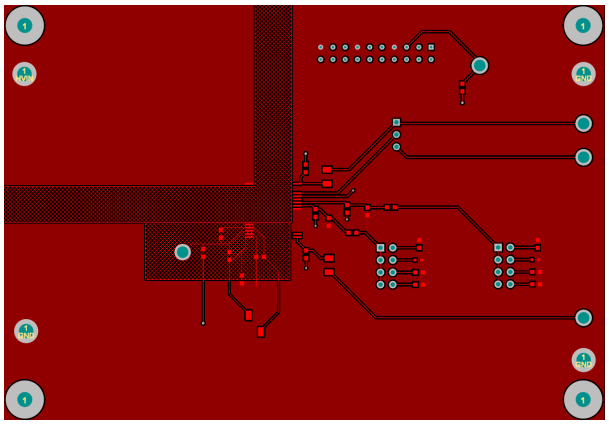


Figure 4-6. Top Layer

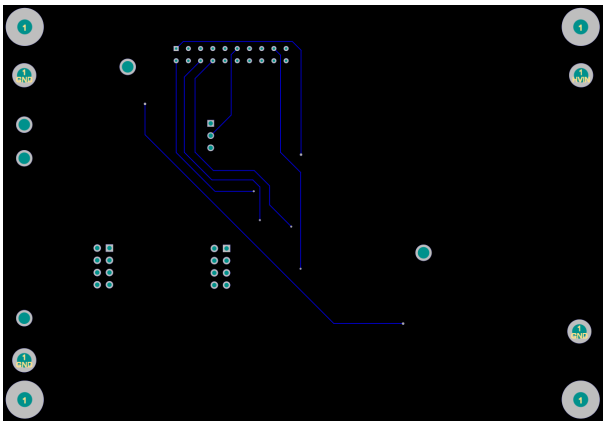


Figure 4-7. Bottom Layer

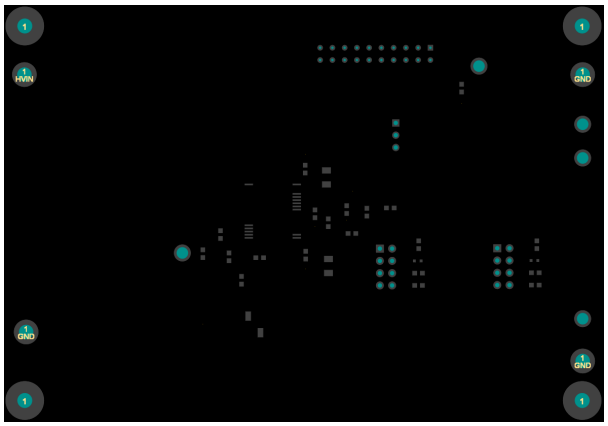


Figure 4-8. Top Solder Mask

4.3 Bill of Materials

Table 4-1. TPS371KEVM Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB	1		Printed Circuit Board		LP140	Any
C1, C5	2	1uF	CAP, CERM, 1uF, 10V, +/- 10%, X7R, 0603	0603	LMK107B7105KA-T	Taiyo Yuden
C2, C4, C6, C8, C9, C10	6	0.1uF	CAP, CERM, 0.1uF, 10V, +/- 10%, X7R, 0603	0603	C0603C104K8RACTU	KEMET
C3, C7	2	0.1uF	CAP, CERM, 33nF, 50V +/- 10%, X7R, 0603	0603	CGA3E2X7R1H333K080AA	TDK Corporation
H1, H2, H3, H4	4	33nF	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone Electronics
J1, J2	2		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec Inc.
J3	1		Header, 100mil, 3x1, Tin, TH	3x1 Header	PEC03SAAN	Sullins Connector Solutions
J4	1		Connector Header Surface Mount 2 position 0.100" (2.54mm)	4x2 Header	54201-G0802ALF	Amphenol ICC (FCI)
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady Corporation
MB2, MB3, MB4, MB5, MB6, MB7, MB8, MB9, MB12, MB13, MB14, MB15, MB16, MB17, MB18, MB19, PIN 1, PIN 10, PIN 11, PIN 20	20		PCB Pin, 0.51 Dia, Gold, TH	1x1 Header	3128-2-00-15-00-00-08-0	Mill-Max Manufacturing Corp.
R1, R2, R3, R6, R7, R8, R9, R10, R11, R12, R13, R14	12		RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	YAGEO
R4, R5	2	10k	RES, 10.0 k, 1%, 0.25 W, 1206	1206	RC1206FR-0710KL	YAGEO
TP1	1	0	Terminal, Turret, TH, Double	Keystone1503-2	1503-2	Keystone Electronics
TP2, TP4, TP8	3	1x2	Terminal, Turret, TH, Double	Keystone1503-2	1503-2	Keystone Electronics
TP3, TP5, TP6, TP7, TP9	5		Terminal, Turret, TH, Triple	Keystone1598-2	1598-2	Keystone Electronics
TPS371K-Q1	1		Wide VIN 1500V Overvoltage and Undervoltage (OV and UV) Detector with Built-in Self-test for Automotive	DFX0015A	TPS371K-Q1	Texas Instruments

5 Additional Information

5.1 Trademarks

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