EVM User's Guide: LM5125EVM-BST

LM5125EVM-BST Evaluation Module

Description

The LM5125EVM-BST evaluation module showcases the features and performance of the LM5125-Q1 wide input voltage synchronous dual-phase boost controller. This EVM is designed for ease of configuration, enabling the user to evaluate different conditions on the module. The standard configuration is designed to provide a 24V/300W output. The output voltage can be dynamically adjusted through the ATRK/DTRK pin.

Get Started

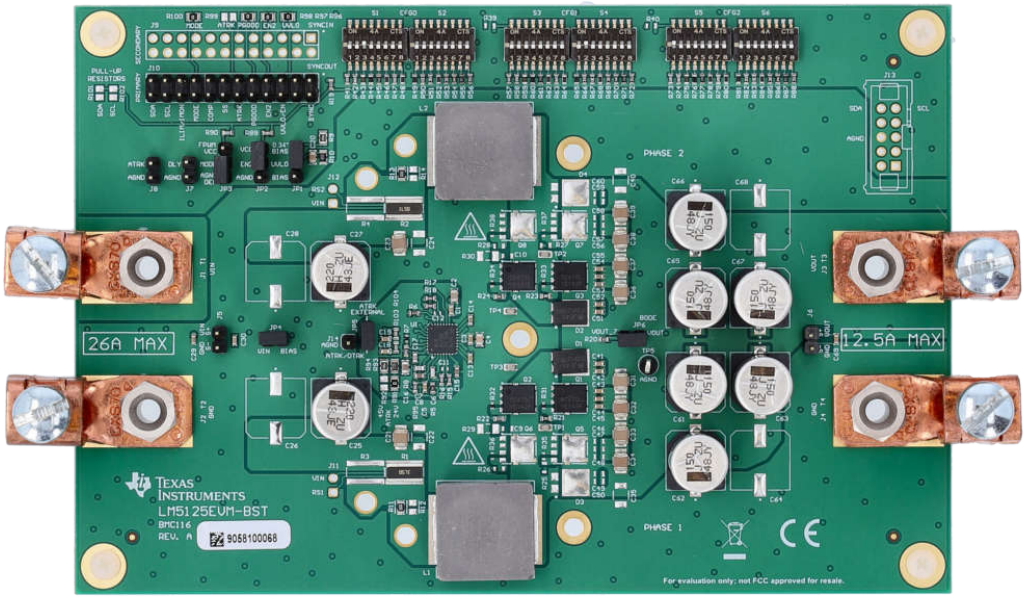
1. Make sure the jumpers and DIP switches are set properly
2. Connect EVM to power supply and load

Features

- Two phase interleaved boost converter
- 1kW peak power and 300W average power
- Output voltage tracking from analog/PWM
- Bypass mode
- Optional Dual Random Spread Spectrum (DRSS)
- Programmable undervoltage lockout (UVLO), Soft-start, and dead time
- Comprehensive fault protections
  - Peak current limit
  - Average current limit
  - Over voltage protection

Applications

- Automotive Class H audio power amplifier
- Automotive LED headlight applications



1 Evaluation Module Overview

1.1 Introduction

The LM5125EVM-BST evaluation module provides a fully functional dual phase synchronous boost converter to evaluate LM5125-Q1. The EVM operates over an input voltage range of 9V to 18V and can handle input transients up to 42V. The EVM provides an output voltage of 24V with 300W rated power and 1kW peak power. The output voltage can also be adjusted up to 45V via ATRK/DTRK pin.

1.2 Kit Contents

- One LM5125EVM-BST PCB assembly
- EVM Disclaimer Read Me

1.3 Specification

Table 1-1. EVM Specification

Parameter	Condition	MIN	TYP	MAX	UNIT
Input Voltage	Operation	9	14.4	18	V
Output Voltage	R_{ATRK} = 40.2kΩ		24		V
	R_{ATRK} = 75kΩ		45		V
Rated Output Power	V_{in} = 14.4V		300		W
Peak Output Power, 100ms	V_{in} = 14.4V		1000		W
Switching frequency			400		kHz
Efficiency	V_{in} = 14.4V, V_{out} = 24V, P_{out}=300W		97.5		%
	V_{in} = 14.4V, V_{out} = 45V, P_{out}=300W		95.7		%

1.4 Device Information

The LM5125-Q1 is a dual phase synchronous boost controller with below features:

- Wide input voltage range from 2.5V to 42V
- Programmable output voltage 6V to 60V
- Dynamic output voltage tracking
- Bypass mode
- Programmable OVP
- Cycle by cycle peak current limit
- Inductor current monitor
- Average input current limit
- Selectable dead time

2 Hardware

2.1 Connector, Jumper, DIP switch and Test point Description

The connectors, jumpers, DIP switches and test points of the EVM are introduced in this section.

2.1.1 Connector Descriptions

Table 2-1. Connectors

Connector	Pin	Description
J1/T1	VIN	Positive power input for the evaluation module
J2/T2	GND	Negative power input for the evaluation module
J3/T3	VOUT	Positive power output for the evaluation module
J4/T4	GND	Negative power output for the evaluation module
J5	1	Input voltage sensing VIN
	2	Input voltage sensing GND
J6	1	Output voltage sensing VOUT
	2	Output voltage sensing GND

2.1.2 Jumper Descriptions

Table 2-2. Jumper Descriptions

Connector	Pins	Description	Default Connection
JP1	1, 2	UVLO/EN pin connected to VIN resistor divider	Y
	2, 3	UVLO/EN pin connected to BIAS	
JP2	1, 2	Phase 2 is turned on	Y
	2, 3	Phase 2 is turned off	
JP3	1, 2	Set to FPWM	
	2, 3	Set to DEM	Y
JP4	1, 2	BIAS pin connected to VIN	Y
JP5	1, 2	RC filter from J8 connected to ATRK/DTRK pin.	Y
JP6	1, 2	Injection signal input for bode plot measurement	Y
J7	1, 2	DLY pin	
J8	1,2	Input to ATRK/DTRK pin. RC filter is inserted.	
J10	1	Pin 23 of U1	
	3	No Connection	
	5	UVLO/EN	
	7	EN2	
	9	PGOOD	
	11	ATRK/DTRK	
	13	SS	
	15	COMP	
	17	MODE	
	19	ILIM/IMON	
	21	SCL	
	23	SDA	
	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24	GND	

2.1.3 DIP Switch Descriptions

The CFG0 pin defines the dead time and the ATRK/DTRK pin 20µA current source for V_{OUT} programming.

Table 2-3. CFG0 Pin Settings

Level	Dead time (ns)	20µA ATRK current
1	14	on
2	30	
3	50	
4	75	
5	100	
6	125	
7	150	
8	200	
9	18	off
10	30	
11	50	
12	75	
13	100	
14	125	
15	150	
16	200	

The CFG1 pin setting defines the V_{OUT} Over Voltage Protection level, Clock Dithering, the 120% input current limit protection (I_{CL_latch}) operation, and the power good pin behavior.

Table 2-4. CFG1 Pin Settings

Level	OVP Bit 0	Clock Dithering Mode	I_{CL_latch}	$PGOOD_{OVP\_enable}$
1	0	enabled (DRSS)	disabled	disabled
2	1			
3	0			enabled
4	1			
5	0		enabled	disabled
6	1			
7	0			enabled
8	1			
9	0	disabled	disabled	disabled
10	1			
11	0			enabled
12	1			
13	0		enabled	disabled
14	1			
15	0			enabled
16	1			

The CFG2 pin defines the V_{OUT} Over Voltage Protection level, if the device uses the internal clock generator or an external clock applied at the SYNCIN pin. It configures as well if the device is a single device or part of a dual device configuration, the SYNCIN and SYNCOUT pin is enabled/disabled accordingly. During clock synchronization, the clock dither function is disabled.

Table 2-5. CFG2 Pin Settings

Level	OVP Bit 1	SYNCIN	Clock Dithering
1	0	off	CFG1 pin
2	1		
3	0		
4	1	on	disabled
≥5	0		

Table 2-6. Overvoltage Protection Level Selection

OVP Level	OVP Bit 1	OVP Bit 0
64V	0	0
50V	0	1
35V	1	0
28.5V	1	1

S1 through S6 are 8-bit DIP switches.

- S1 and S2 are for CFG0
  - S1-postion 1 selects Level 1, …, S1-postion 8 selects Level 8
  - S2-postion 1 selects Level 9, …, S2-postion 8 selects Level 16
- S3 and S4 are for CFG1
  - S3-postion 1 selects Level 1, …, S3-postion 8 selects Level 8
  - S4-postion 1 selects Level 9, …, S4-postion 8 selects Level 16
- S5 and S6 are for CFG2
  - S5-postion 1 selects Level 1, …, S5-postion 8 selects Level 8
  - S6-postion 1 selects Level 9, …, S6-postion 8 selects Level 16

Select position 3 for S1 by default. This selects Level 3 for CFG0:

- Dead time = 50ns
- 20µA ATRK current source = on

Select position 2 for S4 by default. This selects Level 10 for CFG1:

- OVP bit 0 = 1
- DRSS = disabled
- I_{CL_latch} = disabled
- $PGOOD_{OVP\_enable}$ = disabled

Select position 1 for S5 by default. This selects Level 1 for CFG2:

- OVP bit 1 = 0
- Single chip
- Phase shift = 180°
- SYNCIN = off
- SYNCOUT = off

OVP bit 1 = 0 and OVP bit 0 = 1 select OVP level to 50V.

Note

The EVM can be damaged if lower than 50ns dead time is selected or operate with V_{out}>50V. Select OVP level no more than 50V.

2.1.4 Test Points Description

Table 2-7. Test Points Description

Test Point	Name	Description
TP1	SW1	Test point for switch node of phase 1
TP2	SW2	Test point for switch node of phase 2
TP3	GND	Test point for GND
TP4	GND	Test point for GND
TP5	GND	Test point for GND

2.1.5 Easy to Use Features

Output Voltage Tracking

Connect analog tracking voltage signal to J8. A high frequency PWM signal is also acceptable because a two-stage RC filter is inserted.

Select V_{out} between 24V and 45V

- Populate R91=0Ω and keep R92 unpopulated to set V_{out} to 24V (default)
- Populate R92=0Ω and keep R91 unpopulated to set V_{out} to 45V

Refer to Figure 2-1.

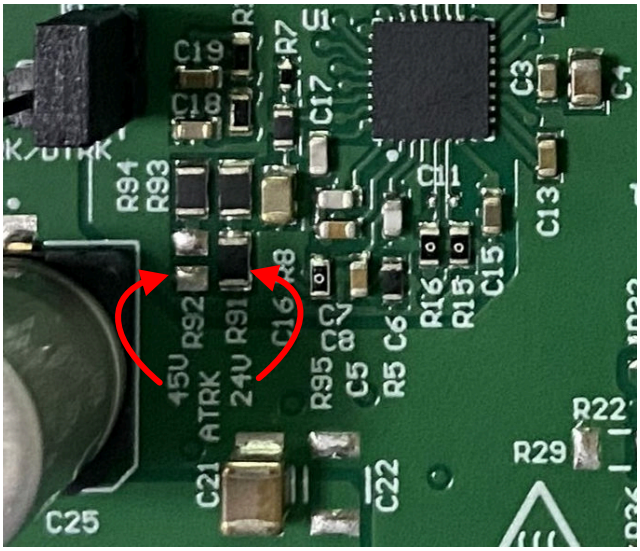


Figure 2-1. Select V_{out} between 24V and 45V

Observe the inductor current with current probe

Remove R11 and solder a wire in the plated through holes to observe the current through L1 with a current probe. Refer to Figure 2-2.

Similarly, remove R13 and solder a wire to observe the current through L2.

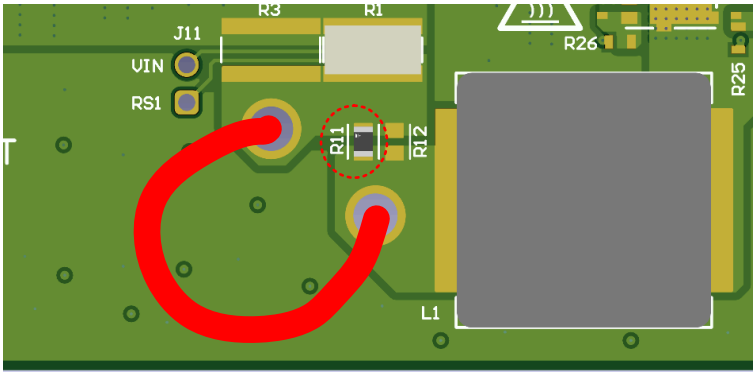


Figure 2-2. Observe L1 inductor current

3 Implementation Results

3.1 Test Setup and Procedure

3.1.1 Test Setup

Figure 3-1 shows the required test setup to evaluate the EVM.

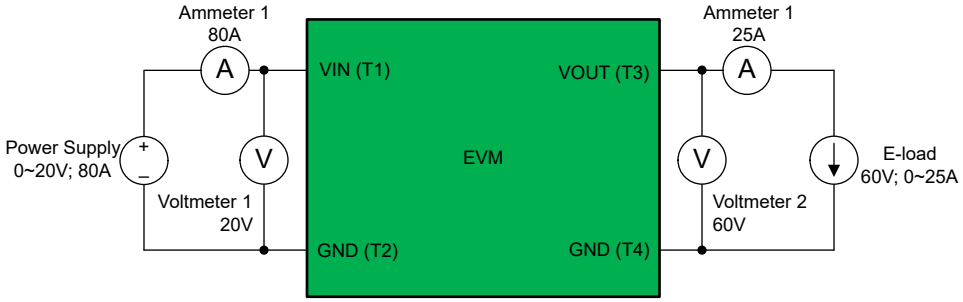


Figure 3-1. EVM Test Setup

The following test equipment is needed:

- Power supply: The power supply needs to support 20V/80A
- Electronic Load: The electronic load need to sink 1000W at 60V
- Multimeters (optional)
  - Voltmeter 1 (V_{IN}): Capable of measuring input voltage of 20V
  - Voltmeter 2 (V_{OUT}): Capable of measuring output voltage of 60V
  - Ammeter 1 (I_{IN}): Capable of 80A DC measurement
  - Ammeter 2 (I_{OUT}): Capable of 25A DC measurement
- Oscilloscope: Minimum 200MHz bandwidth

3.1.2 Test Procedure

1. Make sure the jumpers and DIP switches are set properly. Refer to Section 2.1.2 and Section 2.1.3.
2. Prepare the setup following Figure 3-1.
3. Set the power supply voltage to 14.4V and the electronic load to 0.1A. After the power supply is turned on, the electronic load voltage will be regulated to 24V by default.
4. The load and input voltage may be changed as required.

3.1.3 Precautions

	Caution	Caution Hot surface. Contact can cause burns. Do not touch!

3.2 Performance Data and Results

3.2.1 Efficiency

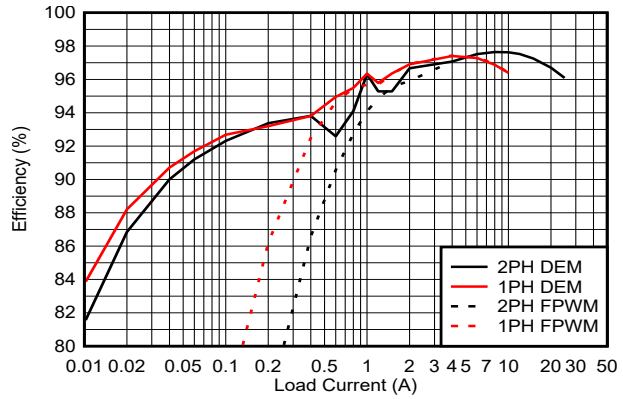


Figure 3-2. Efficiency vs Output Current, V_{in} = 14.4V, V_{out} = 24V

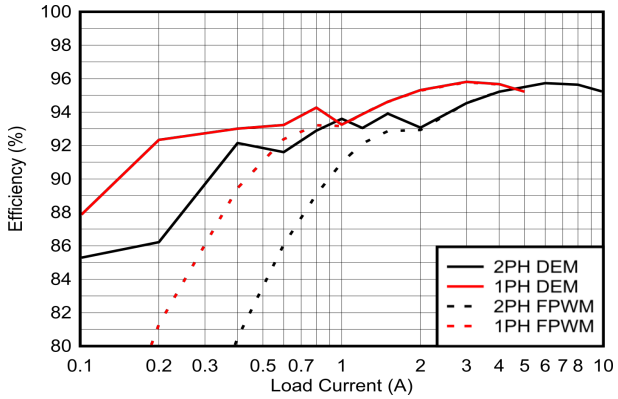


Figure 3-3. Efficiency vs Output Current, V_{in} = 14.4V, V_{out} = 45V

3.2.2 Steady State Waveforms

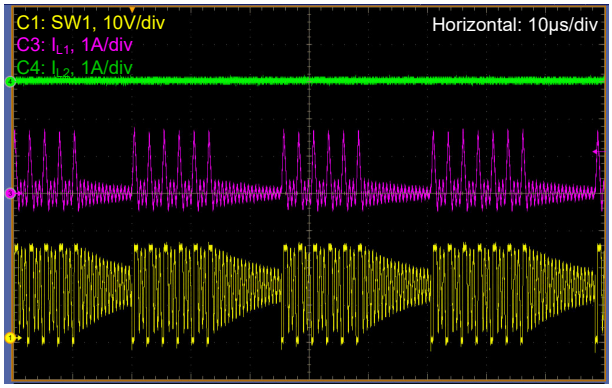


Figure 3-4. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load}= 0.1A

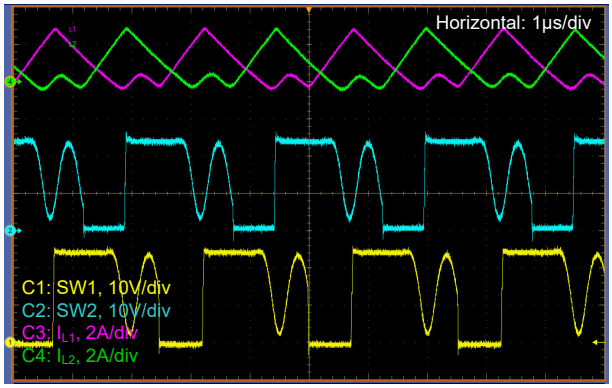


Figure 3-5. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load}= 1A

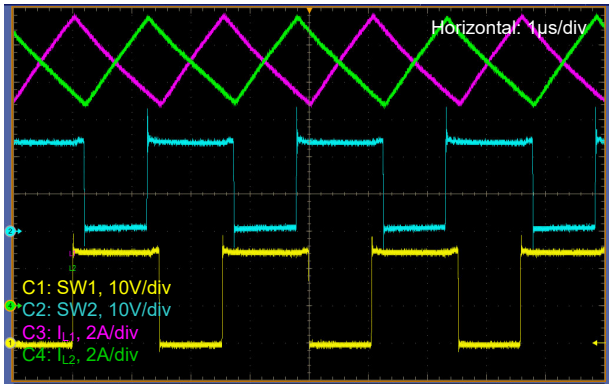


Figure 3-6. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load}= 15A

3.2.3 Step Load Response

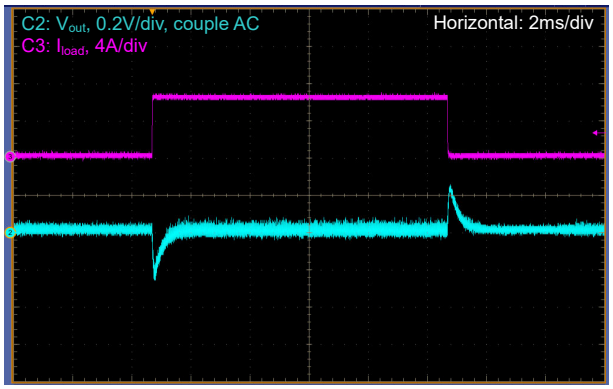


Figure 3-7. Load Transient, V_{in} = 14.4V, V_{out} = 24V, FPWM, I_{load} = 0A to 6.25A at 1A/µs

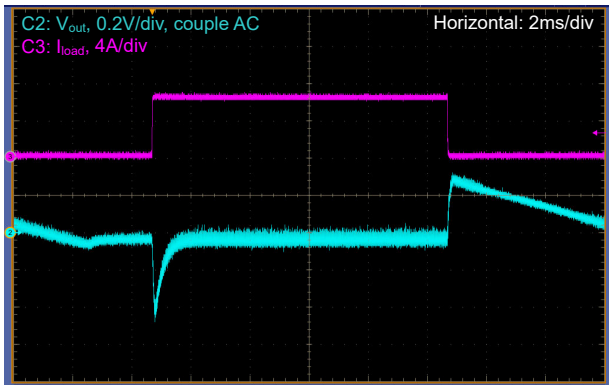


Figure 3-8. Load Transient, V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load} = 0A to 6.25A at 1A/µs

3.2.4 AC Loop Response Curve

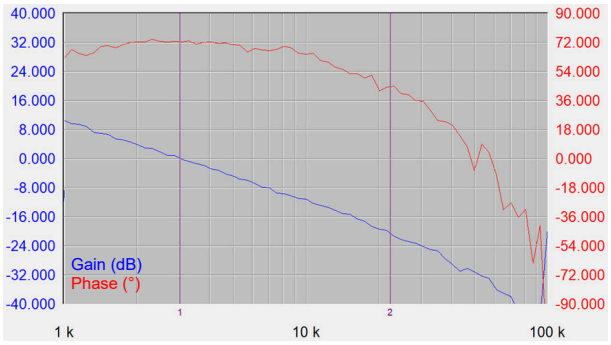


Figure 3-9. Bode Plot, Vin=14.4V, Vout=40V, Iout=10A (Average Current Loop Disabled)

3.2.5 Thermal Performance

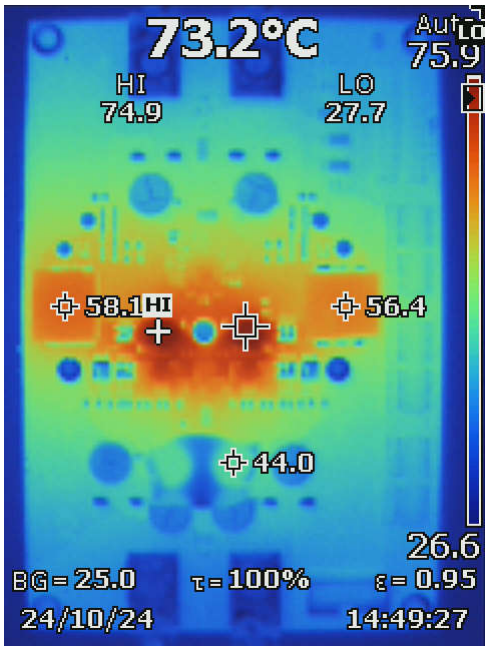


Figure 3-10. V_{in} = 14.4V, V_{out} = 24V, P_{OUT} = 300W, Natural Convection

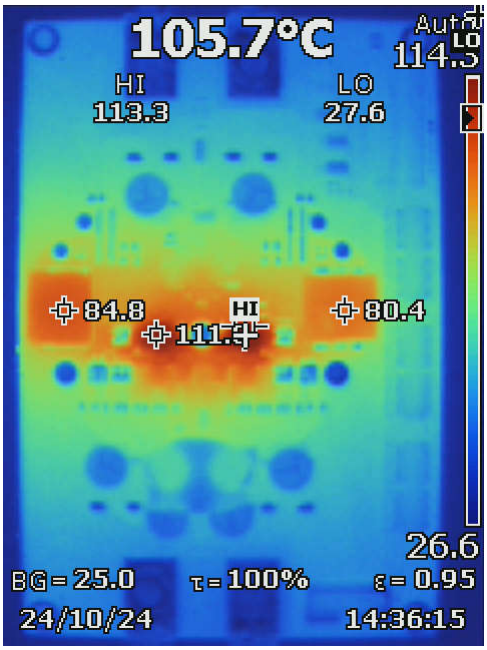


Figure 3-11. V_{in} = 14.4V, V_{out} = 45V, P_{OUT} = 300W, Natural Convection

4 Hardware Design Files

4.1 Schematic

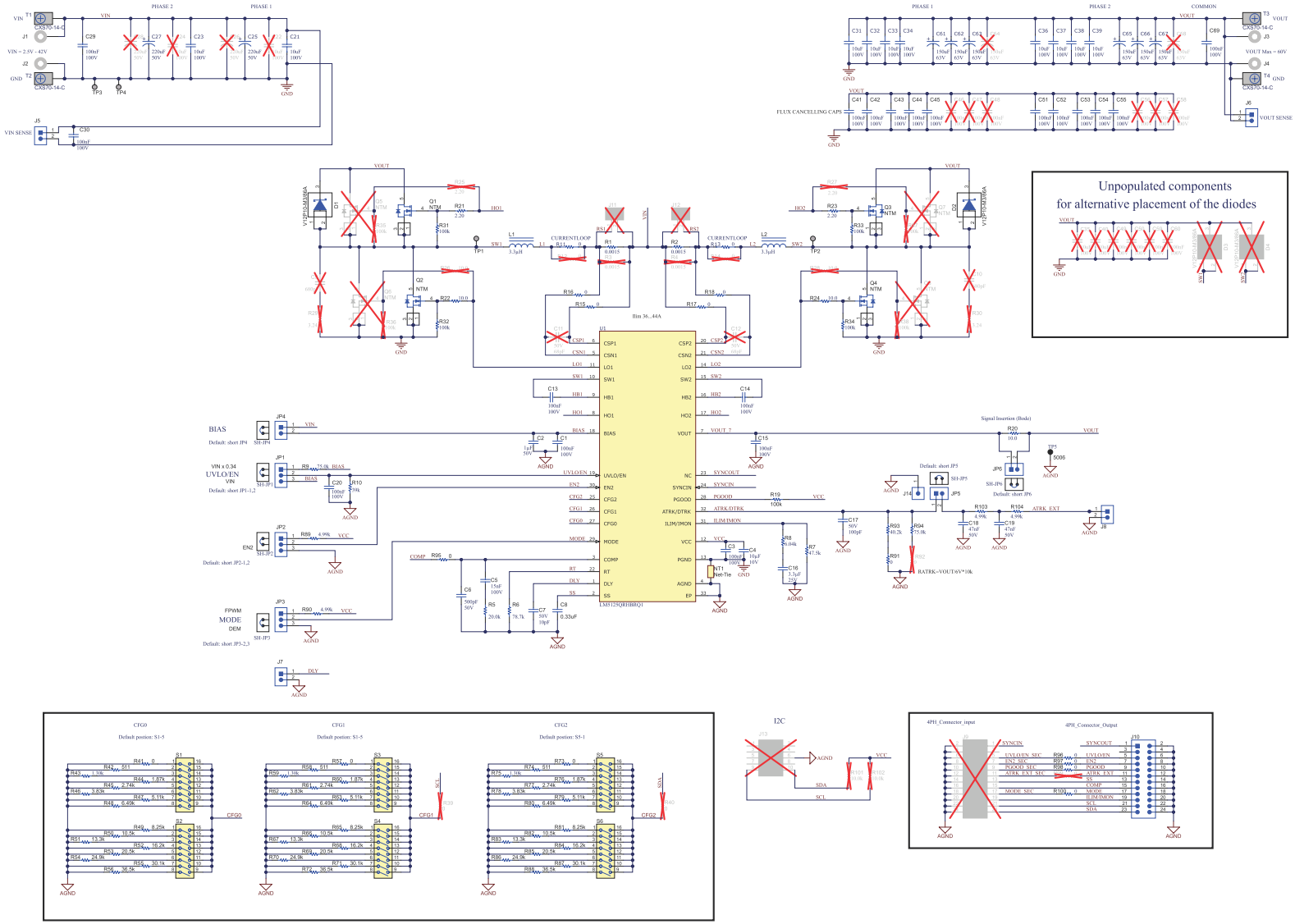


Figure 4-1. Schematic

4.2 PCB Layers

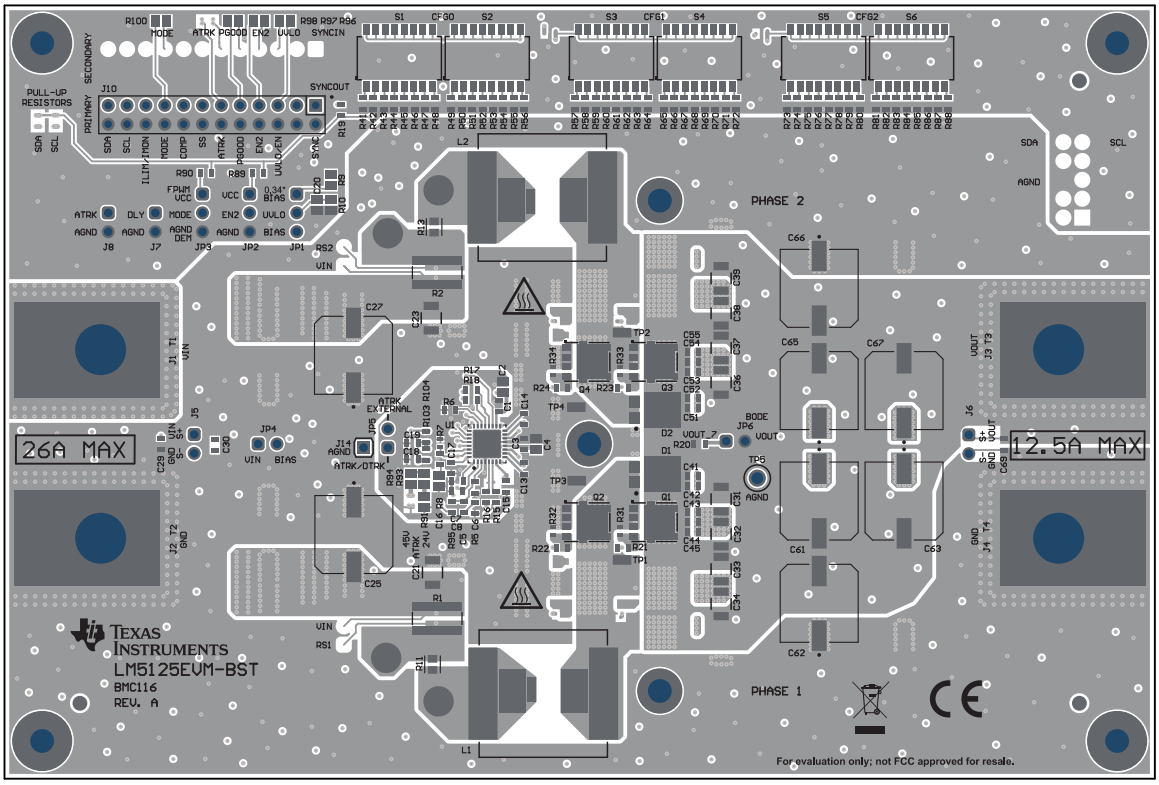


Figure 4-2. Top Silk Screen

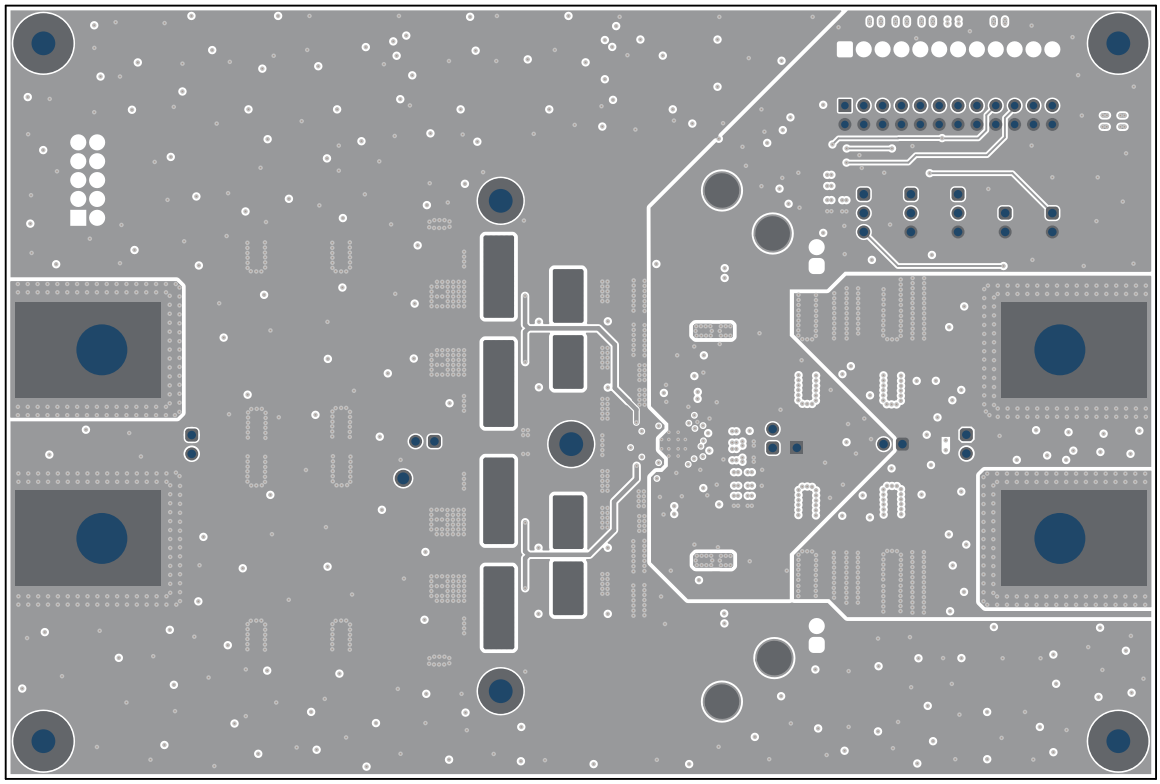


Figure 4-3. Bottom Silk Screen

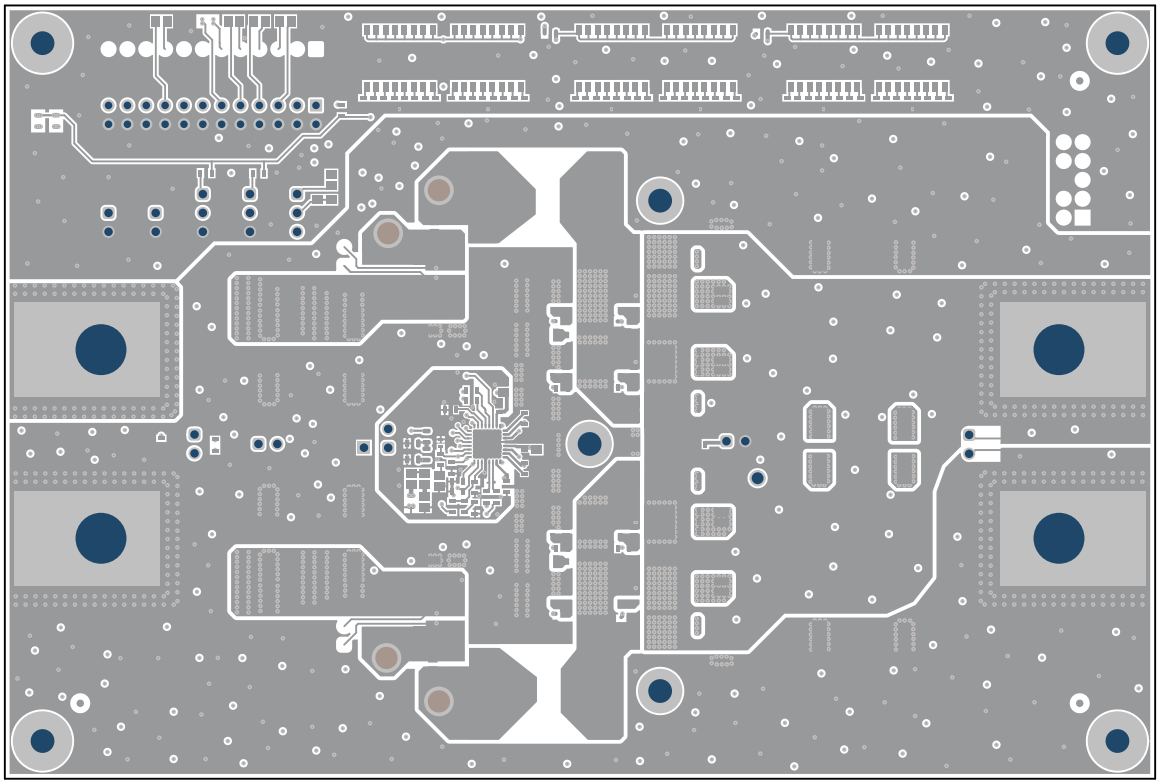


Figure 4-4. Top Layer

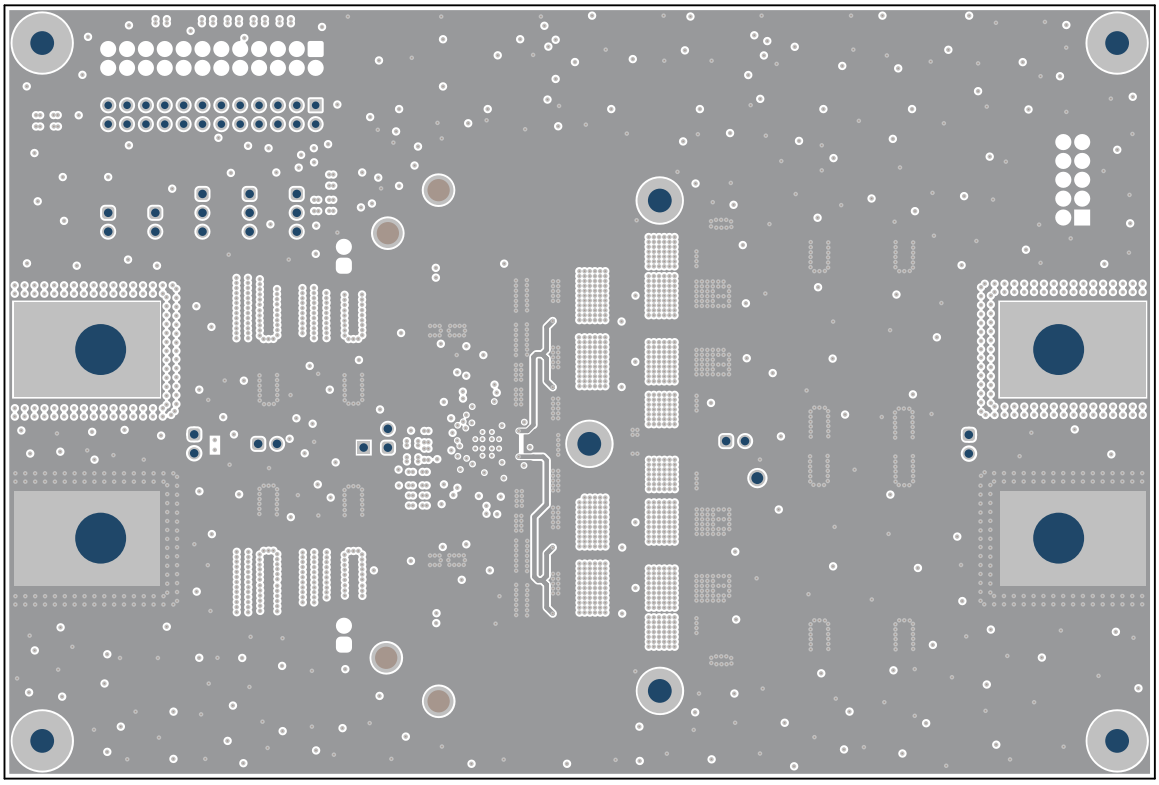


Figure 4-5. Signal Layer 1

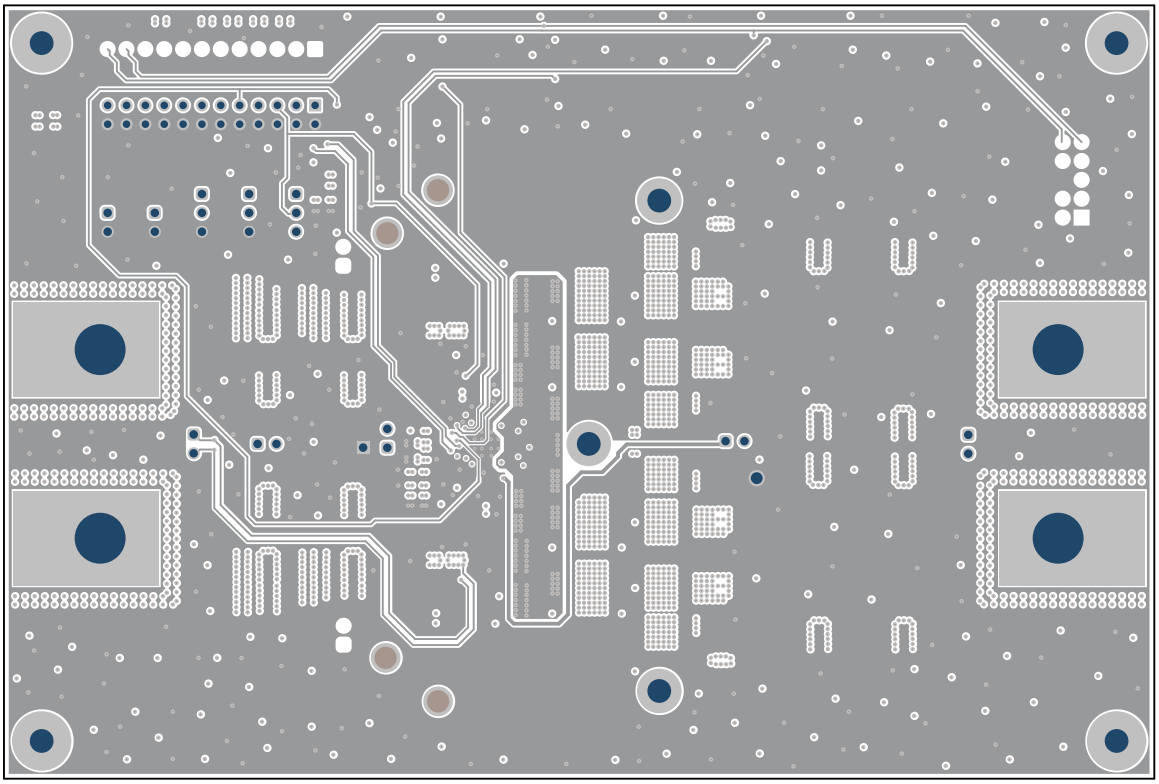


Figure 4-6. Signal Layer 2

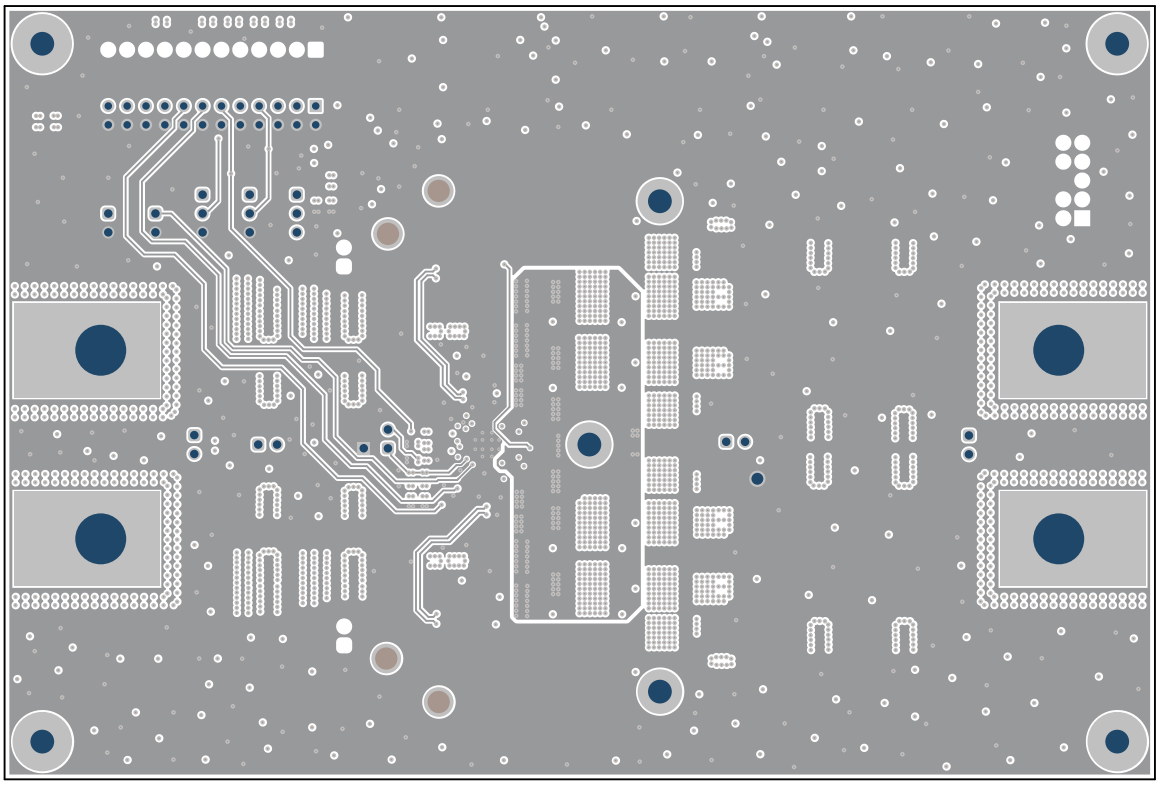


Figure 4-7. Signal Layer 3

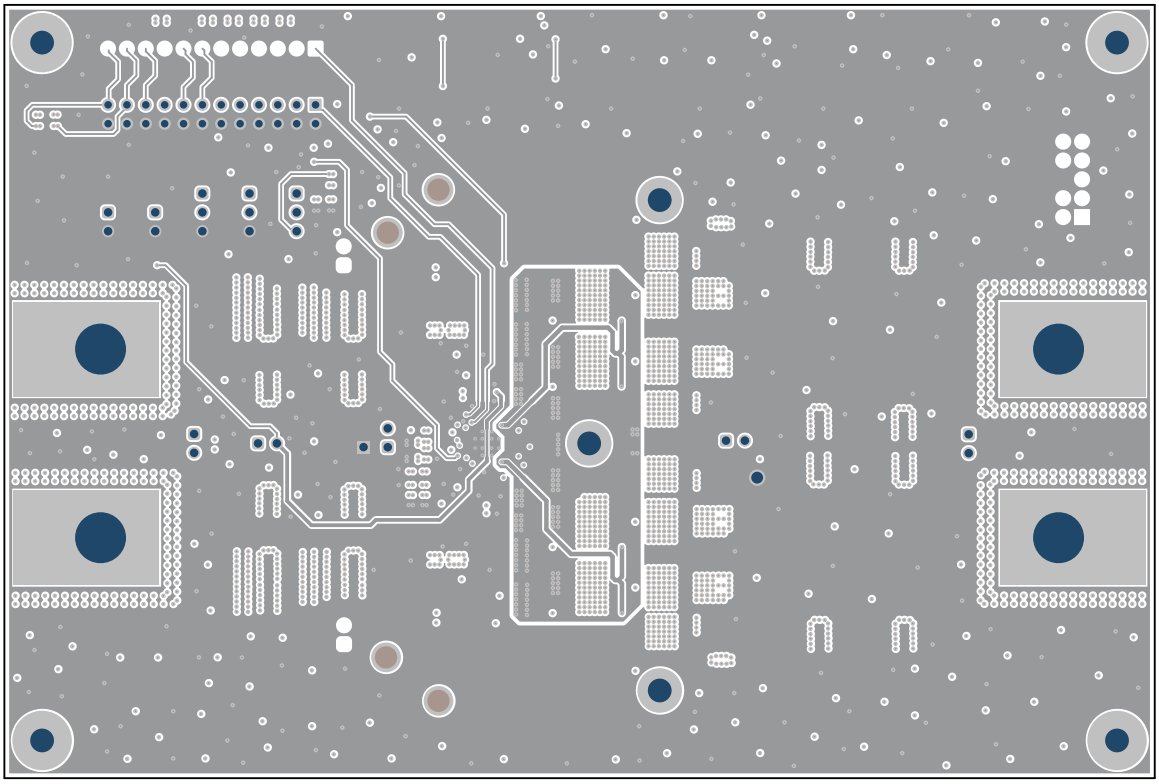


Figure 4-8. Signal Layer 4

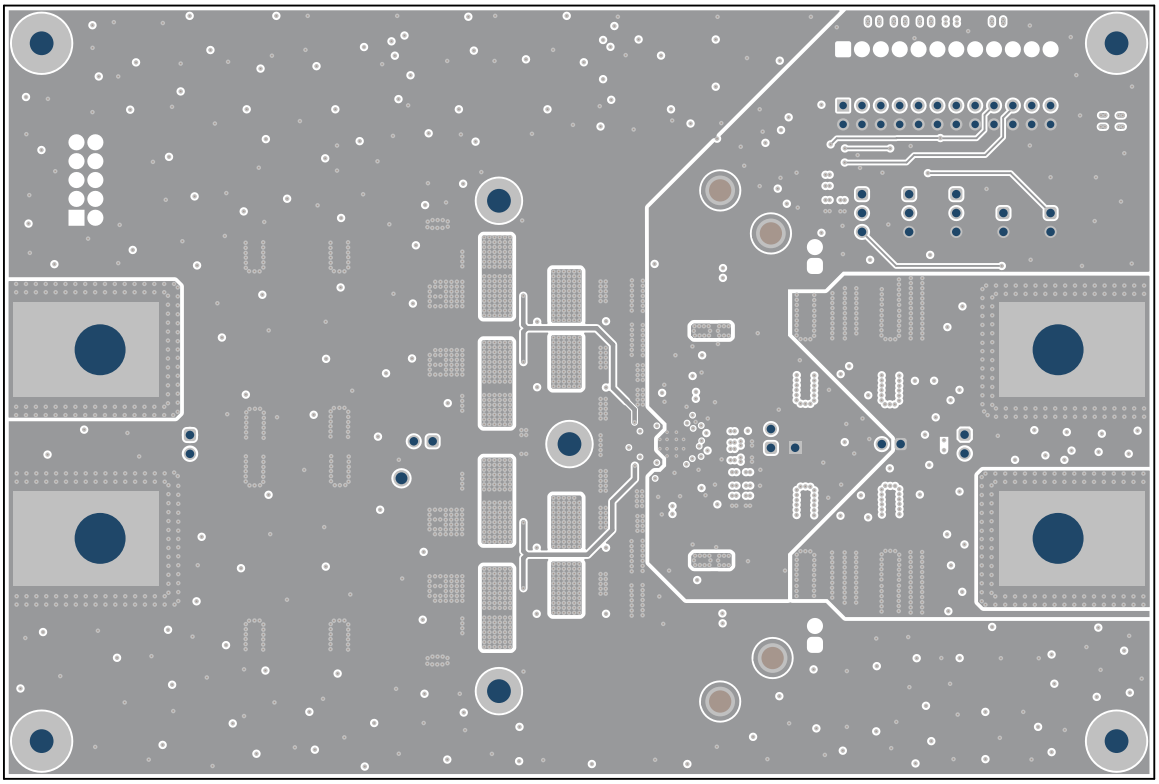


Figure 4-9. Bottom Layer

4.3 Bill of Materials

Table 4-1. Bill of Materials

Designator	Quantity	Description	Part Number	Manufacturer
C1, C3, C13, C14, C15, C29, C30, C41, C42, C43, C44, C45, C51, C52, C53, C54, C55, C69	18	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, 0603	GRM188R72A104KA35D	MuRata
C2	1	CAP, CERM, 1 µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805	GCM21BR71H105KA03K	MuRata
C4	1	CAP, CERM, 10 µF, 10 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805	GCJ21BR71A106KE01L	MuRata
C5	1	CAP, CERM, 0.015 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	GCM188R72A153KA37D	MuRata
C6	1	CAP, CERM, 500 pF, 50 V, +/- 5%, C0G/NP0, 0603	CC0603JRNPO9BN501	Yageo America
C7	1	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0603	C1608C0G1H100D080AA	TDK
C8	1	CAP, CERM, 0.33 uF, 10 V, +/- 10%, X5R, 0603	C0603C334K8PACTU	Kemet
C16	1	CAP, CERM, 3.3 uF, 25 V, +/- 10%, X7R, 0805	C2012X7R1E335K125AB	TDK
C17	1	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	C1608C0G1H101J080AE	TDK
C18, C19	2	CAP, CERM, 0.047 uF, 50 V, +/- 10%, X7R, 0603	C1608X7R1H473K080AA	TDK
C20	1	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	CGA4J2X7R2A104K125AA	TDK
C21, C23, C31, C32, C33, C34, C36, C37, C38, C39	10	10µF ±10% 100V Ceramic Capacitor X7S 1210 (3225 Metric)	GRM32EC72A106KE05L	Murata
C25, C27	2	Aluminum Hybrid Polymer Capacitors 220uF 20% 50V Life 4000Hours AEC-Q200 RADIAL SMT	EEHZU1H221P	Panasonic
C61, C62, C63, C65, C66, C67	6	Aluminum Hybrid Polymer Capacitors 150uF 20% 63V Life 4000Hours AEC-Q200 RADIAL SMT	EEHZU1J151P	Panasonic
D1, D2	2	Diode, Schottky, 100 V, 12 A, AEC-Q101, TO-277A	V12P10-M3/86A	Vishay-Semiconductor
FID1, FID2, FID3	3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
H1, H2, H3, H4	4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone
J1, J2, J3, J4	4	Standard Banana Jack, Uninsulated, 15A	108-0740-001	Cinch Connectivity
J5, J6, J7, J8, JP4, JP5, JP6	7	Header, 2.54 mm, 2x1, Gold, TH	61300211121	Wurth Elektronik
J10	1	Header, 100mil, 12x2, Gold, TH	TSW-112-07-G-D	Samtec
J14	1	Header, 2.54 mm, 1x1, Gold, TH	61300111121	Wurth Elektronik
JP1, JP2, JP3	3	Header, 2.54 mm, 3x1, Gold, TH	61300311121	Wurth Elektronik
L1, L2	2	Inductor, Shielded, 3.3 µH, 32.2 A, 0.00327 ohm, AEC-Q200 Grade 0, SMD	IHLP6767GZER3R3M5A	Vishay-Dale
Q1, Q2, Q3, Q4	4	MOSFET, N-CH, 60 V, 71 A, SO-8FL	NTMFS5C670NLT1G	ON Semiconductor
R1, R2	2	RES, 0.0015, 5%, 2 W, 2512 WIDE	PML100HZPJV1L5	Rohm
R5	1	RES, 20.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060320K0FKEA	Vishay-Dale
R6	1	RES, 78.7 k, 0.1%, 0.1 W, 0603	RT0603BRD0778K7L	Yageo America

Table 4-1. Bill of Materials (continued)

Designator	Quantity	Description	Part Number	Manufacturer
R7	1	RES, 47.5 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040247K5FKED	Vishay-Dale
R8	1	RES, 6.04 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06036K04FKEA	Vishay-Dale
R9, R94	2	RES, 75.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW080575K0FKEA	Vishay-Dale
R10	1	RES, 39 k, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW080539K0JNEA	Vishay-Dale
R11, R13	2	0 Ohms Jumper Chip Resistor 0805 (2012 Metric) Metal Element	WSL080500000ZEA9	Vishay
R15, R16, R17, R18, R41, R57, R73	7	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R19	1	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100KFKEA	Vishay-Dale
R20, R22, R24	3	RES, 10.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310R0FKEA	Vishay-Dale
R21, R23	2	RES, 2.20, 1%, 0.1 W, 0603	ERJ-3RQF2R2V	Panasonic
R31, R32, R33, R34	4	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402100KFKED	Vishay-Dale
R42, R58, R74	3	RES, 511, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603511RFKEA	Vishay-Dale
R43, R59, R75	3	RES, 1.30 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K30FKEA	Vishay-Dale
R44, R60, R76	3	RES, 1.87 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K87FKEA	Vishay-Dale
R45, R61, R77	3	RES, 2.74 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06032K74FKEA	Vishay-Dale
R46, R62, R78	3	RES, 3.83 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06033K83FKEA	Vishay-Dale
R47, R63, R79	3	RES, 5.11 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06035K11FKEA	Vishay-Dale
R48, R64, R80	3	RES, 6.49 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06036K49FKEA	Vishay-Dale
R49, R65, R81	3	RES, 8.25 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06038K25FKEA	Vishay-Dale
R50, R66, R82	3	RES, 10.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K5FKEA	Vishay-Dale
R51, R67, R83	3	RES, 13.3 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060313K3FKEA	Vishay-Dale
R52, R68, R84	3	RES, 16.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060316K2FKEA	Vishay-Dale
R53, R69, R85	3	RES, 20.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060320K5FKEA	Vishay-Dale
R54, R70, R86	3	RES, 24.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060324K9FKEA	Vishay-Dale
R55, R71, R87	3	RES, 30.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060330K1FKEA	Vishay-Dale
R56, R72, R88	3	RES, 36.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060336K5FKEA	Vishay-Dale
R89, R90, R103, R104	4	RES, 4.99 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06034K99FKEA	Vishay-Dale
R91, R96, R97, R98, R100	5	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW08050000Z0EA	Vishay-Dale
R93	1	RES, 40.2 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW080540K2FKEA	Vishay-Dale
R95	1	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3GEY0R00V	Panasonic
S1, S2, S3, S4, S5, S6	6	Switch, SPST, 8 Pos, 25mA, 24VDC, SMD	218-8LPST	CTS Electrocomponents
SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH-JP5, SH-JP6	6	Shunt, 100mil, Flash Gold, Black	SPC02SYAN	Sullins Connector Solutions
T1, T2, T3, T4	4	Terminal 70A Lug	CXS70-14-C	Panduit

Table 4-1. Bill of Materials (continued)

Designator	Quantity	Description	Part Number	Manufacturer
TP1, TP2, TP3, TP4	4	PC Test Point, SMT	RCU-0C	TE Connectivity
TP5	1	Test Point, Compact, Black, TH	5006	Keystone Electronics
U1	1	Wide-VIN, 2.2 MHz dual-phase boost controller with VOUT tracking	LM5125QRHBRQ1	Texas Instruments

5 Additional Information

Trademarks

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2024) to Revision A (April 2025)	Page
• Updated image to reflect changes from revision E3 to revision A	1
• Updated *Efficiency* figures	9
• Updated schematic	12
• Updated PCB layers	13
• Updated bill of materials	17

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