

EVM User's Guide: TPS376X EVM

TPS376X Evaluation Module

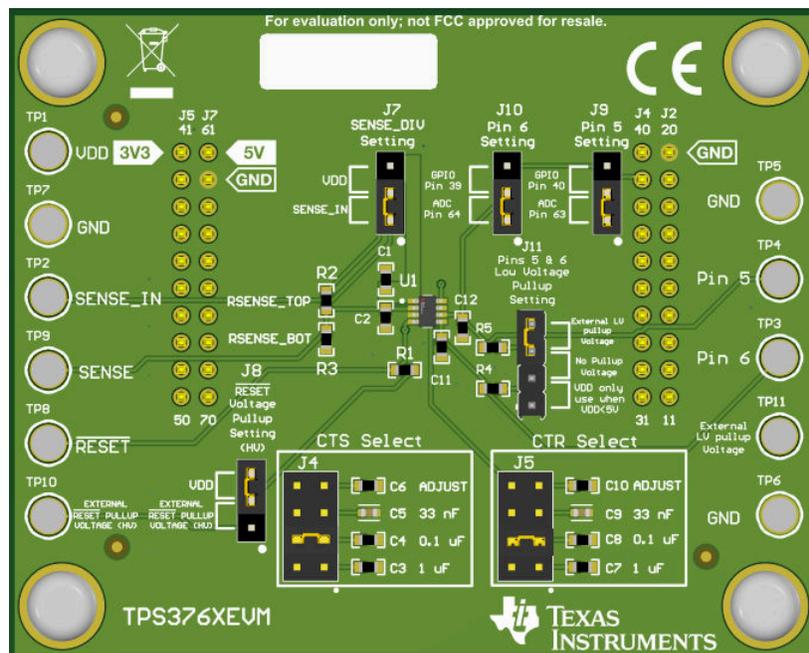


Description

The TPS376XEVM is an evaluation module (EVM) for the TPS3762-Q1 family of voltage supervisors. The purpose of this EVM is to provide a sample design and test point for all input and output pins of the TPS3762-Q1 device to capture measurements and gain familiarity with the device.

Features

- [Functional Safety-Compliant](#)
 - Developed for functional safety applications
- Wide supply voltage range: 2.6 V to 65 V
- Built-in self-test
- Output $\overline{\text{RESET}}$ latching



TPS376XEVM Board

1 Evaluation Module Overview

1.1 Introduction

The TPS376XEVM is an evaluation module (EVM) for the TPS3762-Q1 voltage supervisor. This family is an automotive-grade device with support for undervoltage and overvoltage supervisor and Built-In Self-Test functionality. The TPS376XEVM offers connections to all input and output pins. Test points are provided to give the user access to an extra connection if needed for oscilloscope or multimeter measurements.

1.2 Kit Contents

The TPS376XEVM circuit board comes pre-installed with the TPS3762D02OVDDFRQ1 device for full functionality testing of the TPS3762-Q1 family of devices. The TPS376XEVM circuit board comes packaged in a moisture barrier bag inside of antistatic foam layered cardboard box. Also contained in the box is the EVM literature disclaimer.

Table 1-1. Kit Contents

Item	Quantity
TPS376XEVM	1

1.3 Specification

		MIN	MAX	UNIT
Voltage	V_{DD}	2.7	65	V
Voltage	V_{SENSE} , V_{RESET}	0	65	V
Voltage	V_{CTS} , V_{CTR}	0	5.5	V
Current	I_{RESET} , I_{BIST}	0	±5	mA
Temperature	Operating junction temperature, T_J	-40	125	°C

1.4 Device Information

The TPS376XEVM is shipped pre-installed with the TPS3762D02OVDDFRQ1 device, but can be used with any TPS3762-Q1 variant. The TPS3762-Q1 family has built-in self-test functionality for voltages up to 65 V. The device also includes an optional reset output latching feature.

2 Hardware

2.1 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM.

2.1.1 EVM Jumpers

Table 2-1 lists the default jumper connections and functional description for the device configuration.

Table 2-1. Pinout & Onboard Jumpers

PIN NUMBER / NAME	JUMPER CONNECTION	DEFAULT CONNECTION	DESCRIPTION
Pin 8 / CTS	J4	Closed (pin 3, pin 4)	Jumper J4 configures the CTS pin. Connect a shunt jumper to: pins 1 & 2 to connect to C3, pins 3 & 4 to connect to C4, pins 5 & 6 to connect to C5, pins 7 & 8 to connect to C6. Refer to ### for capacitor values and sense delay timings.
Pin 7 / CTR	J5	Closed (pin 3, pin 4)	Jumper J5 configures the CTS pin. Connect a shunt jumper to: pins 1 & 2 to connect to C7, pins 3 & 4 to connect to C8, pins 5 & 6 to connect to C9, pins 7 & 8 to connect to C10. Refer to ### for capacitor values and reset delay timings.
Pin 2 / SENSE	J7	Closed (pin 1, pin 2)	Jumper J7 configures the SENSE pin. Connect a shunt jumper to pins 1 & 2 to connect to TP2 or pins 2 & 3 to connect to VDD.
Pin 4 / $\overline{\text{RESET}}$	J8	Closed (pin 2, pin 3)	Jumper J8 configures the $\overline{\text{RESET}}$ pin. Connect a shunt jumper to pins 1 & 2 to connect to TP10 or pins 2 & 3 to connect to VDD.
Pin 5 / BIST	J9	Closed (pin 1, pin 2)	Jumper J9 configures the BIST pin. Connect a shunt jumper to pins 1 & 2 to connect to ADC pin 63 or pins 2 & 3 to connect to GPIO pin 40.
Pin 6 / BIST_EN / LATCH_CLR	J10	Closed (pin 1, pin 2)	Jumper J10 configures the BIST_EN / LATCH_CLR pin. Connect a shunt jumper to pins 1 & 2 to connect to ADC pin 64 or pins 2 & 3 to connect to GPIO pin 39.
Pin 5 & 6 / BIST & BIST_EN / LATCH_CLR	J11	Closed (pin 3, pin 4)	Jumper J11 configures the BIST & BIST_EN / LATCH_CLR pin. This jumper connects a pull-up voltage to these pins to clear faults. Connect a shunt jumper to: pins 1 & 2 to connect to VDD, pins 2 & 3 for no connect, pins 3 & 4 to connect to TP11 (external pullup).

2.1.2 EVM Test Points

Table 2-2 lists the test point connections and functional description for the device configuration. Test points are placed throughout the board to verify pin functionality.

Table 2-2. Test Points

PIN NUMBER / NAME	Test Point	Description
Pin 1 / VDD	TP1	Test point TP1 connects to VDD.
Pin 1 / J7	TP2	Test point TP2 connects to J7 pin 1. If a shunt jumper is connected to pins 1 & 2 of J7 then TP2 connects to SENSE.
Pin 5 / BIST	TP3	Test point TP3 connects to BIST.
Pin 6 / BIST_EN / LATCH_CLR	TP4	Test point TP4 connects to BIST_EN / LATCH_CLR.
Pin 3 / GND	TP5	Test point TP5 connects to GND.
Pin 3 / GND	TP6	Test point TP6 connects to GND.
Pin 3 / GND	TP7	Test point TP7 connects to GND.
Pin 4 / $\overline{\text{RESET}}$	TP8	Test point TP8 connects to $\overline{\text{RESET}}$.
Pin 2 / SENSE	TP9	Test point TP9 connects to SENSE.
Pin 1 / J8	TP10	Test point TP10 connects to J8 pin 1. If a shunt jumper is connected to pins 1 & 2 of J8, then TP10 connects to $\overline{\text{RESET}}$ pullup (Used to set external $\overline{\text{RESET}}$ pull-up voltage).

Table 2-2. Test Points (continued)

PIN NUMBER / NAME	Test Point	Description
Pin 4 / J11	TP11	Test point TP11 connects to J11 pin 4. If a shunt jumper is connected to pins 3 & 4 of J11, then TP11 connects to BIST & BIST_EN / LATCH_CLR (Used to provide external pull-up voltage to these pins to clear faults).

2.2 EVM Setup and Operation

This section describes the functionality and operation of the TPS376XEVM. This EVM comes with the TPS3762D02OVDDFRQ1 device installed. Read the TPS3762-Q1 data sheet ([SNVSCE6](#)) for electrical characteristics of this device.

2.2.1 Input Supply Voltage (V_{DD})

The input supply voltage (V_{DD}) is connected through the TP1 on the board. The input supply voltage range is 2.7V to 65 V a 0.1 μ F decoupling capacitor is placed at the input for reducing noise that can propagate through the device (included on the EVM board at C1). Please refer to the device data sheet for additional details.

2.2.2 SENSE

The SENSE voltage is connected through TP9 on the board. Jumper J7 can also configure the SENSE pin to also connect to TP2 (Refer to [Table 2-1](#) for configuration options). The default option of the TPS376XEVM is populated with the TPS3762D02OVDDFRQ1 device, which has a 0.8V overvoltage threshold.

2.2.3 $\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ is connected through TP8 on the board. The $\overline{\text{RESET}}$ output on the device asserts on SENSE going outside the supervisor threshold. The device on the TPS376XEVM is the TPS3762D02OVDDFRQ1, which represents an overvoltage active-low open-drain output on $\overline{\text{RESET}}$.

2.2.4 Built-In Self-Test (BIST)

The BIST is connected through TP3 on the board. Jumper J11 can also configure the BIST pin to also connect to TP11 (Refer to [Table 2-1](#) for configuration options). The TPS3762-Q1 family of devices contain a Built-In Self-Test (BIST) pin for assessing internal device faults. BIST is asserted via the BIST_EN / Latch_CLR pin and remains asserted for a time period, TD_BIST. If BIST encounters a fault, then BIST remains asserted for a period longer than TD_BIST. BIST is an active-low open drain output and requires an external pull-up resistor and voltage. Please refer to the device data sheet for additional details.

2.2.5 Built-In Self-Test Enable and Latch Clear (BIST_EN / LATCH_CLR)

The BIST_EN / LATCH_CLR is connected through TP4 on the board. Jumper J11 can also configure the BIST_EN / LATCH_CLR pin to also connect to TP11 (Refer to [Table 2-1](#) for configuration options). The TPS3762-Q1 family of devices contain a Built-In Self-Test Enable and Latch Clear (BIST_EN / LATCH_CLR) pin for enabling the BIST, as well as clearing a BIST fault. The BIST_EN asserts BIST for a time period, TD_BIST. If BIST encounters a fault, then BIST remains asserted for a period longer than TD_BIST. LATCH_CLR requires a rising edge to clear the flagged fault on the BIST pin. Please refer to the device data sheet for additional details.

2.2.6 $\overline{\text{RESET}}$ Time Delay (CTR)

The TPS3762-Q1 family of devices contain an adjustable $\overline{\text{RESET}}$ time delay pin that controls the time with which the $\overline{\text{RESET}}$ pin de-asserts after reaching the valid condition. The user can adjust the configuration of this pin via the jumper located at J5. Refer to [Section 2.1.1](#) for jumper connections and TPS3762-Q1 data sheet ([SNVSCE6](#)) for capacitor values and $\overline{\text{RESET}}$ delay timings.

2.2.7 Sense Time Delay (CTS)

The TPS3762-Q1 family of devices contain an adjustable sense time delay pin that controls the time with which the $\overline{\text{RESET}}$ pin asserts after reaching the invalid condition. The user can adjust the configuration of this pin via the jumper located at J4. Refer to [Section 2.1.1](#) for jumper connections and TPS3762-Q1 data sheet ([SNVSCE6](#)) for capacitor values and sense delay timings.

3 Implementation Results

3.1 EVM Performance Results

The following measurements are taken using the default TPS376XEVM with the TPS3762D02OVDDFRQ1 device.

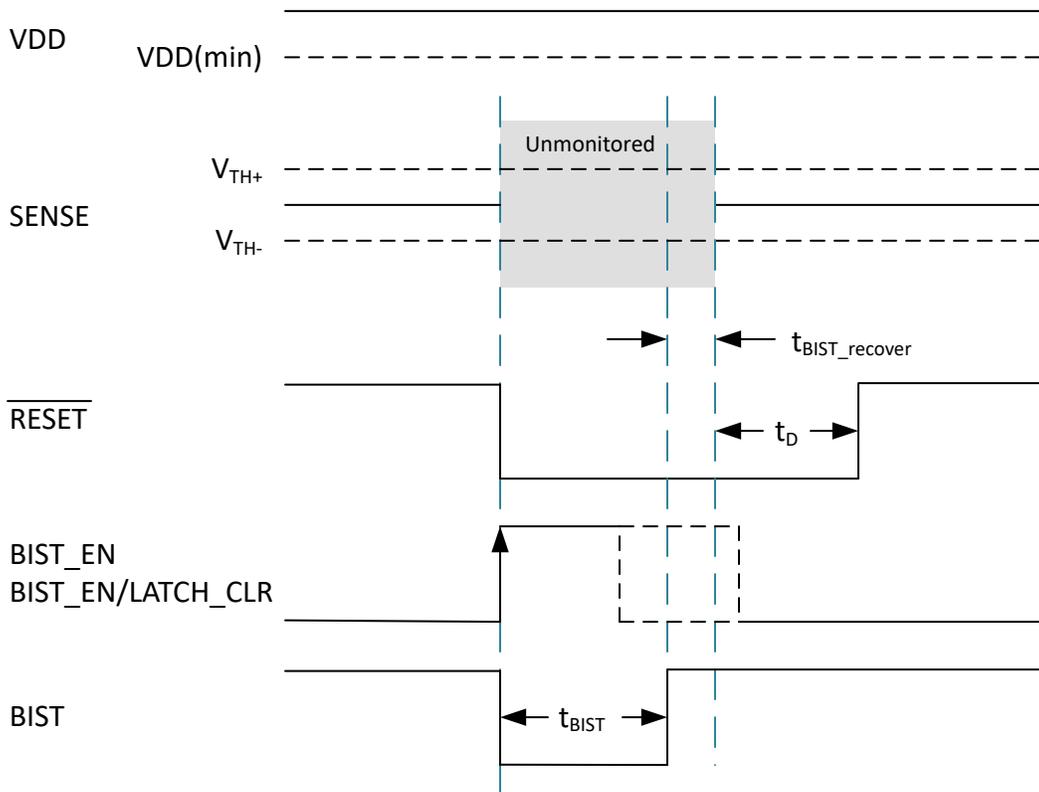


Figure 3-1. BIST with $\overline{\text{RESET}}$ assertion

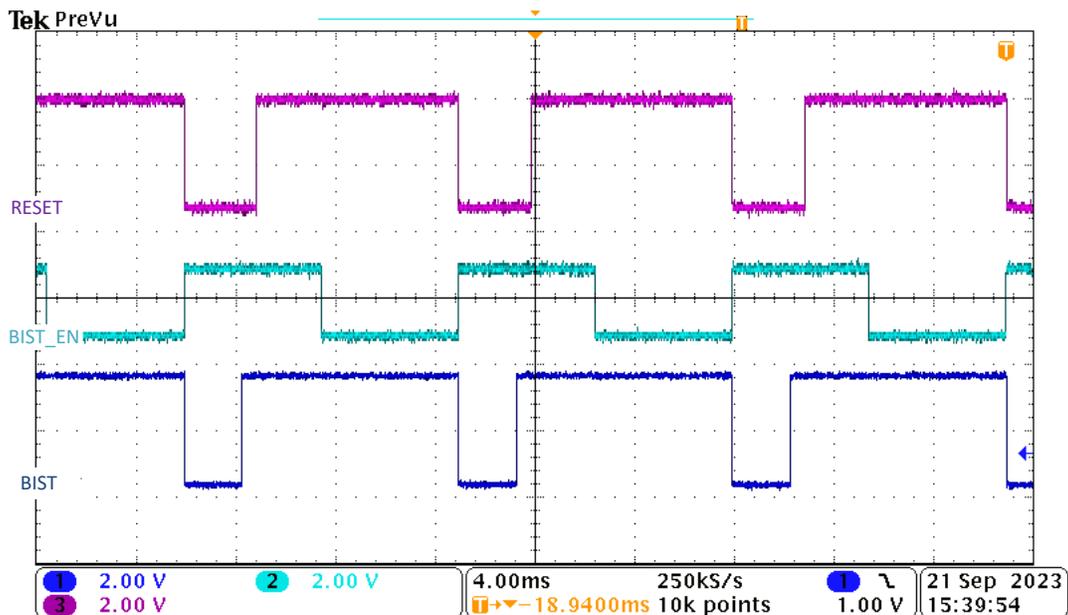


Figure 3-2. BIST with $\overline{\text{RESET}}$ assertion waveform

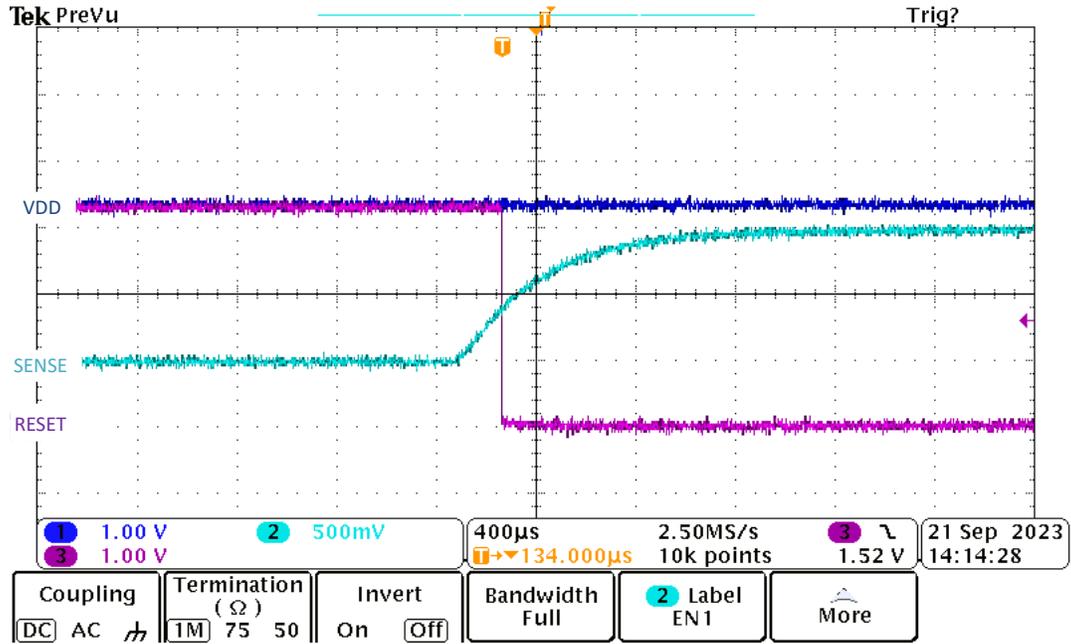


Figure 3-3. OV RESET Assertion waveform

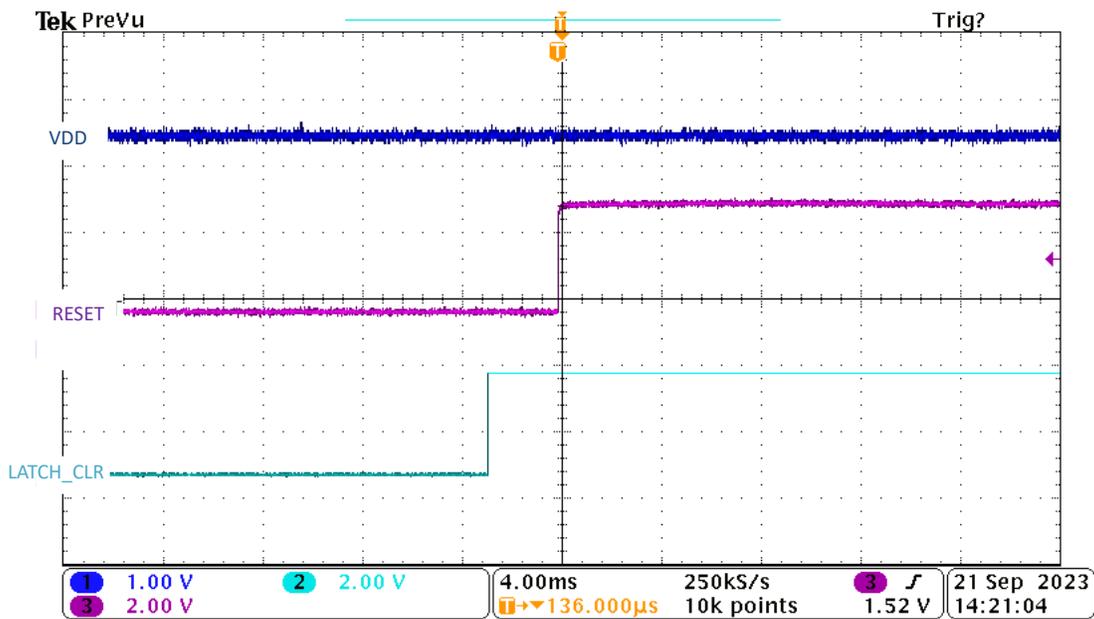


Figure 3-4. RESET Unlatch waveform

4.2 PCB Layout

Figure 4-2 and Figure 4-3 show the top and bottom assemblies of the printed circuit board (PCB) to display the component placement of the EVM.

Figure 4-4 and Figure 4-5 show the top and bottom layouts, Figure 4-6 and Figure 4-7 show the top and bottom layers, and Figure 4-8 shows the top solder mask of the EVM.

Some board variants come with R5, C11, and C12 populated, please remove these components for proper testing of BIST functionality

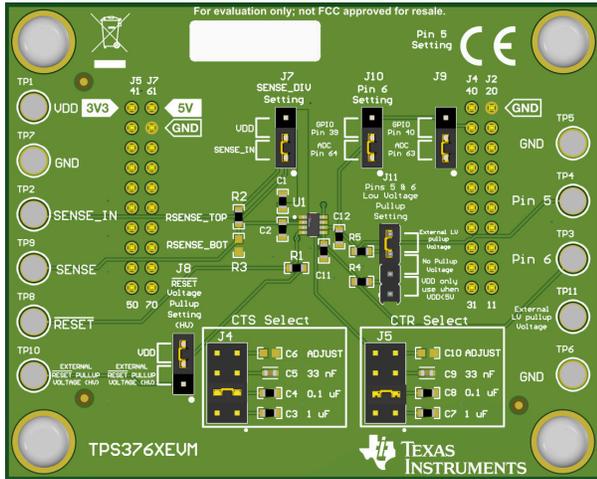


Figure 4-2. Component Placement - Top Assembly

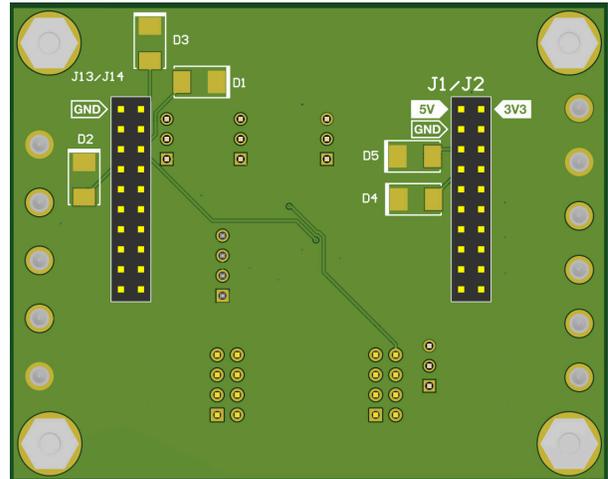


Figure 4-3. Component Placement - Bottom Assembly

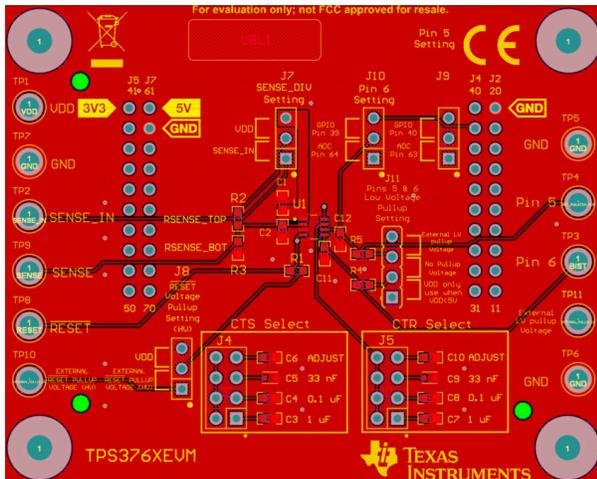


Figure 4-4. Layout - Top

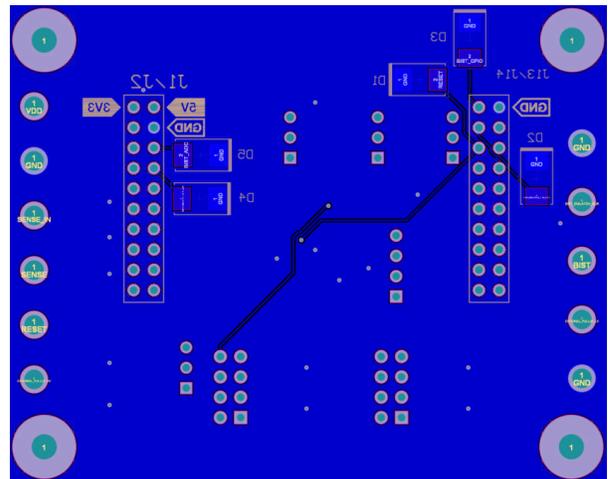


Figure 4-5. Layout - Bottom

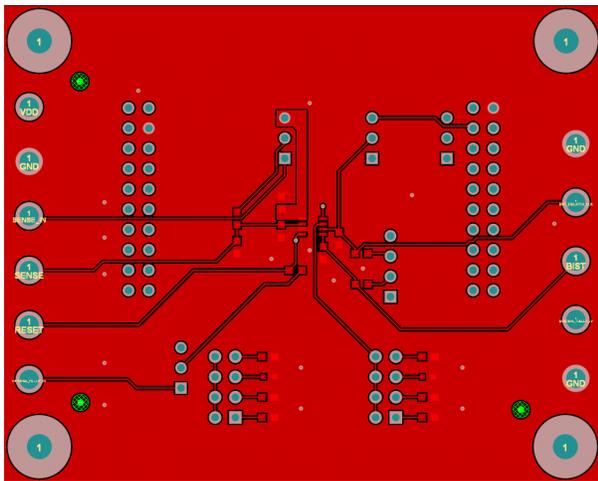


Figure 4-6. Top Layer

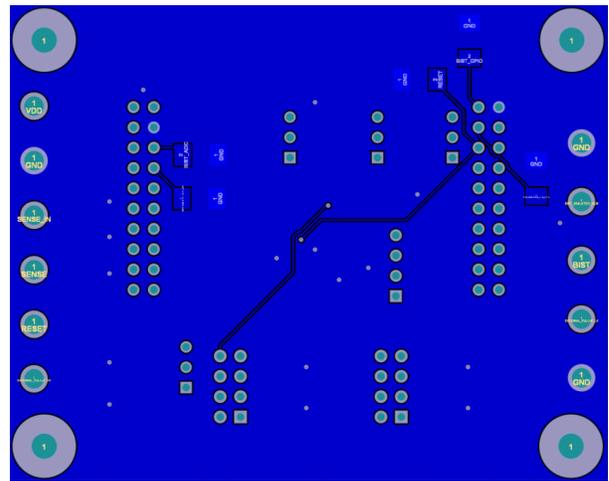


Figure 4-7. Bottom Layer

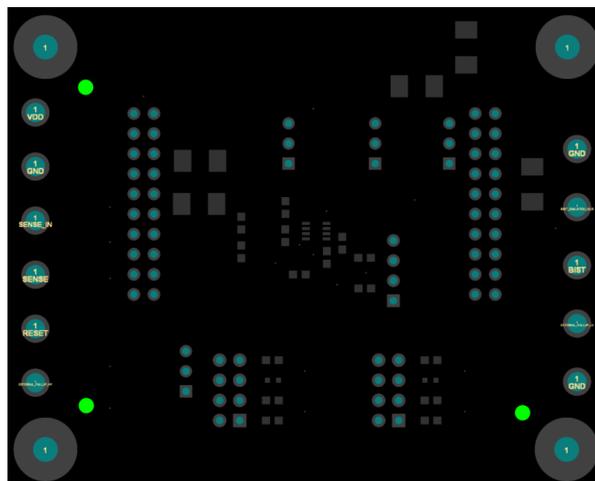


Figure 4-8. Top Solder Mask

4.3 Bill of Materials

Table 4-1. TPS376XEVM Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB	1		Printed Circuit Board		LP098A	Any
C1, C2, C11, C12	4	0.1uF	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, 0603	0603	GRM188R72A104KA35D	Murata
C3, C7	2	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C1608X7R1E105K	TDK
C4, C8	2	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603	0603	0603YC104JAT2A	KYOCERA AVX
C5, C9	2	33 nF	CAP, CER, 33 nF, 50 V, +/- 10%, X7R, 0603	0603	CL10B333KB8WPNC	Samsung Electro-Mechanics
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1/J2, J13/14	2		Receptacle, 2.54mm, 10x2, Tin, TH	10x2 Receptacle	SSQ-110-03-T-D	Samtec
J4, J5	4		Header, 2.54mm, 80x2, Gold, TH	4x2 Header	61308021121	Würth Elektronik
J7, J8, J9, J10	4		Header, 2.54mm, 40x1, Gold, TH	3x1 Header	61304011121	Würth Elektronik
J11	1		Header, 2.54mm, 40x1, Gold, TH	4x1 Header	61304011121	Würth Elektronik
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H	PCB Label 0.650 x 0.200 inch	THT-47-718-10	Brady
R1, R4, R5	3	10k	RES, 10k, +/- 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RC0603FR-0710KL	YAGEO
R2	1	0	RES, 0, +/- 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7	7	1x2	Shunt, 100mil, Gold plated, Black	Shunt	QPC02SXGN-RC	Sullins Connector Solutions
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11	11		Terminal, Turret, TH, Triple	Keystone159 8-2	1598-2	Keystone
U1	1		Wide VIN 65 V Dual Channel Overvoltage & Undervoltage (OV & UV) Detector with Built-in Self-test for Automotive	SOT023-8	TPS37A010122DSKRQ1	Texas Instruments

5 Additional Information

Trademarks

All trademarks are the property of their respective owners.

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。 <https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html>

3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4. *EVM Use Restrictions and Warnings:*
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 *Safety-Related Warnings and Restrictions:*
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
 - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
 5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
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