User's Guide

TPS6290x-Q1 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

The TPS6290x-Q1EVM (BSR196) facilitates the evaluation of the TPS6290x-Q1 1-A, 2-A, and 3-A pin-to-pin compatible buck converters in small 2.2-mm × 2-mm VQFN packages with wettable flank. The BSR196-003 uses the 3-A TPS62903-Q1 to output a 1.2-V output voltage from input voltages between 3 V and 18 V. The BSR069-002 uses the 2-A TPS62902-Q1 to output a 1.8-V output voltage from input voltages between 3 V and 18 V. The BSR069-001 uses the 1-A TPS62901-Q1 to output a 3.3-V output voltage from input voltages up to 18 V. The TPS6290x-Q1 are high-efficiency, low I_Q, Grade 1 AEC-Q100-qualified buck converters that can be used in a variety of automotive applications, such as the following:

- ADAS
- Body electronics and lighting
- Infotainment and cluster
- Hybrid, electric, and powertrain systems
- Any application with a 12-V input voltage or a 1-4 cell lithium battery pack

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Trademarks

1 Introduction

The TPS6290x-Q1 are synchronous, step-down converters in a small 2.2-mm × 2-mm × 0.5-mm VQFN package with wettable flank. Three different devices in this family support 1-A, 2-A, or 3-A output current.

1.1 Performance Specification

Table 1-1, Table 1-2, and Table 1-3 provide a summary of the TPS6290x-Q1EVM performance specifications.

Table 1-1. TPS62903-Q1EVM Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
Input voltage		3	12	18	V
Output voltage setpoint			1.2		V
Output current		0		3	A
MODE/S-CONF (R4) setting	2.5 MHz, auto PFM/PWM with AEE, external FB, output discharge disabled		7.15		kΩ

Table 1-2. TPS62902-Q1EVM Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
Input voltage		3	12	18	V
Output voltage setpoint			1.8		V
Output current		0		2	A
MODE/S-CONF (R4) setting	1 MHz, auto PFM/PWM, external FB, output discharge disabled		16.9		kΩ

Table 1-3. TPS62901-Q1EVM Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
Input voltage		3.4	12	18	V
Output voltage setpoint			3.3		V
Output current		0		1	A
MODE/S-CONF (R4) setting	1 MHz, auto PFM/PWM, external FB, output discharge disabled		16.9		kΩ

1.2 Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate some user modifications. Additional input and output capacitors can be added. Also, the following modifications can be made:

- The input voltage at which the IC turns on can be adjusted with two resistors.
- The soft-start time can be changed.
- The output voltage can track an applied voltage.
- A feedforward capacitor can be added.
- The switching frequency, output discharge setting, MODE setting, and output voltage setting configuration can be changed.

Finally, the loop response can be measured. See the *TPS62903-Q1, 3-V to 18-V, Low I_Q Buck Converter in 2.2-mm × 2-mm VQFN with Wettable Flank Package* data sheet for details of the various settings.

1.2.1 Input and Output Capacitors

C6, C7, and C8 are provided for additional input capacitors. These capacitors are not required for proper operation but can be used to reduce the input voltage ripple.

C9, C10, C11, and C12 are provided for additional bulk output capacitors. These capacitors are not required for proper operation but can be used to reduce the output voltage ripple. The total output capacitance must remain within the recommended range in the *TPS62903-Q1, 3-V to 18-V, Low I_Q Buck Converter in 2.2-mm × 2-mm VQFN with Wettable Flank Package* data sheet for proper operation.

1.2.2 Configurable Enable Threshold Voltage

With JP1 removed, R5 and R6 can be installed to set a user-selectable input voltage at which the IC turns on.

1.2.3 SS/TR Capacitor

C3 sets the soft-start time. This capacitor can be changed to set other soft-start times.

1.2.4 Feedforward Capacitor

C5 is provided as an optional feedforward capacitor (C_{FF}).

1.2.5 MODE/S-CONF Resistor

R4 selects the following:

- Switching frequency
- Output discharge
- MODE setting
- Output voltage setting configuration

When selecting a different switching frequency, the inductor value should also be changed. When using the VSET configuration for setting the output voltage, remove R1 and change the value of R2. See the *TPS62903-Q1, 3-V to 18-V, Low I_Q Buck Converter in 2.2-mm × 2-mm VQFN with Wettable Flank Package* data sheet for details of the various settings.

1.2.6 Loop Response Measurement

The loop response can be measured with simple changes to the circuitry. First, install a 10-Ω resistor across the pads of R9 on the back of the PCB. The pads are spaced to allow installation of an 0603-sized resistor. Next, cut the short section of trace on the top layer between the via on pin 3 and C2. Figure 1-1 shows this change. With these changes, an AC signal (10-mV, peak-to-peak amplitude recommended) can be injected into the control loop across the added 10-Ω resistor. Figure 4-2 shows the results of this test.

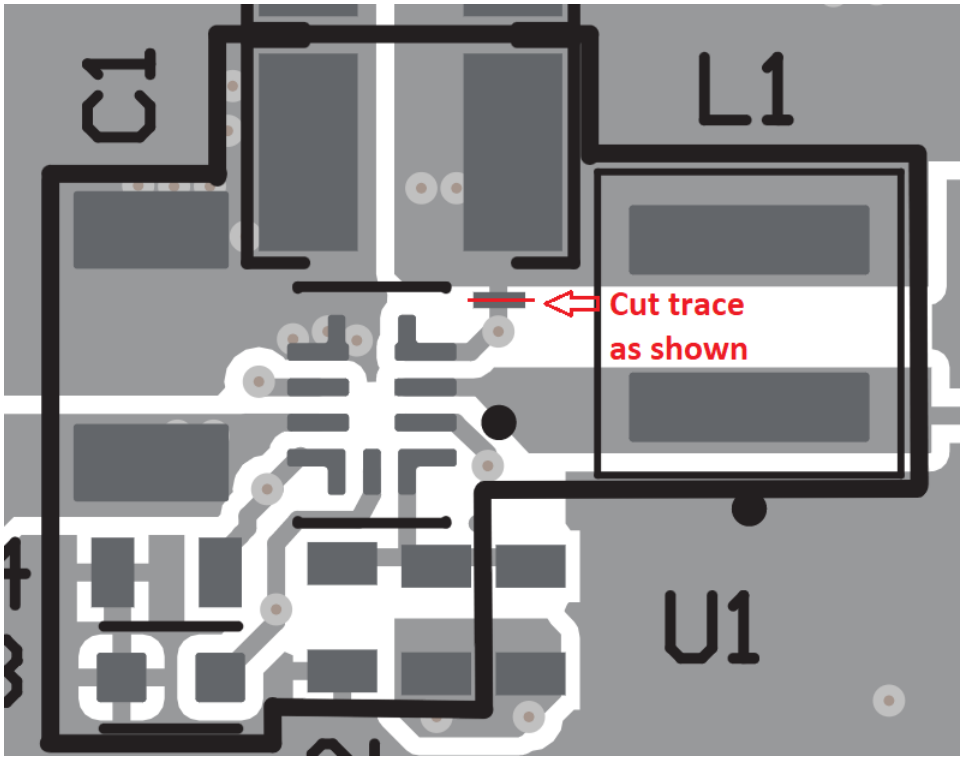

Figure 1-1. Loop Response Measurement Modification (Top Layer)

2 Setup

This section describes how to properly use the EVM.

2.1 Input/Output Connector Descriptions

J1, Pin 1 and 2 – V_{IN}	Positive input connection from the input supply for the EVM
J1, Pin 3 and 4 – S+ or S–	Input voltage sense connections. Measure the input voltage at this point.
J1, Pin 5 and 6 – GND	Return connection from the input supply for the EVM
J2, Pin 1 and 2 – V_{OUT}	Output voltage connection
J2, Pin 3 and 4 – S+ or S–	Output voltage sense connections. Measure the output voltage at this point.
J2, Pin 5 and 6 – GND	Output return connection
J3 – PG or GND	The PG output is on pin 1 of this header with a convenient ground on pin 2.
J4 – TRACK-IN, SS/TR, or GND	By removing C3, the IC tracks an externally applied voltage. Apply the voltage on pin 1 to scale the applied voltage through R7 and R8. The SS/TR voltage can be measured on pin 2.
J5 – SW or GND	This header is not installed. Use the holes in the PCB to measure the SW node on pin 2 with a convenient GND on pin 1.
JP1 – EN	EN pin input jumper. Place the supplied jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC. Remove the jumper to set a configurable enable threshold voltage with R5 and R6.
JP2 – MODE/S-CONF	MODE/S-CONF pin input jumper. Place the supplied jumper across PWM and MODE/S-CONF to operate the IC in forced PWM mode. Place the jumper across PFM/PWM and MODE/S-CONF to operate the IC in auto PFM/PWM mode. Remove the jumper to operate the IC with the MODE/S-CONF settings set by R4.

Note

If it is desired to change between PWM and PFM/PWM modes during operation, JP2 must be set to either PWM or PFM/PWM before enabling the IC.

JP3 – PG Pullup Voltage	PG pin pullup voltage jumper. Place the supplied jumper on JP3 to connect the PG pin pullup resistor to V_{OUT}. Alternatively, the jumper can be removed and a different voltage can be supplied on pin 1 to pull up the PG pin to a different level. This externally applied voltage must remain below 18 V.

3 Safety Instructions

WARNING

Hot surface. Contact may cause burns. Do not touch.

4 Test Results

The TPS6290x-Q1EVM was used to take all the data in the *TPS62903-Q1, 3-V to 18-V, Low I_Q Buck Converter in 2.2-mm × 2-mm VQFN with Wettable Flank Package* data sheet. See the device data sheet for the performance of this EVM.

Figure 4-1 shows the thermal performance of the EVM. "Spot" shows the temperature of the PCB. Figure 4-2 shows the loop response measurement.

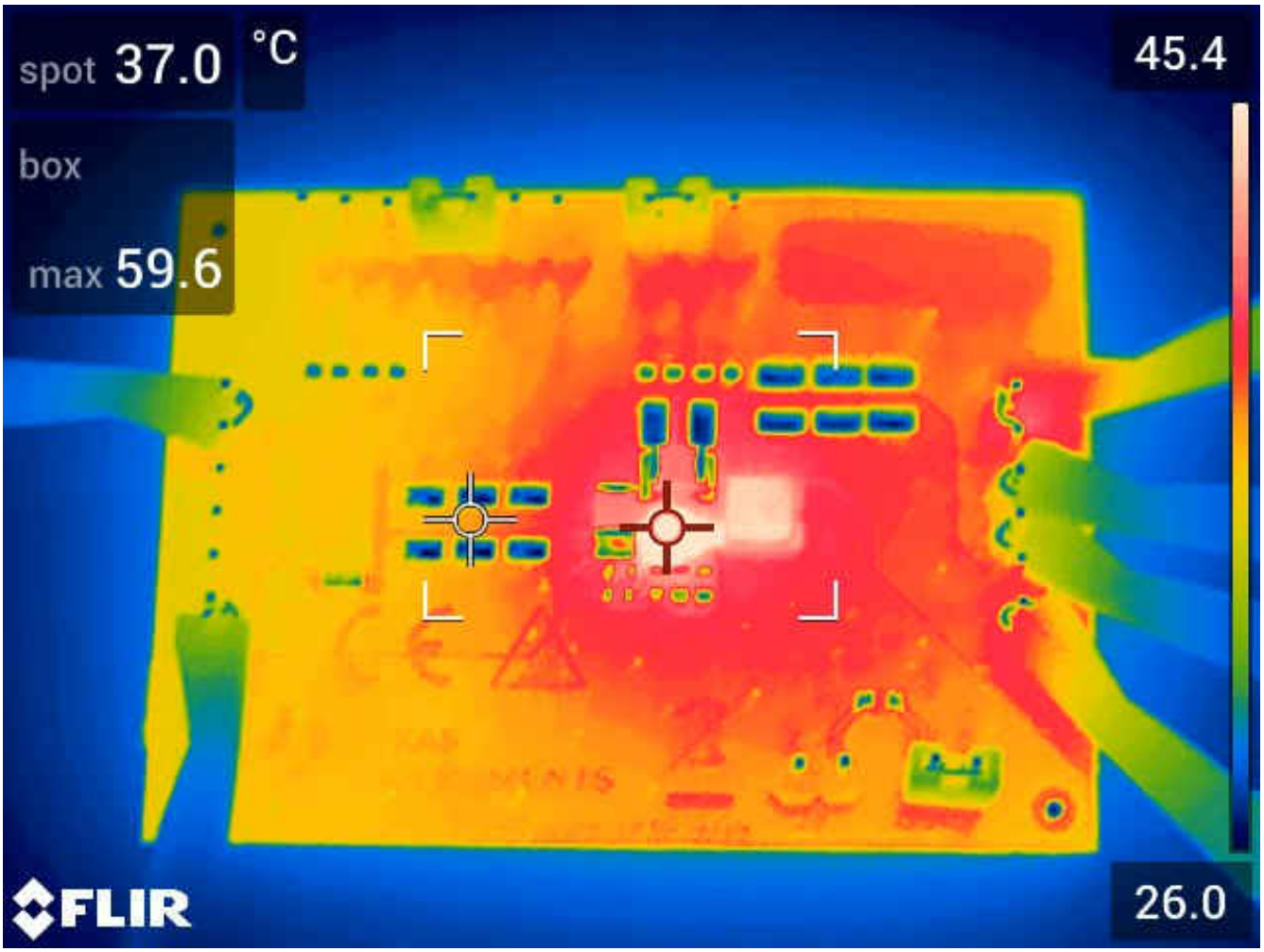

Figure 4-1. Thermal Performance (V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 3000 mA, JP2 Open)

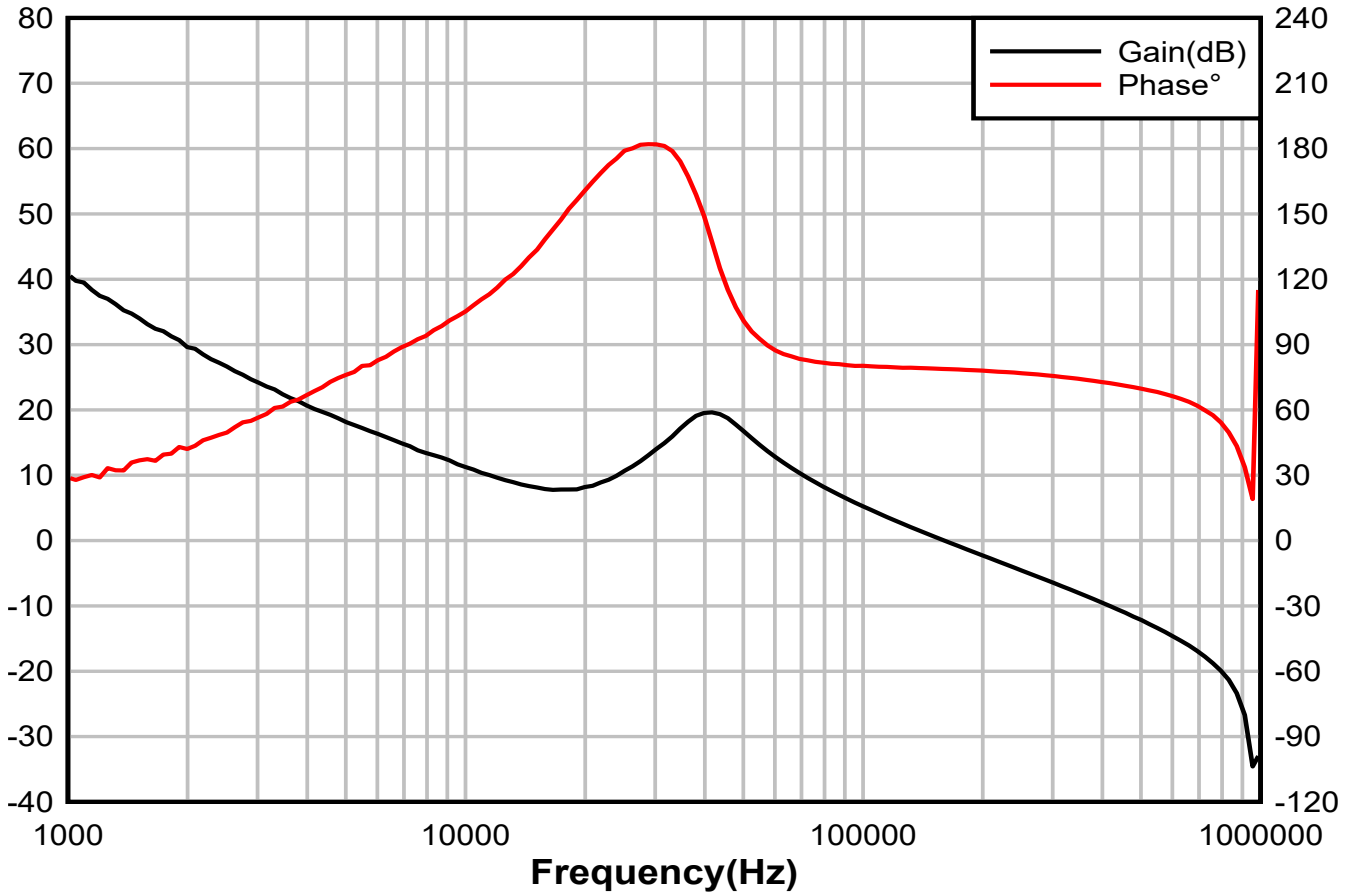

Figure 4-2. Loop Response Measurement (V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 3000 mA, JP2 Open)

5 Board Layout

This section provides the EVM board layout and illustrations in Figure 5-1 through Figure 5-6. The Gerbers are available on the EVM product page.

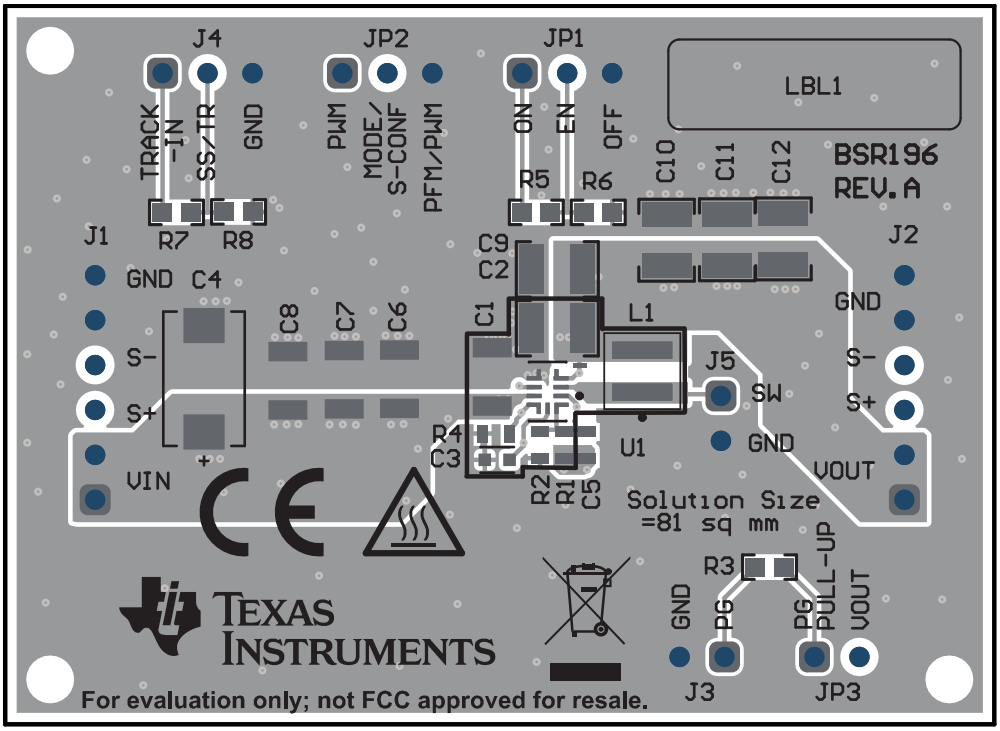

Figure 5-1. Top Assembly

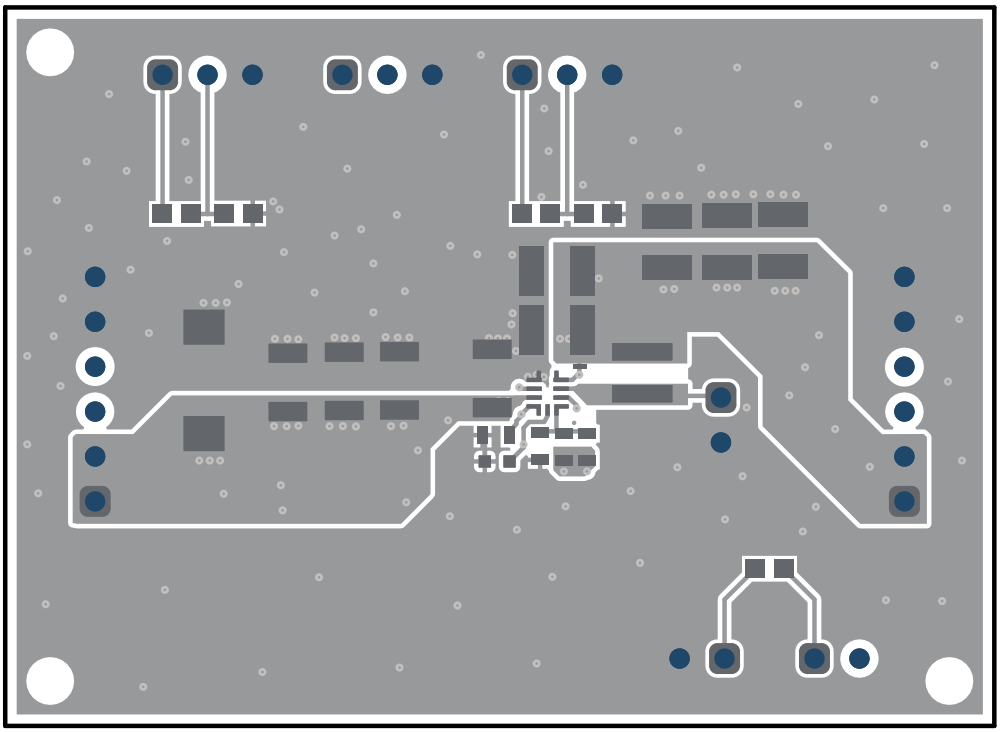

Figure 5-2. Top Layer

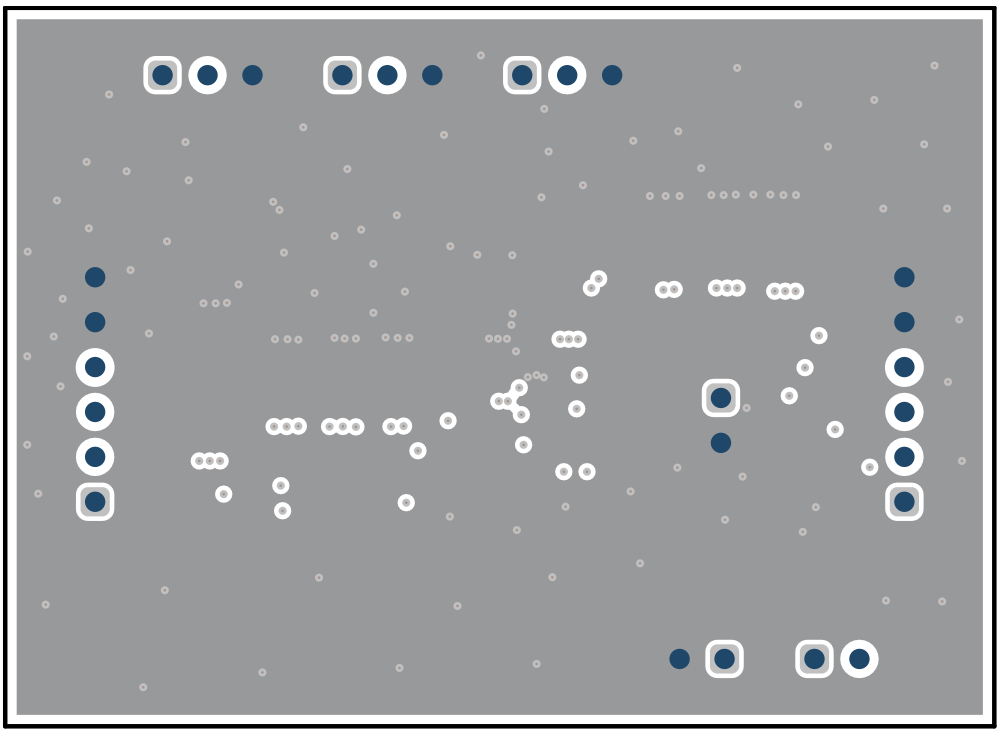

Figure 5-3. Internal Layer 1

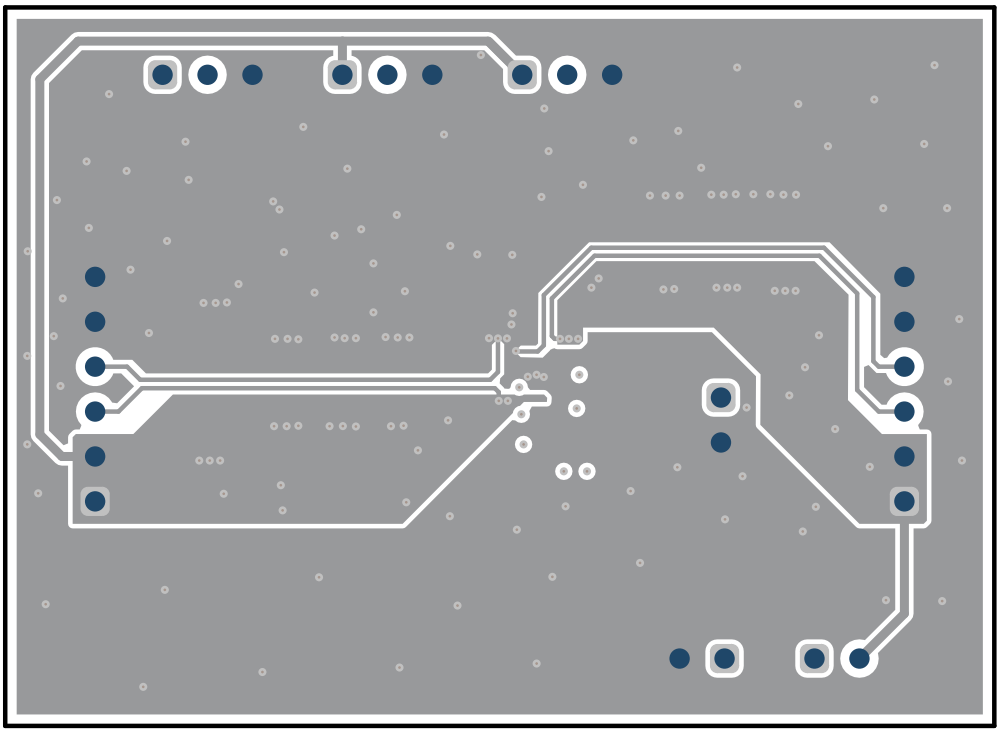

Figure 5-4. Internal Layer 2

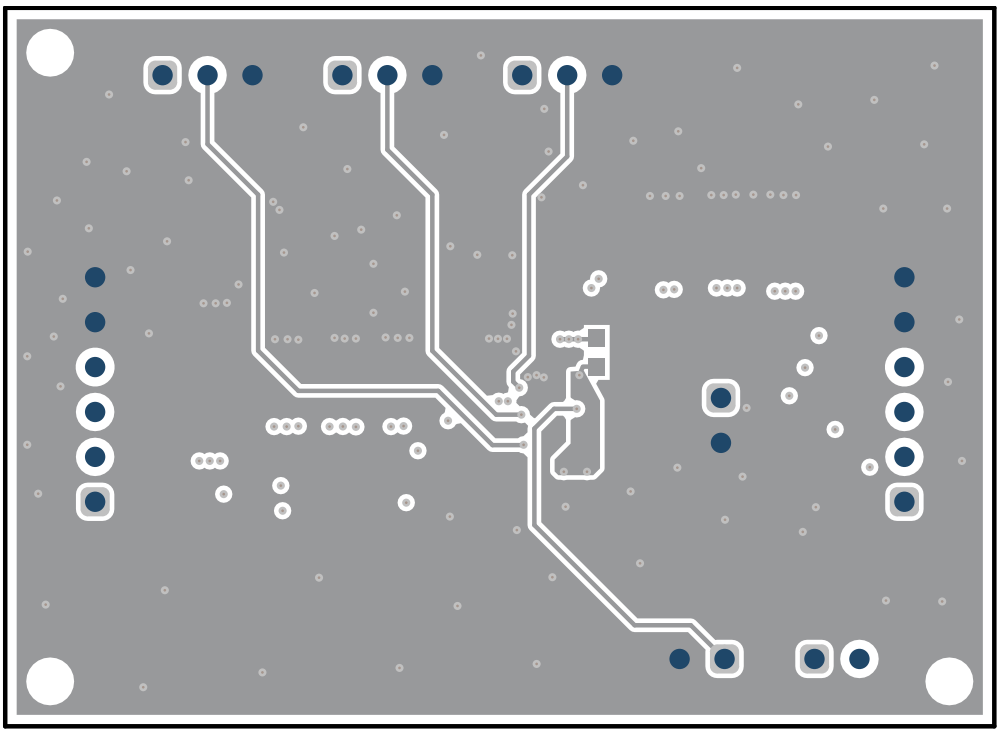

Figure 5-5. Bottom Layer

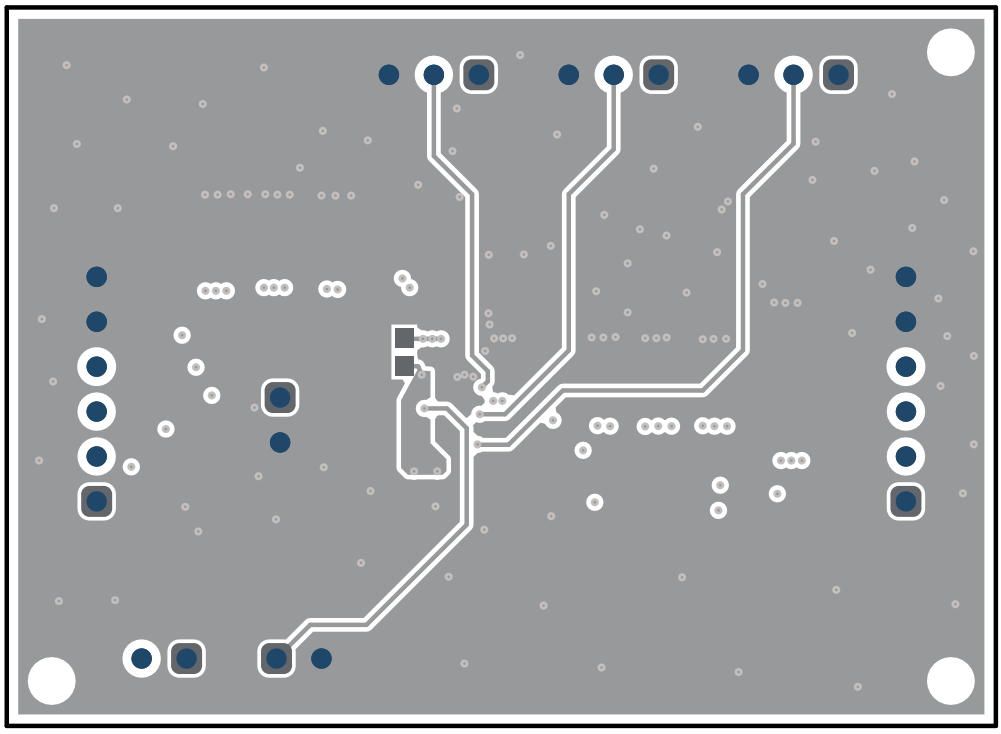

Figure 5-6. Bottom Layer (Mirrored)

6 Schematic and Bill of Materials

This section provides the EVM schematic and bill of materials (BOM).

6.1 Schematic

Figure 6-1, Figure 6-2, and Figure 6-3 illustrate the EVM schematics.

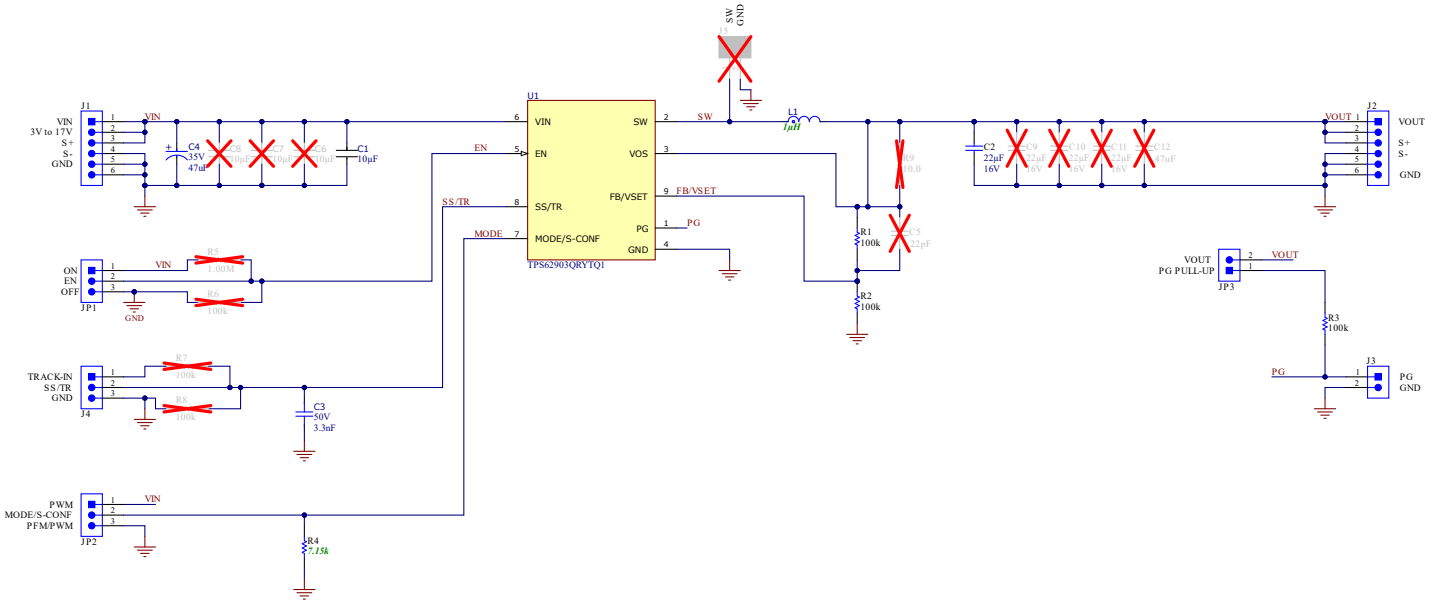

Figure 6-1. TPS62903-Q1EVM Schematic

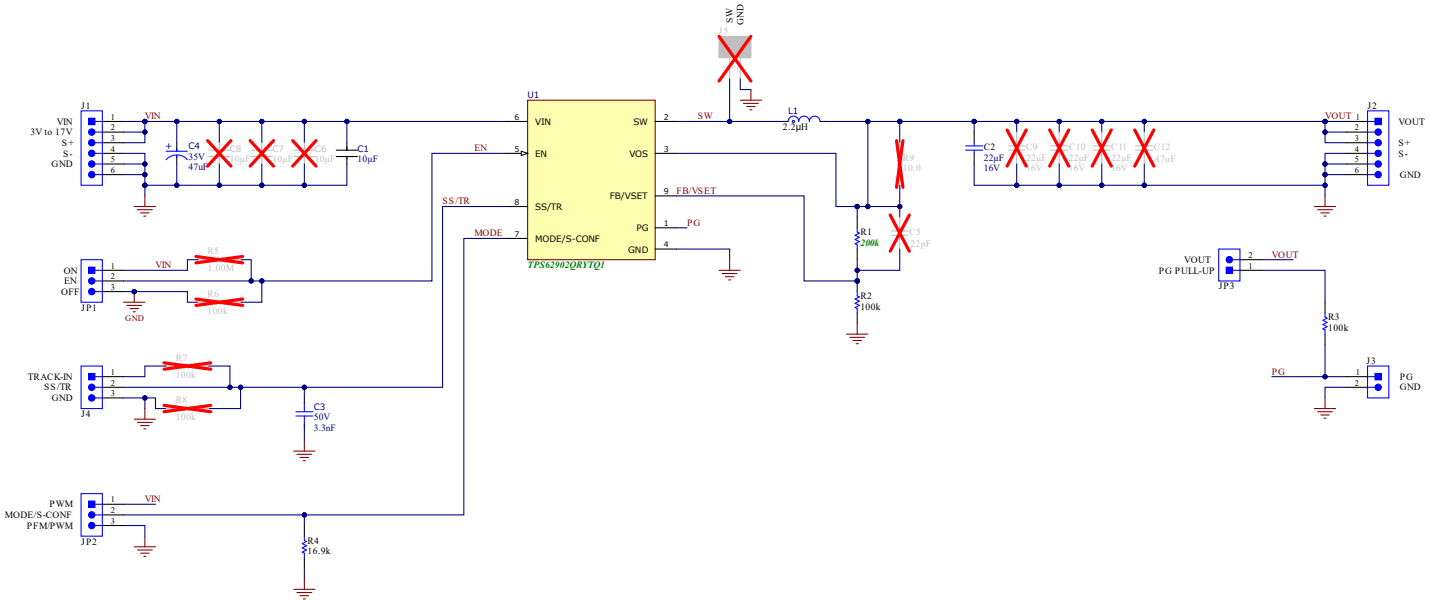

Figure 6-2. TPS62902-Q1EVM Schematic

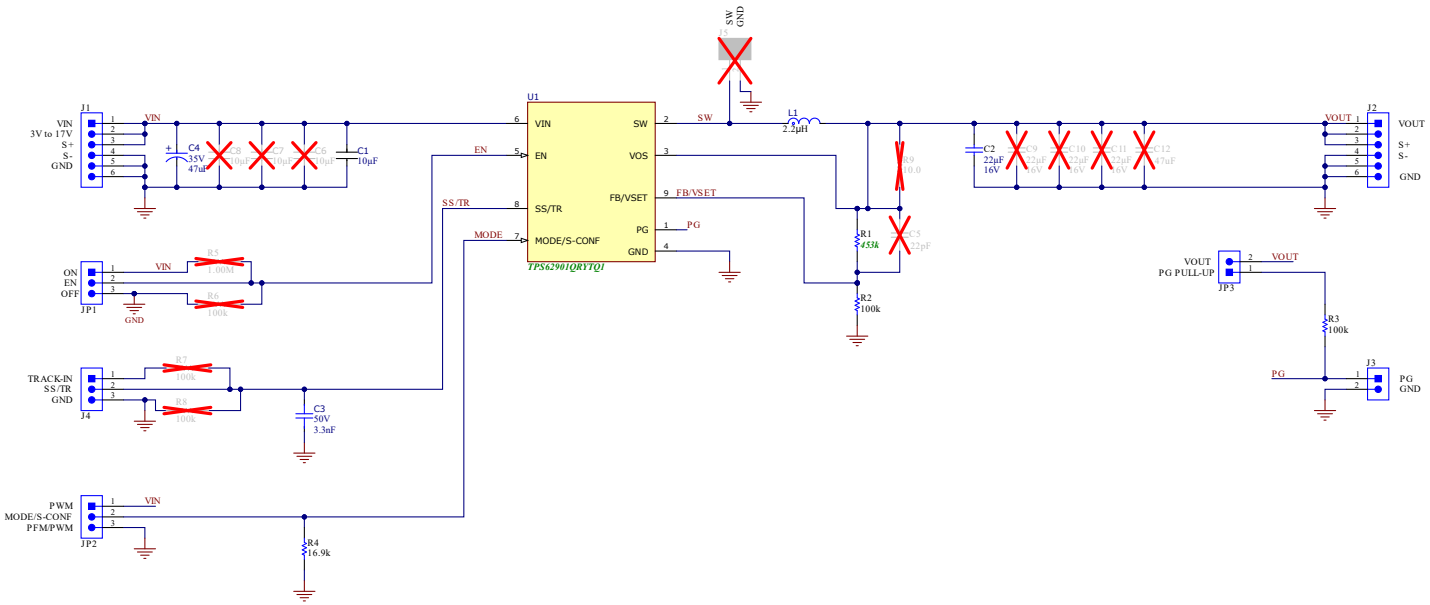

Figure 6-3. TPS62901-Q1EVM Schematic

6.2 Bill of Materials

Table 6-1 lists the BOM for this EVM.

Table 6-1. TPS6290x-Q1EVM Bill of Materials

-001	-002	-003	Reference Designator	Value	Description	Package	Part Number	Manufacturer
1	1	1	C1	10 µF	CAP, CERM, 10 µF, 25 V, ±10%, X8R	1210	CGA6P1X8R1E106K250AE	TDK
1	1	1	C2	22 µF	CAP, CERM, 22 µF, 16 V, ±20%, X8L	1210	CGA6P1X8L1C226M250AC	TDK
1	1	1	C3	3300 pF	CAP, CERM, 3300 pF, 50 V, ±20%, X8R	0603	CGA3E2X8R1H332M080AA	TDK
1	1	1	C4	47 µF	CAP, TA, 47 µF, 35 V, ±10%, 0.5 Ω	2917	T498X476K035ATE500	Kemet
0	0	1	L1	1 µH	Inductor Power Shielded Wirewound 1-µH, 20% Composite, 8.8-A, 8.2-mΩ DCR	4 mm × 4 mm	XGL4020-102MEC	Coilcraft
1	1	0	L1	2.2 µH	Inductor Power Shielded Wirewound 2.2-µH, 20% Composite, 6.2-A, 19.5-mΩ DCR	4 mm × 4 mm	XGL4020-222MEC	Coilcraft
1	0	0	R1	453 kΩ	RES, 453 kΩ, 1%, 0.1 W	0603	Std	Std
0	1	0	R1	200 kΩ	RES, 200 kΩ, 1%, 0.1 W	0603	Std	Std
0	0	1	R1	100 kΩ	RES, 100 kΩ, 1%, 0.1 W	0603	Std	Std
2	2	2	R2, R3	100 kΩ	RES, 100 kΩ, 1%, 0.1 W	0603	Std	Std
1	1	0	R4	16.9 kΩ	RES, 16.9 kΩ, 1%, 0.1 W	0603	Std	Std
0	0	1	R4	7.15 kΩ	RES, 7.15 kΩ, 1%, 0.1 W	0603	Std	Std
1	0	0	U1	TPS62901-Q1(1)	3-V to 18-V, 1-A, low I_Q buck converter in 2.2-mm × 2-mm VQFN package with wettable flank	2.2 mm × 2 mm	TPS62901QRYTRQ1	Texas Instruments
0	1	0	U1	TPS62902-Q1(1)	3-V to 18-V, 2-A, low I_Q buck converter in 2.2-mm × 2-mm VQFN package with wettable flank	2.2 mm × 2 mm	TPS62902QRYTRQ1	Texas Instruments
0	0	1	U1	TPS62903-Q1(1)	3-V to 18-V, 3-A, low I_Q buck converter in 2.2-mm × 2-mm VQFN package with wettable flank	2.2 mm × 2 mm	TPS62903QRYTRQ1	Texas Instruments

(1) The TPS6290x-Q1EVM may be populated with TPS6290x-Q1 (U1) devices that do not contain the correct top-side markings on the top of the device itself. These devices are still fully tested TPS6290x-Q1 devices.

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