

LMR36506MSCEVM User's Guide

The Texas Instruments LMR36506MSCEVM evaluation module help designers evaluate the operation and performance of the LMR36506-Q1 wide-input buck converters. The LMR36506-Q1 is an easy-to-use synchronous step-down DC/DC converter capable of driving up to 0.6 A of load current from an input voltage of up to 65 V. The LMR36506MSCEVM features an output voltage of 5 V and a switching frequency of 2.2 MHz. See the [LMR36506-Q1 3-V-65-V, 0.6-A Synchronous Buck Converter Optimized for Size and Light Load Efficiency](#) data sheet for additional features, detailed descriptions, and available options.

Table 1. Device and Package Configurations

EVM	U1	FREQUENCY	SPREAD SPECTRUM	CURRENT	PIN 1 TRIM
LMR36506MSCEVM	LMR36506MSCQRPETQ1	2200 kHz	Enabled	0.6 A	MODE/SYNC

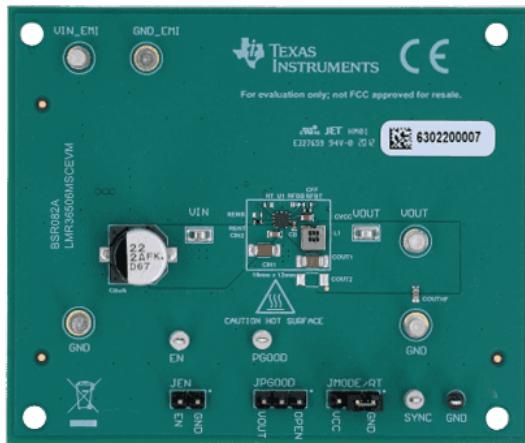


Figure 1. LMR36506MSCEVM Board

Contents

1	Setup	3
2	Operation	5
3	Schematic.....	6
4	Board Layout	7
5	Bill of Materials	10
6	Test Results	11

List of Figures

1	LMR36506MSCEVM Board	1
2	EVM Board Connections.....	3
3	Jumper Locations.....	4
4	LMR36506MSCEVM Schematic.....	6
5	Top View of EVM	7
6	EVM Top Copper Layer.....	7
7	EVM Mid Layer One.....	8
8	EVM Mid Layer Two.....	8
9	EVM Bottom Copper Layer.....	9
10	LMR36506MSCEVM 5 V _{OUT} Efficiency	11
11	LMR36506MSCEVM 5 V _{OUT} Load Regulation	11
12	LMR36506MSCEVM Load Transient 12 V _{IN} , 5 V _{OUT} , I _{OUT} = 0.3 A to 0.6 A, T _R = T _F = 1 μs CH1 = V _{OUT} , CH4 = I _{OUT}	11
13	LMR36506MSCEVM Output Ripple 12 V _{IN} , 5 V _{OUT} , I _{OUT} = 0 A.....	11
14	LMR36506MSCEVM 5 V _{OUT} Thermal Capture, 12 V _{IN} , 0.6 A Load, 2.2 MHz	12
15	LMR36506MSCEVM 5 V _{OUT} Thermal Capture, 24 V _{IN} , 0.6 A Load, 2.2 MHz	12
16	LMR36506MSCEVM CISPR25 Conducted EMI Results 13.5 V _{IN} , 5 V _{OUT} , I _{OUT} = 0.6 A (Blue-Average and Yellow-Peak)	12
17	LMR36506MSCEVM CISPR25 Conducted EMI Results 13.5 V _{IN} , 5 V _{OUT} , I _{OUT} = 0.6 A (Blue-Average and Yellow-Peak)	12

List of Tables

1	Device and Package Configurations	1
2	Bill of Materials	10

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1 Setup

This section describes the test points and connectors on the EVM and how to properly connect, set up, and use the LMR36506MSCEVM.

1.1 Test Points

The test points on the top of the board can be used for connecting to the input and output of the EVM. See [Figure 2](#) for typical test setup. The functions of the test points connections are:

- **VIN_EMI** — Input supply to EVM including an EMI filter. Connect to a suitable input supply. Connect at this point for conducted EMI test.
- **GND_EMI** — Ground connection for the input supply
- **VIN** — Input supply to the IC. Can be connected to DMM to measure input voltage after EMI filter
- **VOUT** — Output voltage test point of EVM. Can be connected to a desired load
- **GND** — Ground test points
- **EN** — This test point is connected to the EN pin. By default, there is a pullup resistor R2 (RENT) to VIN to enable the IC.
- **PGOOD** — This test point is connected to the PGOOD pin from the IC. It is an open-drain output of the PGOOD pin. Can be tied to external supply through a pullup resistor or left open
- **SYNC** — In a **MODE/SYNC** trim part, this test point is connected to the SYNC pin of the IC. Can be connected to an external clock to synchronize the IC. Make sure R4 (RMODE) is installed and R5 (RT) is not installed. In a **RT** trim part, this test point is connected to the RT pin of the IC when the R4 (RMODE) is installed.

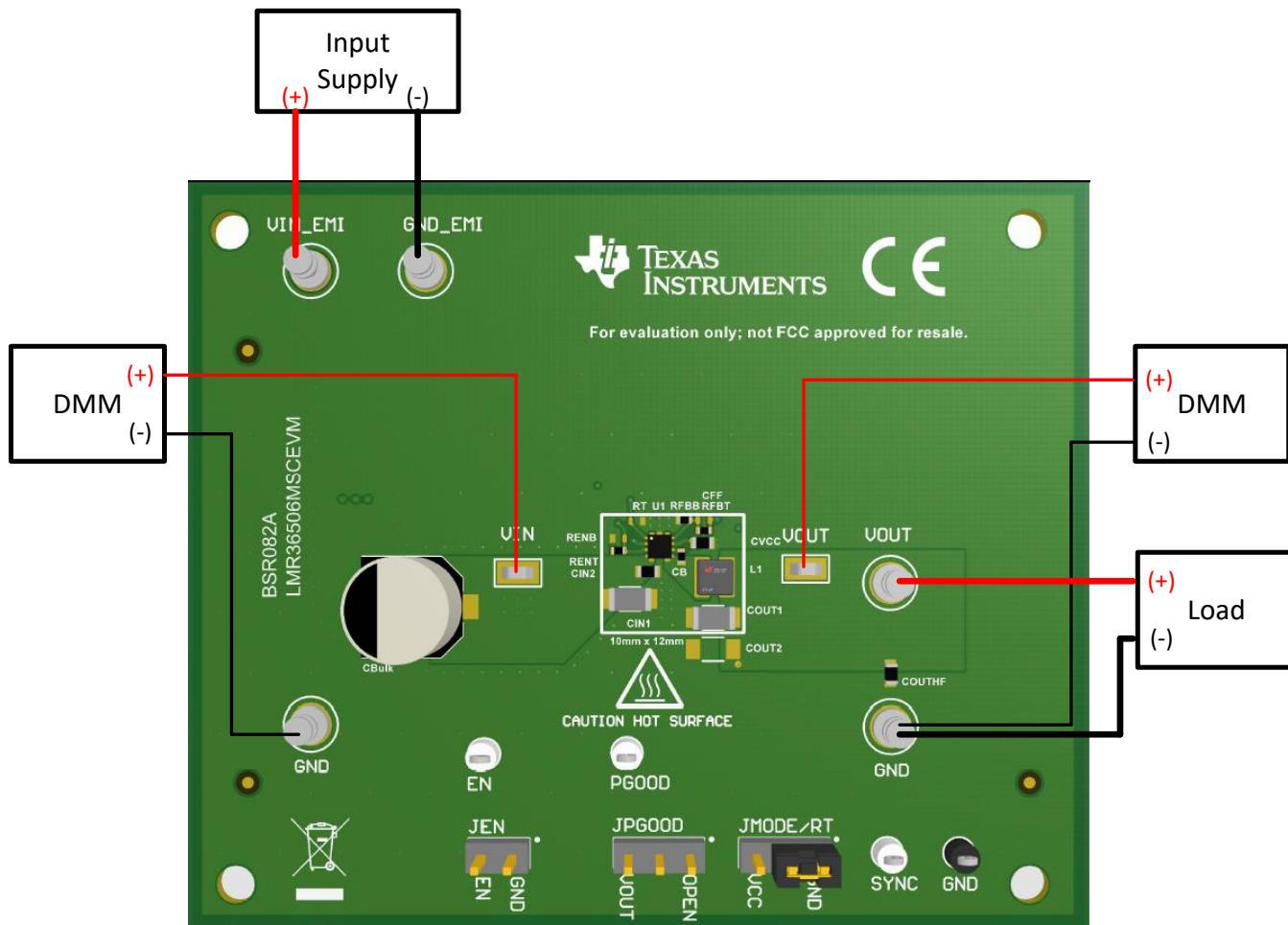


Figure 2. EVM Board Connections

1.2 Jumpers

See [Figure 3](#) for jumper locations.

- **JEN** - This jumper allows the ENABLE input to be connected to GND in order to disable the IC. By default, this jumper is left open since there is a pullup resistor R2 (RENT) to VIN to enable the IC.
- **JPGOOD** - Use this jumper to select how the PGOOD pin can be connected. A jumper can be used to connect pin 2 and 3. In this configuration, the PGOOD pin will be pulled up to VOUT through R9 (RPGOOD) with a value of 100 kΩ. By default, this jumper is left open.
- **JMODE/RT** - Use this jumper to select the mode of operation in a **MODE/SYNC** trim part. Connecting a jumper between pin 1 and 2 cause the IC to operate in PFM (Pulse Frequency Modulation) mode for a higher efficiency at light load. A jumper between pin 2 and pin 3 causes the IC to operate in FPWM mode (Forced Pulse Width Modulation) mode. By default, the jumper is connected between pin 1 and 2.
In an **RT** trim part, connecting this jumper from pin 1 and 2 sets the switching frequency to 2.2 MHz and connecting this jumper from pin 2 and 3 sets the switching frequency to 1 MHz. See the [LMR36506-Q1 3-V-65-V, 0.6-A Synchronous Buck Converter Optimized for Size and Light Load Efficiency](#) data sheet for more information on switching frequency configuration.

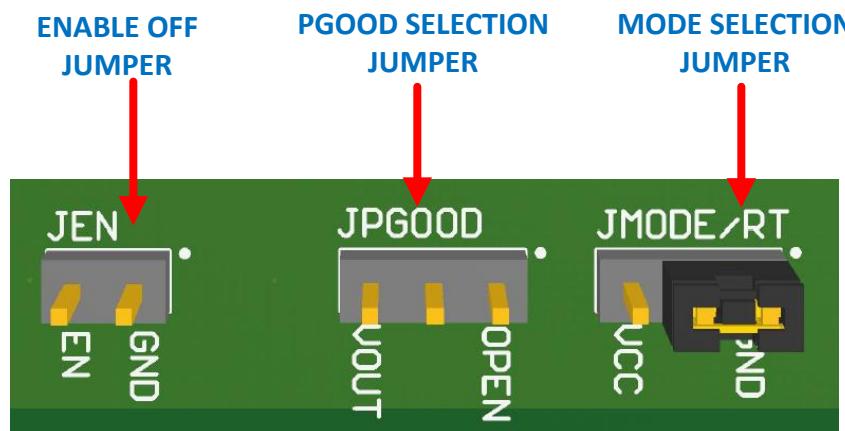


Figure 3. Jumper Locations

2 Operation

2.1 Quick Start

1. Connect the voltage supply between the VIN_EMI and GND_EMI test points.
2. Connect the load between the VOUT and GND test points.
3. Set the supply voltage at an appropriate level between 5.5 V to 65 V. Set the current limit of the supply to an appropriate level.
4. Turn on the power supply. With the default configuration, the EVM powers up and provides $V_{OUT} = 5$ V.
5. Monitor the output voltage. The maximum load current must be 0.6 A with the LMR36506 device.

3 Schematic

VIN = 5.5V - 65V

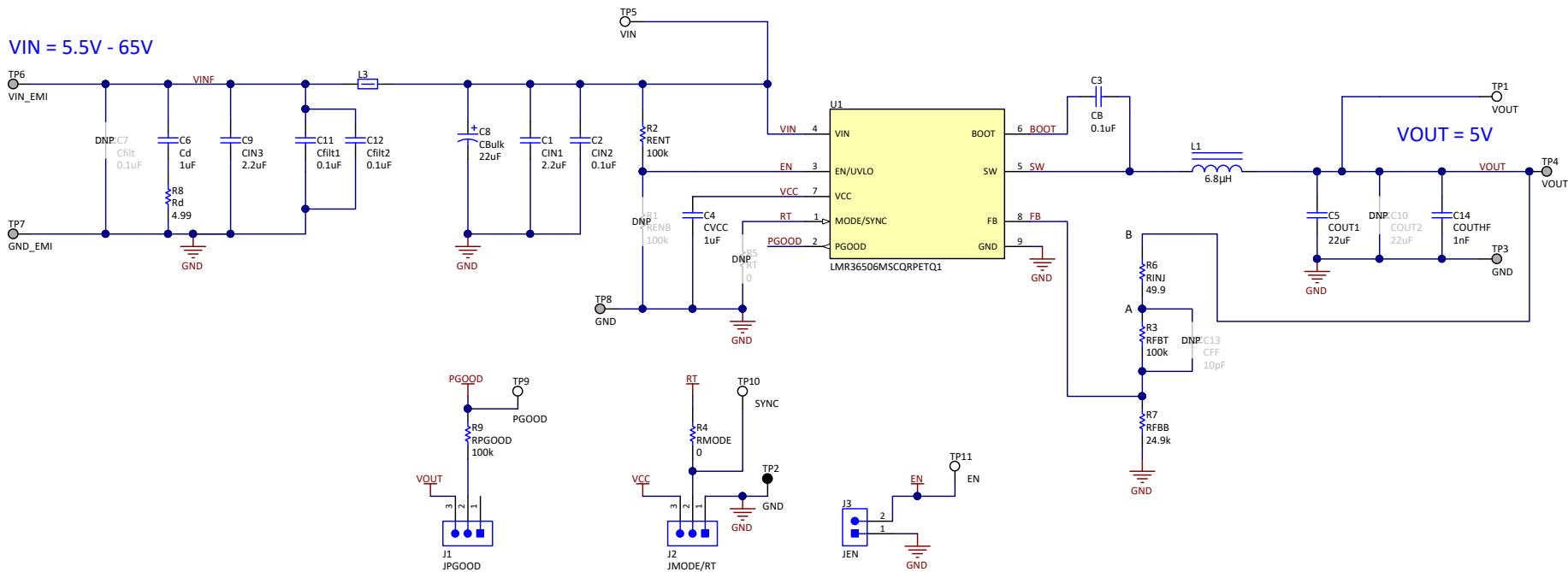


Figure 4. LMR36506MSCEVM Schematic

4 Board Layout

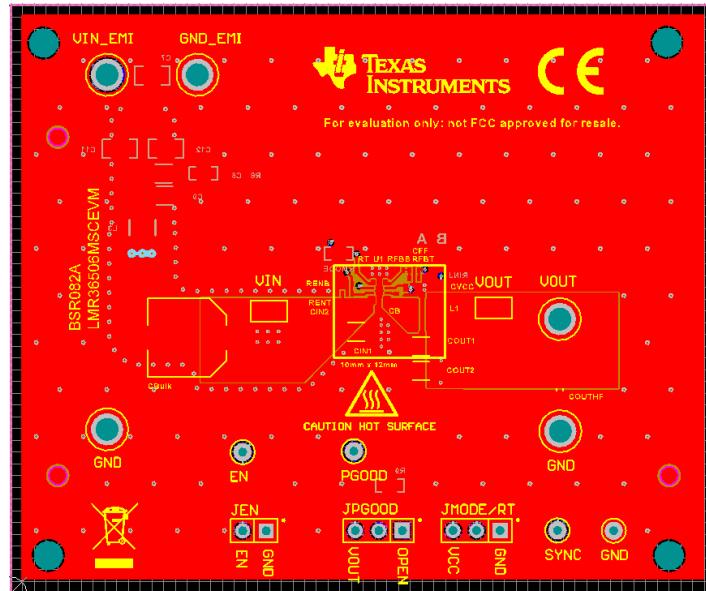


Figure 5. Top View of EVM

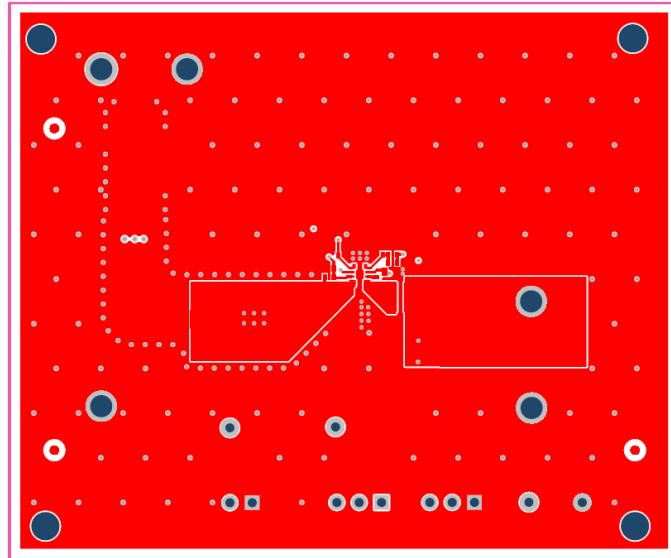


Figure 6. EVM Top Copper Layer

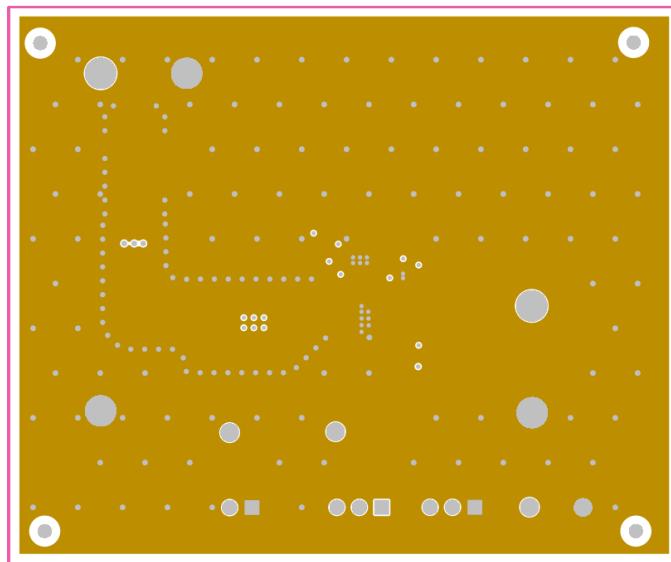


Figure 7. EVM Mid Layer One

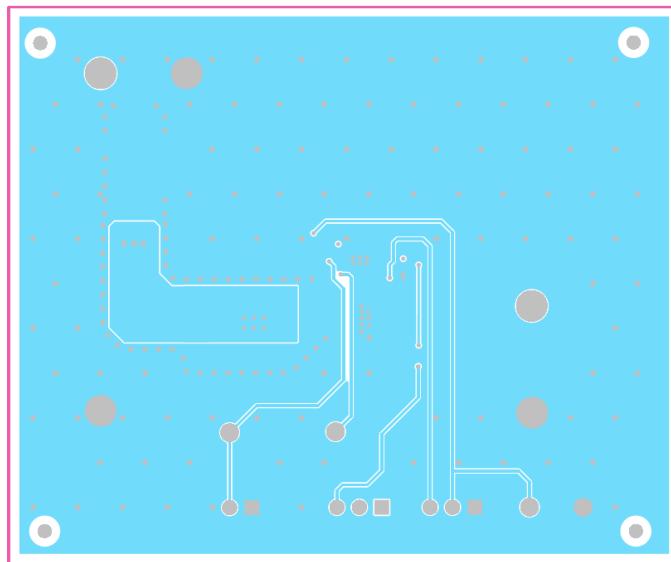


Figure 8. EVM Mid Layer Two

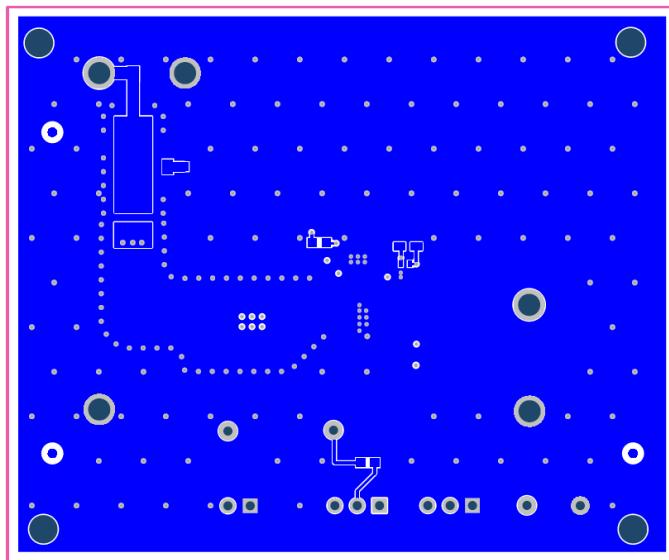


Figure 9. EVM Bottom Copper Layer

5 Bill of Materials

Table 2. Bill of Materials

DESIGNATOR	COMMENT	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
C1, C9	CIN1, CIN3	CAP, CERM, 2.2 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 1206	TDK	CGA5L3X7S2A225K160AB	2
C2	CIN2	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, 0603	MuRata	GRM188R72A104KA35D	1
C3	CB	CAP, CERM, 0.1 uF, 25 V, +/- 20%, X7R, 0402	TDK	C1005X7R1E104M050BB	1
C4	CVCC	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206052	1
C5	COUT1	CAP, CERM, 22 uF, 10 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	MuRata	GCM31CR71A226KE02	1
C6	Cd	CAP, CERM, 1 uF, 100 V, +/- 10%, X7R, 1206	TDK	C3216X7R2A105K160AA	1
C7	Cfilt	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	TDK	CGA4J2X7R2A104K125AA	0
C8	CBulk	CAP, AL, 22 uF, 100 V, +/- 20%, 1.3 ohm, AEC-Q200 Grade 2, SMD	Panasonic	EEE-FK2A220P	1
C10	COUT2	CAP, CERM, 22 uF, 10 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	MuRata	GCM31CR71A226KE02	0
C11, C12	Cfilt1, Cfilt2	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	TDK	CGA4J2X7R2A104K125AA	2
C13	CFF	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	TDK	CGA2B2C0G1H100D050BA	0
C14	COUTHF	CAP, CERM, 1000 pF, 100 V, +/- 10%, X7R, 0603	MuRata	GRM188R72A102KA01D	1
FID1, FID2, FID3, FID4, FID5, FID6	Fiducial	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	0
J1, J2	JPGOOD, JMODE/RT	Header, 100mil, 3x1, Gold, TH	Samtec	HTSW-103-07-G-S	2
J3	JEN	Header, 100mil, 2x1, Gold, TH	Samtec	HTSW-102-07-G-S	1
L1	74438336068	FIXED IND 6.8UH 1.6A 193 MOHM	Wurth Electronics	74438336068	1
L3	FBMH3225HM601NT	Ferrite Bead, 600 ohm @ 100 MHz, 3 A, 1210	Taiyo Yuden	FBMH3225HM601NT	1
R1	RENB	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402100KFKED	0
R2, R3	RENT, RFBT	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402100KFKED	2
R4	RMODE	RES, 0.5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06030000Z0EA	1
R5	RT	RES, 0, 0%, 0.2 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04020000Z0EDHP	0
R6	RINJ	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040249R9FKED	1
R7	RFBB	RES, 24.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040224K9FKED	1
R8	Rd	RES, 4.99, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06034R99FKEA	1
R9	RPGOOD	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100KFKEA	1
SH-J1	SNT-100-BK-G	Shunt, 100mil, Gold plated, Black	Samtec	SNT-100-BK-G	1
TP1, TP5	VOUT, VIN	Test Point, Miniature, SMT	Keystone	5015	2
TP2	GND	Test Point, Miniature, Black, TH	Keystone	5001	1
TP3, TP4, TP6, TP7, TP8	GND, VOUT, VIN_EMI, GND_EMI	Terminal, Turret, TH, Double	Keystone	1502-2	5
TP9, TP10, TP11	PGOOD, SYNC, EN	Test Point, Miniature, White, TH	Keystone	5002	3
U1	LMR36506MSCQR-PETQ1	LMR36503/06-Q1 Wide Input 60-V Synchronous, DC-DC Buck Converter, RPE0009A (VQFN-9)	Texas Instruments	LMR36506MSCQRPETQ1	1

6 Test Results

[Section 6.1](#) details the test results from the LMR36506MSCEVM variant.

6.1 LMR36506MSCEVM Test Results

The LMR36506MSCEVM variant is used for all figures from [Figure 10](#) to [Figure 17](#) variant.

6.1.1 Efficiency and Load Regulation

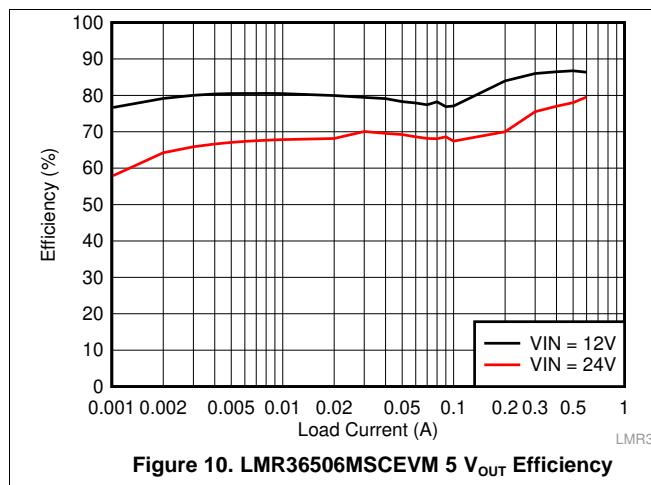


Figure 10. LMR36506MSCEVM 5 V_{OUT} Efficiency

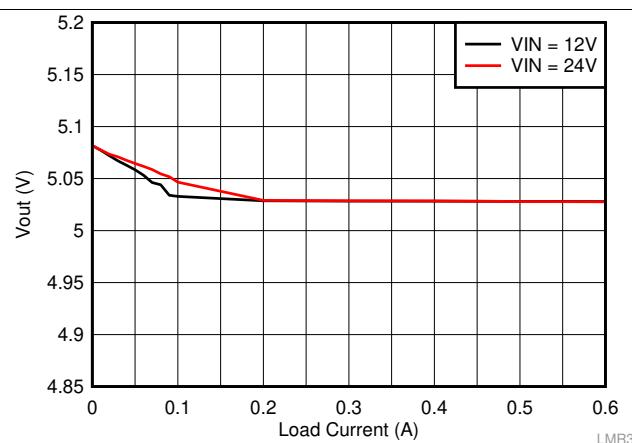


Figure 11. LMR36506MSCEVM 5 V_{OUT} Load Regulation

6.1.2 Load Transients



Figure 12. LMR36506MSCEVM Load Transient
12 V_{IN}, 5 V_{OUT}, I_{OUT} = 0.3 A to 0.6 A, T_R = T_F = 1 μs
CH1 = V_{OUT}, CH4 = I_{OUT}

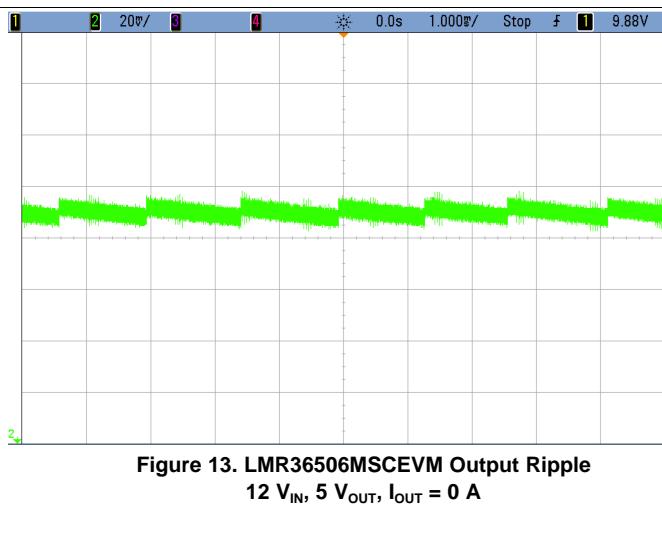
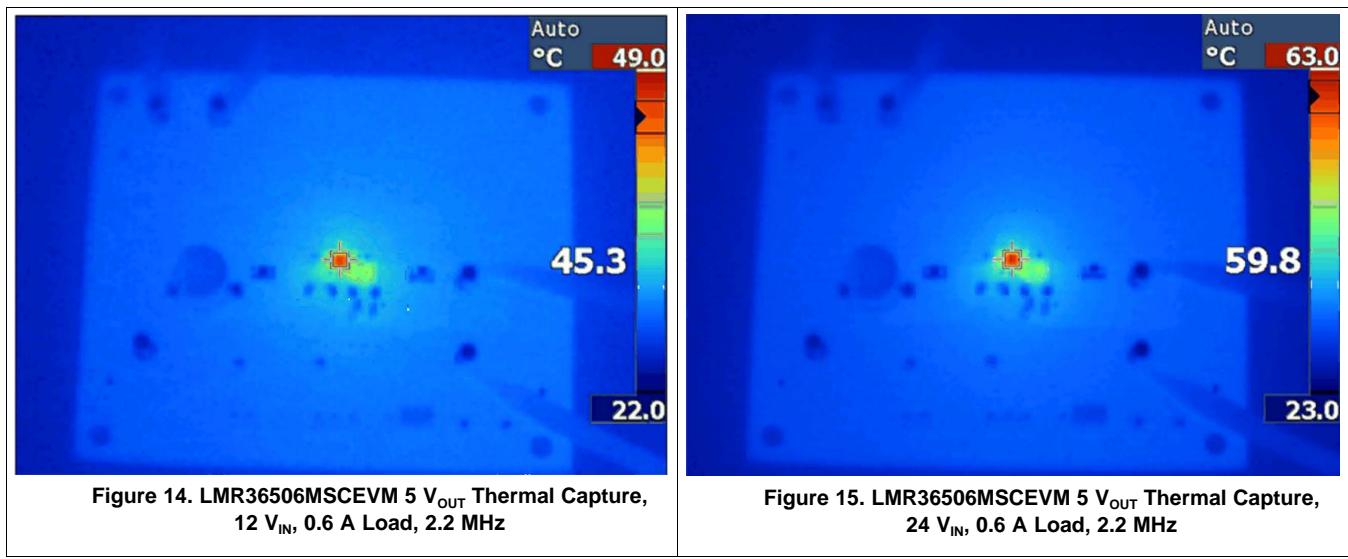
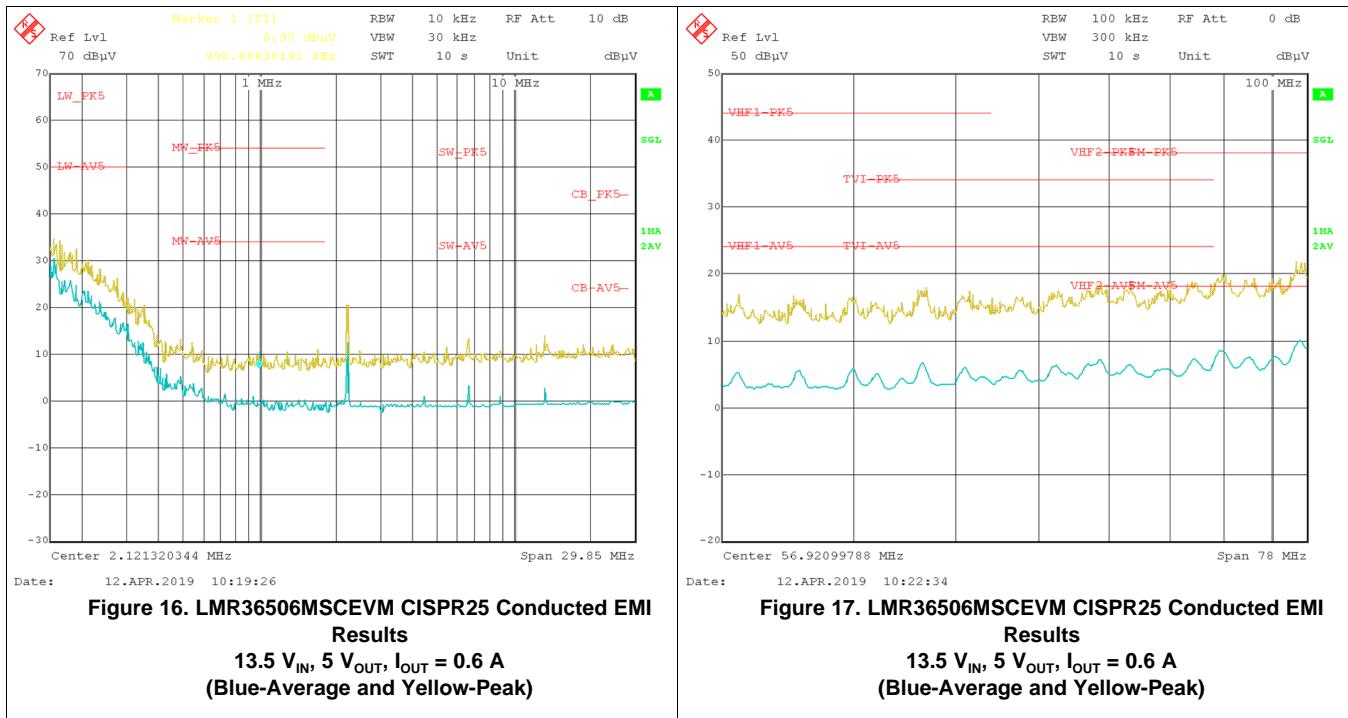


Figure 13. LMR36506MSCEVM Output Ripple
12 V_{IN}, 5 V_{OUT}, I_{OUT} = 0 A

6.1.3 Thermal Picture



6.1.4 Conducted EMI



Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2020) to A Revision	Page
• Updated EVM board image.	1
• Updated EVM board connections image.	3
• Updated LMR36506MSCEVM schematic.	6
• Updated top PCB view image.	7
• Updated top copper layer image.	7
• Updated EVM mid-layer one image.	8
• Updated EVM mid-layer two image.	8
• Updated EVM bottom copper layer image.	9

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