LP87523J-Q1 Technical Reference Manual

This document provides the register bit values for the one-time programmable (OTP) bits of the orderable part number, LP87523JRNFRQ1.

1 Introduction

This technical reference manual can be used as a reference for the LP87523J-Q1 default register bits after OTP memory download. This technical reference manual does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the *LP8752x-Q1 Four-Phase 10-A Buck Converter With Integrated Switches* data sheet.

Table 1 lists the main OTP settings for power rails. Table 2 lists the register bits loaded from OTP memory.

Table 1. Main OTP Settings for Power Rails

Description		Bit Name	Value
Device identification	OTP configuration	OTP_ID	30h
BUCK0, BUCK1 (2-phase operation)	Output voltage	BUCK0_VSET	1150 mV
	Enable, EN pin, or I^2C register	EN_BUCK0, EN_PIN_CTRL0, BUCK0_EN_PIN_SELECT	EN1
	Force PWM	BUCK0_FPWM	Yes
	Force multiphase	BUCK0_FPWM_MP	No
	Peak current limit per phase	N/A	2.5 A
	Maximum load current	N/A	3 A
	Slew rate	N/A	3.8 mV/µs
BUCK2	Output voltage	BUCK2_VSET	1060 mV
	Enable, EN pin, or I^2C register	EN_BUCK2, EN_PIN_CTRL2, BUCK2_EN_PIN_SELECT	EN1
	Force PWM	BUCK2_FPWM	Yes
	Peak current limit	N/A	3 A
	Maximum load current	N/A	2 A
	Slew rate	N/A	3.8 mV/µs
BUCK3	Output voltage	BUCK3_VSET	1350 mV
	Enable, EN pin, or I^2C register	EN_BUCK3, EN_PIN_CTRL3, BUCK3_EN_PIN_SELECT	EN1
	Force PWM	BUCK3_FPWM	Yes
	Peak current limit	N/A	2.5 A
	Maximum load current	N/A	1.5 A
	Slew rate	N/A	3.8 mV/µs
Switching frequency		N/A	2 MHz
I^2C address		N/A	60h

NOTE: The maximum total output capacitance (local + POL) per phase (BUCK0, BUCK1, BUCK2, BUCK3) depends on the slew rate setting. Check the data sheet for the allowed capacitance value.

Copyright © 2019, Texas Instruments Incorporated

2 Register Bits Loaded From OTP Memory

Table 2 lists the register bit values loaded from the OTP memory during device start-up.

Table 2. Summary of Registers Bits

Address	Register Name	Bit	Value
0x01	OTP_REV	OTP_ID[7:0]	30h
0x02	BUCK0_CTRL1	EN_BUCK0	1h
0x02	BUCK0_CTRL1	EN_PIN_CTRL0	1h
0x02	BUCK0_CTRL1	BUCK0_EN_PIN_SELECT[1:0]	0h
0x02	BUCK0_CTRL1	BUCK0_FPWM	1h
0x02	BUCK0_CTRL1	BUCK0_FPWM_MP	0h
0x04	BUCK1_CTRL1	EN_BUCK1	1h
0x04	BUCK1_CTRL1	EN_PIN_CTRL1	1h
0x04	BUCK1_CTRL1	BUCK1_EN_PIN_SELECT[1:0]	0h
0x04	BUCK1_CTRL1	BUCK1_FPWM	1h
0x06	BUCK2_CTRL1	EN_BUCK2	1h
0x06	BUCK2_CTRL1	EN_PIN_CTRL2	1h
0x06	BUCK2_CTRL1	BUCK2_EN_PIN_SELECT[1:0]	0h
0x06	BUCK2_CTRL1	BUCK2_FPWM	1h
0x06	BUCK2_CTRL1	BUCK2_FPWM_MP	0h
0x08	BUCK3_CTRL1	EN_BUCK3	1h
0x08	BUCK3_CTRL1	EN_PIN_CTRL3	1h
0x08	BUCK3_CTRL1	BUCK3_EN_PIN_SELECT[1:0]	0h
0x08	BUCK3_CTRL1	BUCK3_FPWM	1h
0x0A	BUCK0_VOUT	BUCK0_VSET[7:0]	6Bh
0x0C	BUCK1_VOUT	BUCK1_VSET[7:0]	6Bh
0x0E	BUCK2_VOUT	BUCK2_VSET[7:0]	59h
0x10	BUCK3_VOUT	BUCK3_VSET[7:0]	93h
0x12	BUCK0_DELAY	BUCK0_SHUTDOWN_DELAY[3:0]	2h
0x12	BUCK0_DELAY	BUCK0_STARTUP_DELAY[3:0]	3h
0x13	BUCK1_DELAY	BUCK1_SHUTDOWN_DELAY[3:0]	2h
0x13	BUCK1_DELAY	BUCK1_STARTUP_DELAY[3:0]	3h
0x14	BUCK2_DELAY	BUCK2_SHUTDOWN_DELAY[3:0]	2h
0x14	BUCK2_DELAY	BUCK2_STARTUP_DELAY[3:0]	4h
0x15	BUCK3_DELAY	BUCK3_SHUTDOWN_DELAY[3:0]	4h
0x15	BUCK3_DELAY	BUCK3_STARTUP_DELAY[3:0]	2h
0x16	GPIO2_DELAY	GPIO2_SHUTDOWN_DELAY[3:0]	1h
0x16	GPIO2_DELAY	GPIO2_STARTUP_DELAY[3:0]	6h
0x17	GPIO3_DELAY	GPIO3_SHUTDOWN_DELAY[3:0]	0h
0x17	GPIO3_DELAY	GPIO3_STARTUP_DELAY[3:0]	Fh
0x19	CONFIG	DOUBLE_DELAY	0h
0x19	CONFIG	CLKIN_PD	1h
0x19	CONFIG	EN4_PD	0h
0x19	CONFIG	EN3_PD	1h
0x19	CONFIG	TDIE_WARN_LEVEL	1h
0x19	CONFIG	EN2_PD	0h
0x19	CONFIG	EN1_PD	0h
0x21	TOP_MASK1	GPIO_MASK	1h
0x21	TOP_MASK1	SYNC_CLK_MASK	1h
0x21	TOP_MASK1	TDIE_WARN_MASK	0h
0x21	TOP_MASK1	I_LOAD_READY_MASK	1h
0x22	TOP_MASK2	RESET_REG_MASK	1h
0x23	BUCK_0_1_MASK	BUCK1_PG_MASK	1h

Copyright © 2019, Texas Instruments Incorporated

Table 2. Summary of Registers Bits (continued)

Address	Register Name	Bit	Value
0x23	BUCK_0_1_MASK	BUCK1_ILIM_MASK	1h
0x23	BUCK_0_1_MASK	BUCK0_PG_MASK	1h
0x23	BUCK_0_1_MASK	BUCK0_ILIM_MASK	1h
0x24	BUCK_2_3_MASK	BUCK3_PG_MASK	1h
0x24	BUCK_2_3_MASK	BUCK3_ILIM_MASK	1h
0x24	BUCK_2_3_MASK	BUCK2_PG_MASK	1h
0x24	BUCK_2_3_MASK	BUCK2_ILIM_MASK	1h
0x28	PGOOD_CTRL1	PG3_SEL[1:0]	1h
0x28	PGOOD_CTRL1	PG2_SEL[1:0]	1h
0x28	PGOOD_CTRL1	PG1_SEL[1:0]	1h
0x28	PGOOD_CTRL1	PG0_SEL[1:0]	1h
0x29	PGOOD_CTRL2	HALF_DELAY	1h
0x29	PGOOD_CTRL2	EN_PG0_NINT	0h
0x29	PGOOD_CTRL2	PGOOD_SET_DELAY	0h
0x29	PGOOD_CTRL2	EN_PGFLT_STAT	0h
0x29	PGOOD_CTRL2	PGOOD_WINDOW	1h
0x29	PGOOD_CTRL2	PGOOD_OD	1h
0x29	PGOOD_CTRL2	PGOOD_POL	0h
0x2B	PLL_CTRL	PLL_MODE[1:0]	0h
0x2B	PLL_CTRL	EXT_CLK_FREQ[4:0]	1h
0x2C	PIN_FUNCTION	EN_SPREAD_SPEC	1h
0x2C	PIN_FUNCTION	EN_PIN_CTRL_GPIO3	1h
0x2C	PIN_FUNCTION	EN_PIN_SELECT_GPIO3	0h
0x2C	PIN_FUNCTION	EN_PIN_CTRL_GPIO2	1h
0x2C	PIN_FUNCTION	EN_PIN_SELECT_GPIO2	0h
0x2C	PIN_FUNCTION	GPIO3_SEL	1h
0x2C	PIN_FUNCTION	GPIO2_SEL	1h
0x2C	PIN_FUNCTION	GPIO1_SEL	0h
0x2D	GPIO_CONFIG	GPIO3_OD	1h
0x2D	GPIO_CONFIG	GPIO2_OD	0h
0x2D	GPIO_CONFIG	GPIO1_OD	1h
0x2D	GPIO_CONFIG	GPIO3_DIR	1h
0x2D	GPIO_CONFIG	GPIO2_DIR	1h
0x2D	GPIO_CONFIG	GPIO1_DIR	1h
0x2F	GPIO_OUT	GPIO3_OUT	1h
0x2F	GPIO_OUT	GPIO2_OUT	1h

Copyright © 2019, Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated