User's Guide

LP8752x-Q1 Configuration Guide

ABSTRACT

This configuration guide is designed to help one understand how to use a micro-controller unit (MCU) to configure an LP8752x-Q1 PMIC. Instead of requiring a new one time programmable configuration (OTP) for each design, a specific LP8752x-Q1 variants described in this configuration guide can be configured at startup through inter-integrated circuit (I2C) bus to meet design requirements.

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Trademarks

1 Introduction

The LP8752x-Q1 contains four step-down DC/DC converter cores, which are configured as 4-phase single output, 3-phase and single phase outputs, one dual phase and two single phase outputs, four single phase outputs or two dual phase outputs. The device is controlled by an I2C-compatible serial interface and by enable signals. Typically the settings such as output voltages, startup/shutdown sequences etc. for the LP8752x-Q1 PMIC are programmed during IC manufacturing by a one time programmable memory (OTP). However, with an MCU this device can also be configured after each start up to fit different design requirements. Default values for the configuration registers (volatile memory) are loaded from the OTP during device power-up, and through I2C bus the registers can be updated to desired values.

This document explains how to set up an LP8752x-Q1 PMIC to be configured at start up so that it can be used in different designs, without the need for a new OTP. Specific OTP versions described in this document have been designed to allow the PMIC to be easily configured at each power-up. For device specifications and detailed functionality, see the device-specific data sheet.

2 Setup

There are a few important connections to make sure the LP8752x-Q1 is configured correctly, each of which are described in this section. A good example of how to connect an MCU to the LP8752x-Q1 PMIC is shown in Figure 2-1.

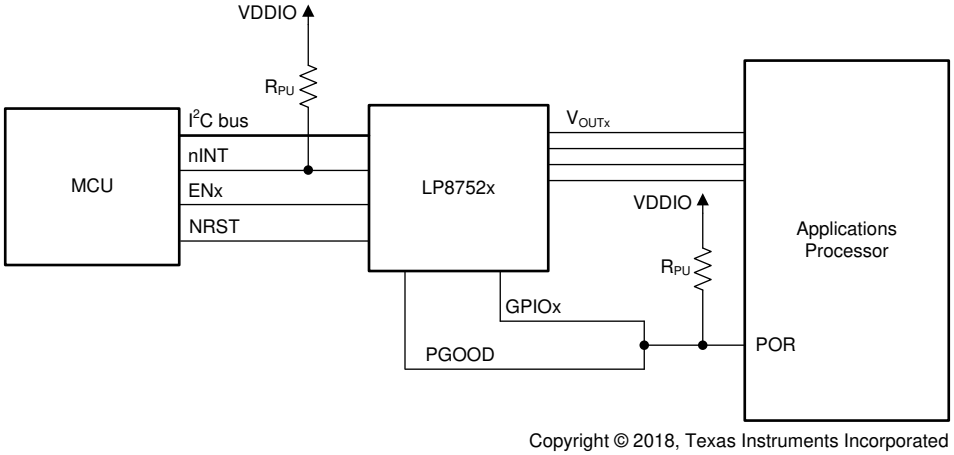

Figure 2-1. Typical MCU Connection to LP8752x-Q1 for Start-Up Configuration

2.1 SCL/SDA Pins

The SCL and SDA lines (pins 5 & 6, respectively) are used to communicate between the MCU and the LP8752x-Q1 PMIC using an I2C compatible Interface. The I2C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed on the line and remain HIGH even when the bus is idle. The LP8752x-Q1 supports standard mode (100kHz), fast mode (400kHz), fast mode plus (1MHz), and high-speed mode (3.4MHz). For all I2C protocol details,see the device-specific data sheet.

2.2 NRST Pin

The NRST pin (pin 20) is used to reset the device logic/enable device internal logic and IO interface. When the NRST voltage is below threshold level all power switches, references, controls, and bias circuitry of the LP8752x-Q1 device are turned off. When NRST is set to high level (and VANA is above UVLO level) this initiates power-on-reset (POR), OTP reading and enables the system I/O interface. The I2C host must allow at least 1.2ms before writing or reading data to the LP8752x-Q1. Device enters STANDBY-mode after internal startup sequence. The host can change the default register setting by I2C if needed. The regulator(s) can be enabled/disabled by ENx pin(s) or by I2C interface.

2.3 ENx (GPIOx) Pins

Enable pins EN1 (GPIO1), EN2 (GPIO2), EN3 (GPIO3) (pins 7, 15, 2) are I2C configurable general-purpose input/output (GPIO) pins. The direction, function, and output type (open-drain or push-pull) are programmable for the GPIOs. When configured as EN pin, they can be used to start the buck converter startup sequence based on programmed timing. Shutdown times can be programmed as well. It is recommended that the ENx pins be driven low until the device is configured to the desired settings. When programmed as enable signals, drive these pins low to disable or high to enable the associated buck converters.

2.4 nINT

The nINT pin (pin 19) is an open-drain, active low output from the LP8752x-Q1 PMIC. Connect this pin to an external pullup resistor. If RESET_REG_MASK bit is unmasked, then an interrupt is generated on this pin whenever the RESET_REG_INT bit is set high. The RESET_REG_INT bit is set high when either the VANA supply voltage has decreased below the undervoltage threshold level or the host has requested a reset using the SW_RESET bit in the RESET register or device is reset by NRST. By monitoring the nINT pin, the MCU knows when the PMIC registers are reset to the default values determined by the OTP, and takes the necessary actions to make sure that the PMIC is configured as needed.

After a power-on reset, the LP8752x-Q1 PMIC requires a delay of 1.2ms before there can be any communication through the I2C interface. When the RESET_REG_MASK bit is unmasked, this required delay can be monitored through the nINT pin. After a power-on reset, the nINT pin is driven high while the registers are reset and the OTP is read to set the registers to their initial values. After 1.2ms, the nINT pin is driven low, signaling that the registers have been reset and can be configured to fit the design requirements.

Else, when RESET_REG_MASK bit is masked, nINT does not have any reaction to a power-on-reset.

Note

To monitor the nINT pin correctly, the MCU must clear all interrupts before enabling all of the outputs on the LP8752x-Q1 PMIC. Write a 1 to the RESET_REG bit in the INT_TOP2 register to clear this interrupt. If all interrupts are not cleared before enabling the LP8752x-Q1 PMIC outputs, then there is no change on the nINT pin when an interrupt is generated and the MCU is not able to detect a register reset. Make sure that the RESET_REG_MASK bit in the TOP_MASK2 register is unmasked so that an interrupt can be generated on nINT.

3 Configuration

This section describes the default OTP settings, and how to configure these settings to meet design requirements.

3.1 Configuration Sequence

Using the setup described in Section 2 allows the MCU to easily configure the LP8752x-Q1 PMIC after a power-on reset, or after any event causing a register reset. To make sure that this is done correctly, follow the sequence described in this section. The following list shows the actions to take to make sure the LP8752x-Q1 PMIC is configured correctly. These actions must be taken after a power-on reset or a register reset.

1. Power on PMIC. (V_{VANA} > $VANA_{UVLO}$)
2. Set NRST high
3. Wait for 1.2ms (or for nINT line to be set low, if RESET_REG_MASK = 0)
4. Set new configuration using I2C communication in recommended order. See Section 3.3.
   a. Voltage settings
   b. Regulator settings
   c. GPIO settings
   d. Clock sync functions
   e. PGOOD settings
   f. Interrupt settings
   g. Startup / shutdown settings
   h. Set ENx pin control bits
   i. Set EN_BUCKx bits
5. Clear Interrupts.
6. Set ENx pin high to startup sequence.

Upon a power-on reset, waiting for the nINT line to be set low makes sure that the PMIC is ready for I2C communication. Waiting for the nINT line to be set low at any other time allows the PMIC to know when a register reset has occurred. The timing diagrams in Figure 3-1, Figure 3-2, and Figure 3-3 show how to configure the LP8752x-Q1 PMIC after a power-on reset or register reset has occurred. Once all of the I2C writes are finished, the MCU clears the interrupt and enables the PMIC. The MCU can do this by writing a 1 to the RESET_REG bit to clear the interrupt and by pulling the ENx pin high to turn on the PMIC outputs.

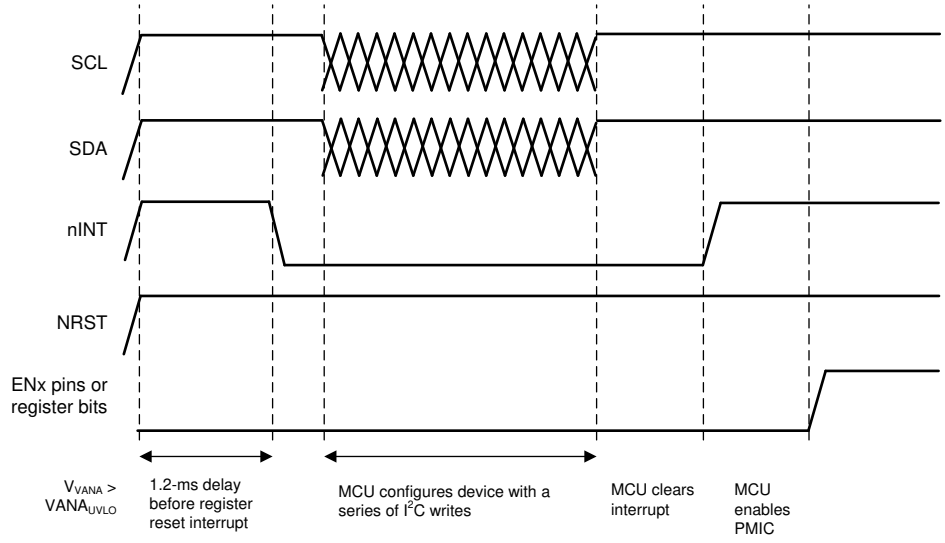

Figure 3-1. Configuration Sequence During Startup (RESET_REG_MASK = 0)

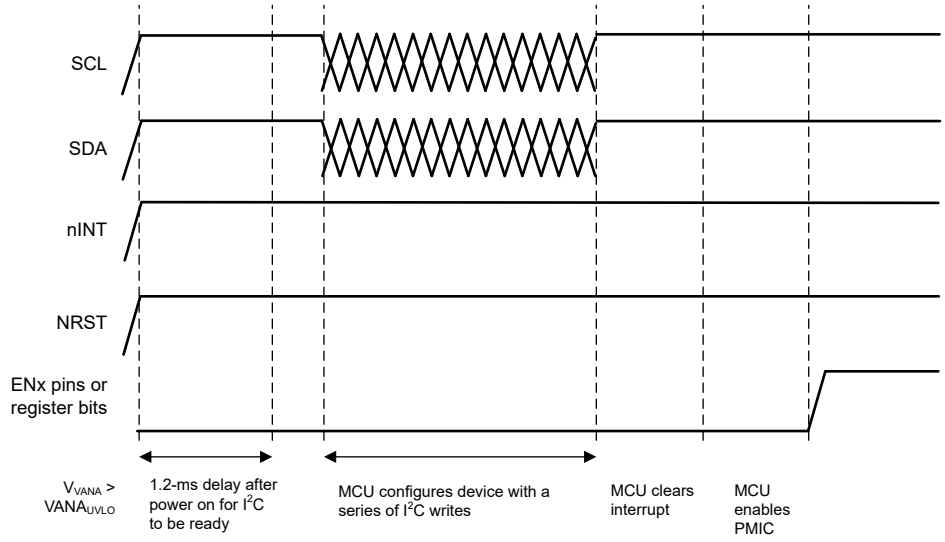

Figure 3-2. Configuration Sequence During Startup (RESET_REG_MASK = 1)

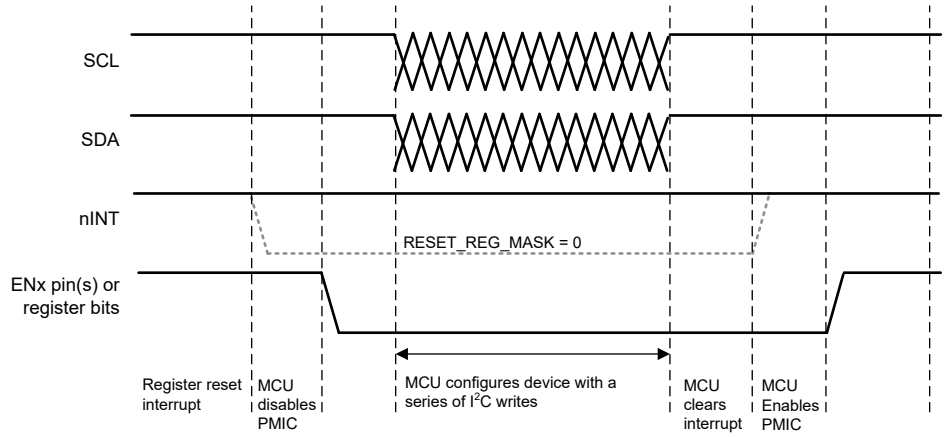

Figure 3-3. Configuration Sequence During Reset

3.2 Default OTP Configurations

All LP8752x-Q1 PMIC resource settings are stored in the form of volatile registers. These settings define buck output voltages, GPIO functionality, and power-up and power-down sequences. For a full list of the setting registers, see the device-specific data sheet. A different OTP is needed for each possible phase configuration. Phase configuration is not I2C configurable.

Each device has predefined values stored in OTP which control the default configuration of the device. For the default OTP-programmed values for each device, see the device-specific Technical Reference Manual (TRM). The tables in this section list the configurability of each bit.

Table 3-1 shows device settings for BUCK0, BUCK1, BUCK2, BUCK3. Maximum allowed slew-rate for BUCKx depends on the output capacitance. For output capacitance boundary conditions, see the device-specific data sheet.

Table 3-1. BUCKx OTP Settings

	Description	Bit Name	Configurable
General settings	Buck phase configuration (for example, four single phase denoted as 1+1+1+1, four phase single output denoted as 4 ph). For multiphase configuration master buck defines the output voltage, startup/shutdown times, and so forth. For more information, see the device-specific data sheet.	-	No Refer to part number: LP87521x - 4 ph LP87522x - 3+1 LP87523x - 2+1+1 LP87524x - 1+1+1+1 LP87525x - 2+2
	Switching frequency	-	No
	Spread spectrum	EN_SPREAD_SPEC	Yes
	Startup and shutdown delay range, 0...4.8ms / 0... 10ms / 0...15ms / 0...30ms	DOUBLE_DELAY, HALF_DELAY	Yes
BUCK settings	Output voltage	BUCKx_VSET	Yes
	Enable, ENx-pin or I2C register	EN_PIN_CTRLx	Yes
	Control for BUCK0	EN_BUCKx	Yes
	Force PWM mode or auto mode	BUCKx_FPWM	Yes
	Force multiphase mode or auto mode	BUCKx_FPWM_MP	Yes
	Peak current limit	ILIMx	No
	Slew rate	SLEW_RATEx	Yes
	Startup Delay	BUCKx_STARTUP_DELAY	Yes
	Shutdown Delay	BUCKx_SHUTDOWN_DELAY	Yes

Table 3-2 lists the device settings for GPIOs.

Table 3-2. EN, CLKIN and GPIO Pin Settings

	Description	Bit Name	Configurable
EN1 (GPIO1) pin	EN1 (GPIO1) pin pulldown resistor enable or disable	EN1_PD	Yes
EN2 (GPIO2) pin	EN2 (GPIO2) pin pulldown resistor enable or disable	EN2_PD	Yes
EN3 (GPIO3) pin	EN3 (GPIO3) pin pulldown resistor enable or disable	EN3_PD	Yes
CLKIN pin	CLKIN pin pull-down resistor enable or disable	CLKIN_PD	Yes
	Frequency of external clock when connected to CLKIN	EXT_CLK_FREQ	Yes
	Mode for the internal PLL. When PLL disabled, internal RC OSC is used	PLL_MODE	Yes
EN1 (GPIO) control	Enable or GPIO	GPIO1_SEL	Yes
	Input or output in GPIO mode	GPIO1_DIR	Yes
	Output type open drain or push-pull	GPIO1_OD	Yes
	Default state of GPIO output	GPIO1_OUT	Yes
EN2 (GPIO) control	Enable or GPIO	GPIO2_SEL	Yes
	Input or output in GPIO mode	GPIO2_DIR	Yes
	Output type open drain or push-pull	GPIO2_OD	Yes
	Default state of GPIO output	GPIO2_OUT	Yes
	Pin control of GPIO, EN2 or EN3	EN_PIN_CTRL_GPIO2, EN_PIN_SELECT_GPIO2	Yes
	Startup Delay	GPIO2_ STARTUP_DELAY	Yes
	Shutdown Delay	GPIO2_ SHUTDOWN_DELAY	Yes

Table 3-2. EN, CLKIN and GPIO Pin Settings (continued)

	Description	Bit Name	Configurable
EN3 (GPIO) control	Enable or GPIO	GPIO3_SEL	Yes
	Input or output in GPIO mode	GPIO3_DIR	Yes
	Output type open drain or push-pull	GPIO3_OD	Yes
	Default state of GPIO output	GPIO3_OUT	Yes
	Pin control of GPIO, EN2 or EN3	EN_PIN_CTRL_GPIO3, EN_PIN_SELECT_GPIO3	Yes
	Startup Delay	GPIO3_ STARTUP_ DELAY	Yes
	Shutdown Delay	GPIO3_ SHUTDOWN_ DELAY	Yes

Table 3-3 shows device settings for PGOOD.

Table 3-3. PGOOD OTP Settings

	Description	Bit Name	Configurable
Signals monitored by PGOOD	BUCKx output voltage / voltage and current (master bucks)	PGx_SEL	Yes
PGOOD mode selections	PGOOD thresholds for BUCKx (Undervoltage / Window (undervoltage and overvoltage))	PGOOD_WINDOW	Yes
	PGOOD valid debounce time	PGOOD_SET_DELAY	Yes
	PGOOD signal mode (status / latched until fault source read)	EN_PGFLT_STAT	Yes
	PGOOD output mode (push-pull or open drain)	PGOOD_OD	Yes
	PGOOD polarity (active high / active low)	PGOOD_POL	Yes

Table 3-4 lists the device settings for thermal warning. For interrupt settings, see Table 3-6.

Table 3-4. Protections OTP Settings

	Description	Bit Name	Configurable
Protections	Thermal warning level (125°C or 137°C)	TDIE_WARN_LEVEL	Yes
	Input over-voltage protection	-	No

Table 3-5 shows device settings for I2C and OTP revision ID values.

Table 3-5. Device Identification and I2C Settings

	Description	Bit Name	Configurable
I2C slave ID (7-bit)	Device I2C address	-	No Refer to TRM for default value.

Table 3-6 lists device settings for interrupts. When interrupt from an event is unmasked, an interrupt is generated to nINT pin.

Table 3-6. Interrupt Mask Settings

	Interrupt event	Bit Name	Configurable
General	Sync clock appears or disappears	SYNC_CLK_MASK	Yes
	Thermal warning	TDIE_WARN_MASK	Yes
	Load measurement ready	I_LOAD_READY_MASK	Yes
	Register reset	RESET_REG_MASK	Yes
BUCK0	Buck0 PGOOD has reached threshold level	BUCK0_PG_MASK	Yes
	Buck0 current limit triggered	BUCK0_ILIM_MASK	Yes
BUCK1	Buck1 PGOOD has reached threshold level	BUCK1_PG_MASK	Yes
	Buck1 current limit triggered	BUCK1_ILIM_MASK	Yes
BUCK2	Buck2 PGOOD has reached threshold level	BUCK2_PG_MASK	Yes
	Buck2 current limit triggered	BUCK2_ILIM_MASK	Yes

Table 3-6. Interrupt Mask Settings (continued)

	Interrupt event	Bit Name	Configurable
BUCK3	Buck3 PGOOD has reached threshold level	BUCK3_PG_MASK	Yes
	Buck3 current limit triggered	BUCK3_ILIM_MASK	Yes

3.3 Recommended Order of Configuring Registers Through I2C

This section goes through the main settings that can be configured to fit a specific design, in the recommended order. for all of these settings and their corresponding bits/registers, see the device-specific data sheet and Section 3.2.

3.3.1 Voltage Settings

The default voltage settings for the bucks are OTP-dependent. Refer to the device TRM for the default values. Change the default voltage settings by writing to the respective fields listed below. To see how the values of these registers correspond to different voltages, see the device-specific data sheet. Depending on phase configuration, only master buck voltage needs to be set.

- BUCK0_VSET field in BUCK0_VOUT register
- BUCK1_VSET field in BUCK1_VOUT register
- BUCK2_VSET field in BUCK2_VOUT register
- BUCK3_VSET field in BUCK3_VOUT register

3.3.2 Other Regulator Settings

Each buck has 2 CTRL registers that can be used to set slew rates as well as enable their output discharge resistors or set auto/forced PWM mode and auto/forced multiphase mode. Included in these registers is an EN_PIN_CTRLx, EN_BUCKx, and BUCKx_EN_PIN_SELECT[1:0] bits for each regulator. It is recommended to set the EN_PIN_CTRLx, EN_BUCKx, and BUCKx_EN_PIN_SELECT[1:0] bits last to avoid any regulators turning on before configuration is complete. These regulator setting fields are summarized in Figure 2-1. For a full description of all registers and their settings, see the device-specific data sheet.

Table 3-7. Regulator Control Settings Registers

Regulator	Register	Fields that are expected to already be configured	Fields to configure when the PMIC is ready to be powered up (Section 3.3.8)
BUCK0	BUCK0_CTRL_1	EN_ROOF_FLOOR0, EN_RDIS0, BUCK0_FPWM, BUCK0_FPWM_MP	BUCK0_EN_PIN _CTRL, EN_BUCK0, BUCK_0_EN_PIN_SELECT[1:0]
	BUCK0_CTRL_2	SLEW_RATE0[1:0]	
BUCK1	BUCK1_CTRL_1	EN_ROOF_FLOOR1, EN_RDIS1, BUCK1_FPWM	BUCK1_EN_PIN _CTRL, EN_BUCK1, BUCK_1_EN_PIN_SELECT[1:0]
	BUCK1_CTRL_2	SLEW_RATE1[1:0]	
BUCK2	BUCK2_CTRL_1	EN_ROOF_FLOOR2, EN_RDIS2, BUCK2_FPWM, BUCK2_FPWM_MP	BUCK2_EN_PIN _CTRL, EN_BUCK2, BUCK_2_EN_PIN_SELECT[1:0]
	BUCK2_CTRL_2	SLEW_RATE2[1:0]	
BUCK3	BUCK3_CTRL_1	EN_ROOF_FLOOR3, EN_RDIS3, BUCK3_FPWM	BUCK3_EN_PIN _CTRL, EN_BUCK3, BUCK_3_EN_PIN_SELECT[1:0]
	BUCK3_CTRL_2	SLEW_RATE3[1:0]	

3.3.3 GPO Settings

The LP8752x-Q1 device supports up to three GPIO signals. The GPIO signals are multiplexed with enable signals. The selection between enable and GPIO function is set with GPIOx_SEL bits in PIN_FUNCTION register. When the pin is selected for GPIO function, additional bits defines how the GPIO operates:

- GPIOx_DIR defines the direction of the GPIO, input or output (GPIO_CONFIG register)
- GPIOx_OD defines the type of the output when the GPIO is set to output, either push-pull with VANA level or open-drain (GPIO_CONFIG register)

When the GPIOx is defined as output, the logic level of the pin is set by GPIOx_OUT bit (in GPIO_OUT register). When the GPIOx is defined as input, read the logic level of the pin from the GPIOx_IN bit (in GPIO_IN register). The control of the GPIOs configured to outputs can be included to start-up and shutdown sequences. The GPIO control for a sequence with ENx signal is selected by EN_PIN_CTRL_GPIOx and EN_PIN_SELECT_GPIOx bits (in PIN_FUNCTION register). The delays during start-up and shutdown are set by GPIOx_STARTUP_DELAY[3:0] and GPIOx_SHUTDOWN_DELAY[3:0] bits (in GPIOx_DELAY register) in the same way as control of the regulators. The GPIOx signals have a selectable pull-down resistor. The pull-down resistors are selected by ENx_PD bits (in CONFIG register). For more information on each of the fields in the GPIO registers, see the device-specific data sheet.

3.3.4 Clock Sync Functions

The LP8752x-Q1 device contains a CLKIN input to synchronize switching clock of the buck regulator with the external clock. Depending on the PLL_MODE[1:0] bits (in PLL_CTRL register) and the external clock availability, the external clock is selected and interrupt is generated. Optionally, mask this interrupt with the SYNC_CLK_MASK bit in TOP_MASK1 register. The nominal frequency of the external input clock is set by EXT_CLK_FREQ[4:0] bits (in PLL_CTRL register) and ranges from 1MHz to 24MHz with 1MHz steps. The external clock must be inside accuracy limits (–30%/+10%) for valid clock detection. For more information on this function, see the device-specific data sheet.

3.3.5 PGOOD Settings

The PGOOD output can be used to monitor several signals and has multiple settings to configure as listed below.

- Monitoring of regulator output voltage (Individual regulators are selectable)
- Undervoltage only or undervoltage and overvoltage monitoring
- Monitoring output current
- Debounce time setting
- Push-pull or open drain output
- Gated or continuous operating mode
- Adjustable polarity

For more information on the PGOOD signal functionality, see the device-specific data sheet.

3.3.6 Interrupt Settings

The LP8752x-Q1 PMIC has many interrupt signals used to indicate different events including regulator overcurrent events, regulator PGOOD events, regulator short-circuit events, and clock events. The registers containing all of these interrupts are listed as follows:

- INT_TOP1 register
- INT_TOP2 register
- INT_BUCK_0_1 register
- INT_BUCK_2_3 register

These interrupts can be masked or unmasked using the registers below. For the default mask settings, see the device-specific TRM. When RESET_REG_INT bit is unmasked, this allows the MCU to know when the PMIC registers are reset to the values determined by the OTP, so the MCU takes the necessary actions to verify that the PMIC is configured as needed. Unmask other interrupts as needed. If multiple interrupts are unmasked, read the interrupt registers to determine the specific cause when an interrupt is generated on the nINT line.

- TOP_MASK1 register
- TOP_MASK2 register
- BUCK_0_1_MASK register
- BUCK_2_3_MASK register

3.3.7 Startup and Shutdown Sequence

Each of the bucks and GPOs on the LP8752x-Q1 can be set to startup and shutdown in a specific sequence. To configure the desired sequence the STARTUP_DELAY and SHUTDOWN_DELAY fields for each output need to be set to a value between 0x0 and 0xF. The delay time that this value corresponds to depends on the DOUBLE_DELAY bit and the HALF_DELAY bit located in the CONFIG register. A value of 0 on both of these bits allow a delay ranging from 0ms to 15ms with 1ms steps. Figure 3-4 shows an example of how these delays can be used to configure a startup and shutdown sequence, in this case with EN1 signal. For a full description of all registers and their settings, see the device-specific data sheet.

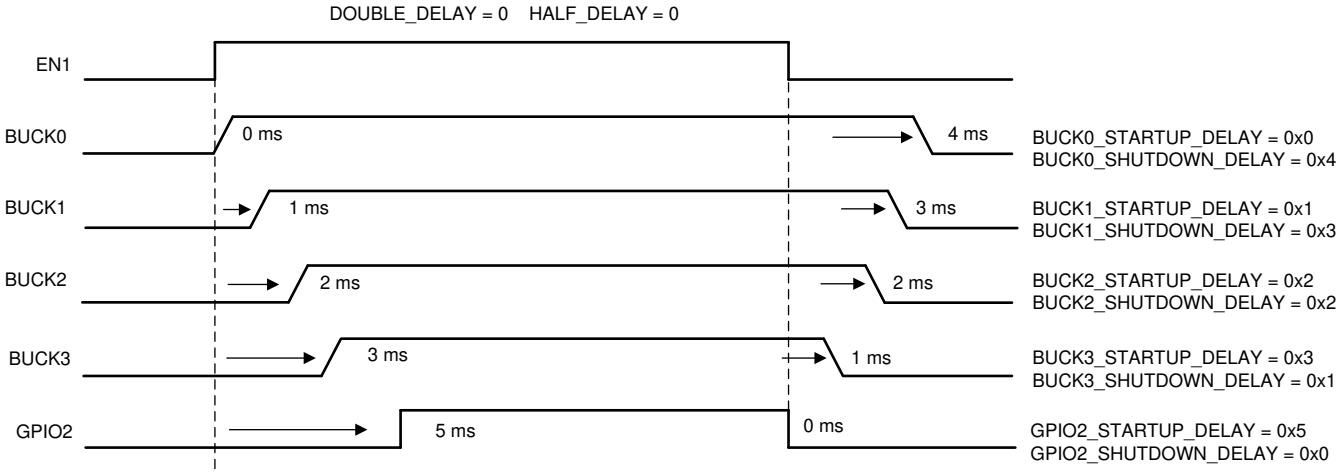

Figure 3-4. Startup and Shutdown Sequence Timing Diagram

3.3.8 Set ENx Pin Control Bits

Each output can be controlled by either I2C communication, or a combination of I2C communication and an ENx pin, as determined by each output's EN_PIN_CTRLx and BUCKx_EN_PIN_SELECT[1:0] bits. When controlled via I2C (EN_PIN_CTRLx = 0), the selected output is turned on using the corresponding EN_BUCKx bits. Note that the sequencing delay settings are not effective in this case. When controlled using a combination of I2C and the ENx pin (EN_PIN_CTRLx = 1), both the ENx pin (set with BUCKx_EN_PIN_SELECT[1:0]) and the corresponding EN_BUCKx bit must be set high to turn on an output.

Once all of the other device settings have been set, set the EN_PIN_CTRLx bit high for each output that needs to be turned on for the design, allowing the ENx pin(s) to control each desired output.

3.3.9 Set EN_BUCKx Bits

Once the EN_PIN_CTRLx bits are set high for each output that needs to be turned on for the design, the EN_BUCKx bits for each corresponding output can also be set high. It is important that the EN_PIN_CTRLx bits are set before the EN_BUCKx bits so that no outputs are turned on accidentally. Once the EN_BUCKx bits are set high the MCU must be finished with the required I2C commands and can move on to clearing interrupts and setting the ENx pin high to start startup sequence as described in Section 3.1.

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2018) to Revision A (July 2025)	Page
• Clarified nINT behavior dependent on RESET_REG_MASK bit	3
• Added Figure 3-2	4
• Updated Figure 3-3 with mask-dependent nINT response	4
• Changed *LP8752x0-Q1*-specifc references to generic configuration settings	5
• Deleted *LP8752x-Q1* columns from tables	5
• Changed Voltage Settings to OTP-dependent	8

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