User's Guide

LMR43620-Q1 EVM User's Guide

ABSTRACT

The Texas Instruments LMR43620MQ3EVM-2M evaluation module (EVM) helps designers evaluate the operation and performance of the LMR43620-Q1 wide-input buck converter. The LMR43620-Q1 is an easy-to-use synchronous step-down voltage converter capable of driving up to 2 A of load current from an input voltage of up to 36 V. The LMR43620MQ3EVM-2M features an output voltage of 3.3 V and a switching frequency of 2.2 MHz. See the data sheet for additional features, detailed descriptions, and available options.

Table 1-1. Device and Package Configurations

EVM	U1	FREQUENCY	SPREAD SPECTRUM	CURRENT	PIN 1 TRIM
LMR43620MQ3EVM-2M	LMR43620MSC3RPEQ1	2200 kHz	Enabled	2 A	MODE/SYNC

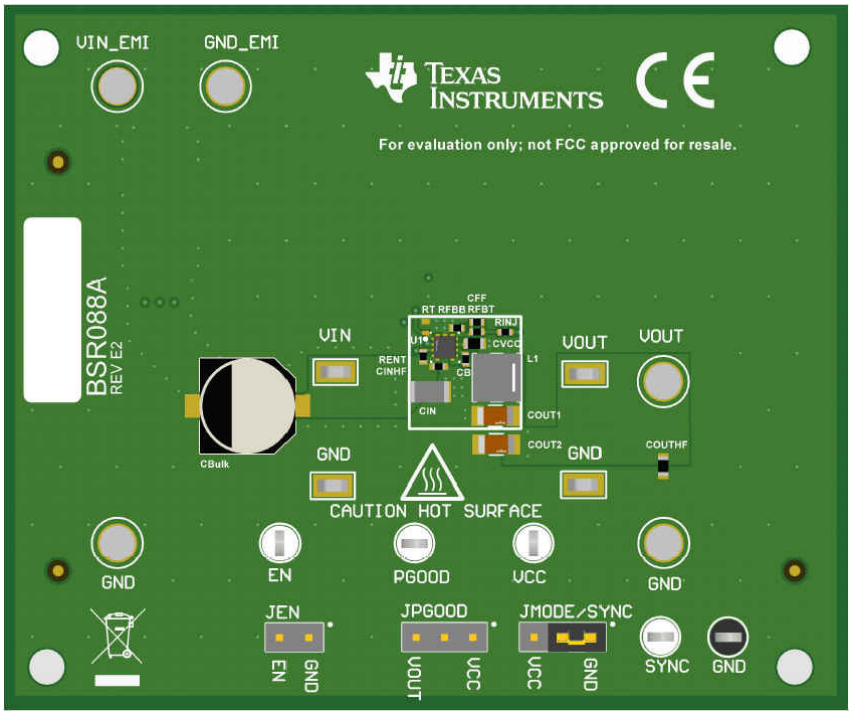

Figure 1-1. LMR43620MQ3EVM-2M Board

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Trademarks

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1 Setup

This section describes the test points and connectors on the EVM and how to properly connect, set up, and use the LMR43620-Q1 EVM.

1.1 Test Points

The test points on the board can be used for connecting to the input of a power supply and output load for the EVM. See Figure 1-1 for typical test setup. The functions of the test points connections are:

- **VIN_EMI —** Input supply to EVM including an EMI filter. Connect to a suitable input supply. Connect at this point for EMI test.
- **GND_EMI —** Ground connection for the input supply
- **VIN —** Input supply to the IC. Can be connected to DMM to measure input voltage after EMI filter.
- **VOUT —** Output voltage test point of EVM. Can be connected to a desired load.
- **GND —** Ground test points
- **EN —** This test point is connected to the EN pin. By default, there is a pullup resistor, R1 (RENT), to VIN to enable the IC.
- **PGOOD —** This test point is connected to the PGOOD pin from the IC. Can be tied to an external supply through a pullup resistor or left open.
- **SYNC —** In a **MODE/SYNC** trim part, this test point is connected to the SYNC pin of the IC. This test point can also be connected to an external clock to synchronize the IC. Make sure R9 (RJM) is installed and R8 (RSYNC) is not installed when applying a sync clock input.

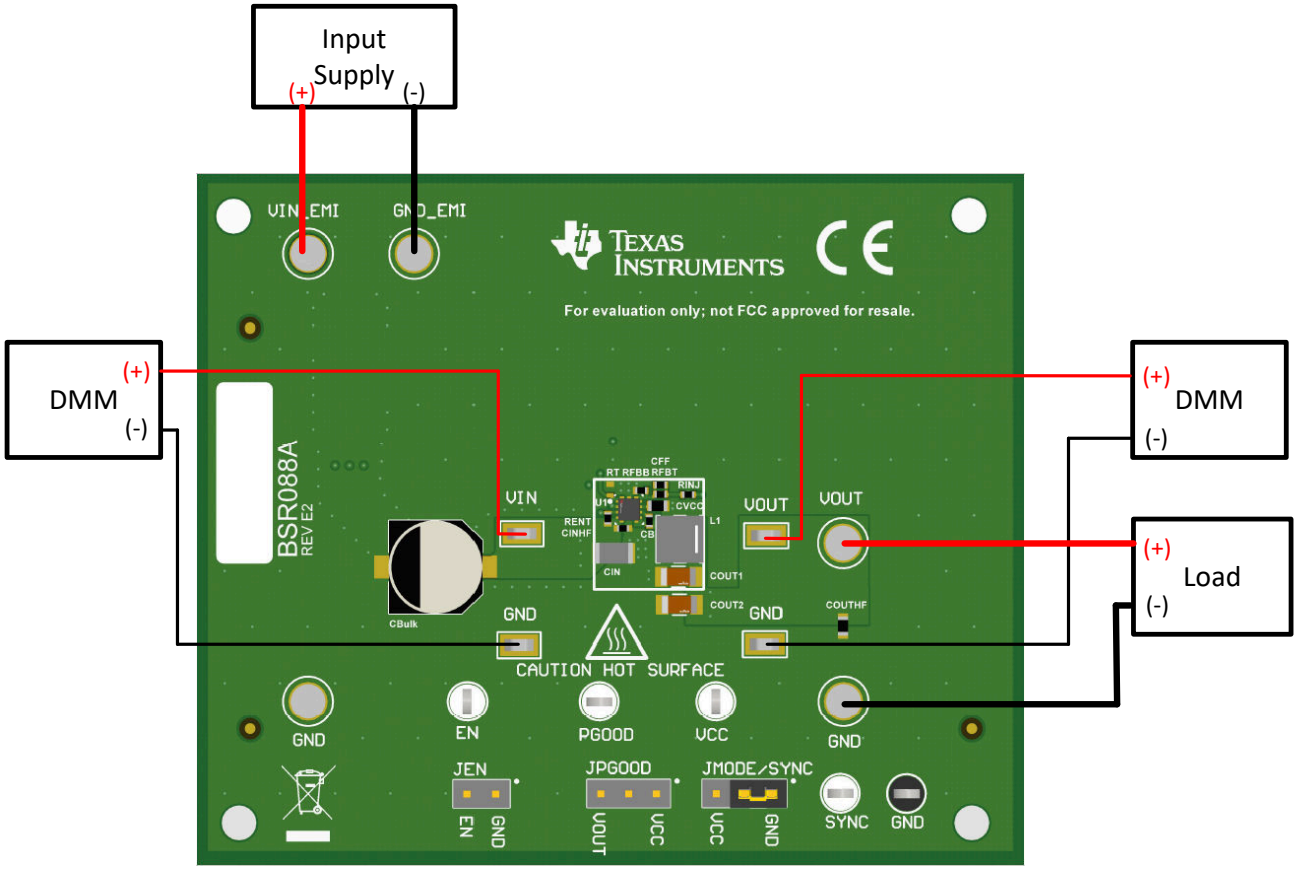

Figure 1-1. EVM Board Connections

1.2 Jumpers

See Figure 1-2 for jumper locations.

- **JEN —** This jumper allows the ENABLE input to be connected to GND in order to disable the IC. By default, this jumper is left open since there is a pullup resistor, R2 (RENT), to VIN to enable the IC.
- **JPGOOD —** Use this jumper to select how the PGOOD pin is connected. A jumper can be used to connect pin 2 and 3. In this configuration, the PGOOD pin will be pulled up to VOUT through R7 (RPGOOD) with a value of 100 kΩ. When connecting the jumper between pin 1 and 2, the PGOOD pin will be pulled up to VCC through R7 (RPGOOD) with a value of 100 kΩ. By default, this jumper is not populated.
- **JMODE/SYNC —** Use this jumper to select the mode of operation in a *MODE/SYNC* trim part. Connecting a jumper between pin 1 and 2 sets the IC operation to PFM (pulse frequency modulation) mode for a higher efficiency at light load. A jumper between pin 2 and pin 3 causes the IC to operate in FPWM (forced pulse width modulation) mode. By default, the jumper is connected between pin 1 and 2. Pin 1 is indicated by the dot on the PCB.

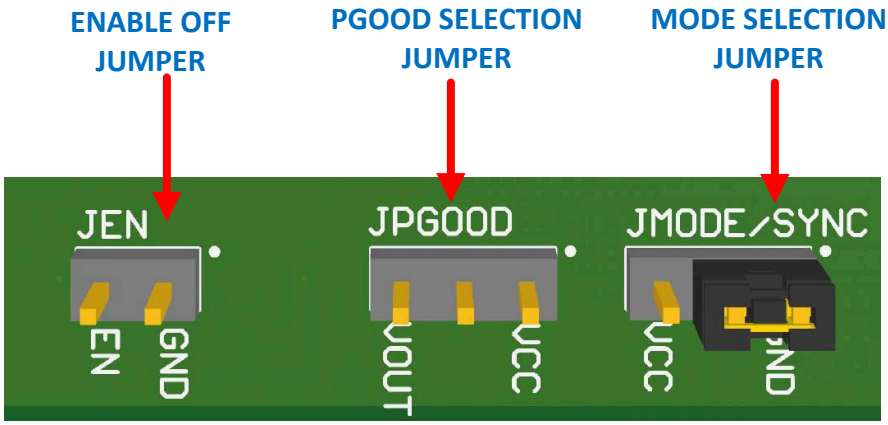

Figure 1-2. Jumper Locations

2 Operation

2.1 Quick Start

1. Connect the voltage supply between the VIN_EMI and GND_EMI supply connections.
2. Connect the load between the VOUT and GND test points.
3. Set the supply voltage at an appropriate level between 3.5 V to 36 V. Set the current limit of the supply to an appropriate level.
4. Turn on the power supply. With the default configuration, the EVM powers up and provides V_{OUT} = 3.3 V.
5. Monitor the output voltage. The maximum load current is rated at 2 A with the LMR43620-Q1 device.

3 Schematic

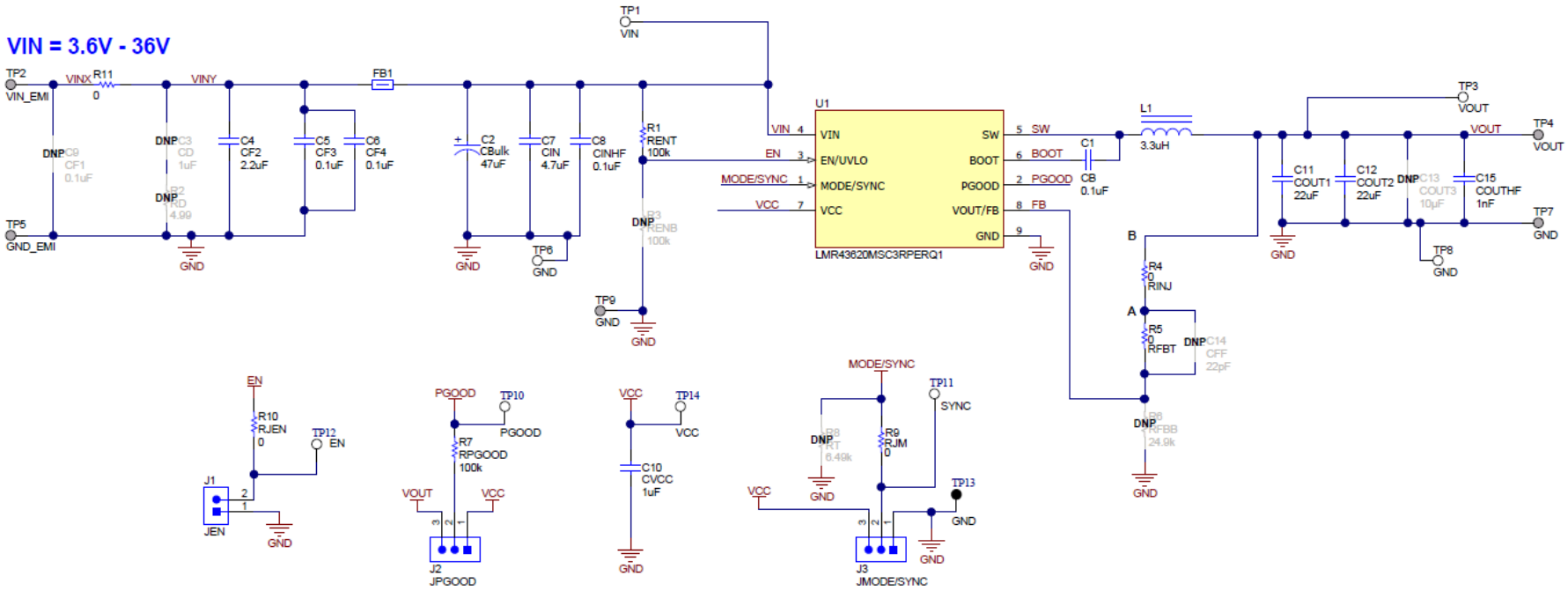

Figure 3-1. LMR43620MQ3EVM -2M Schematic

4 Board Layout

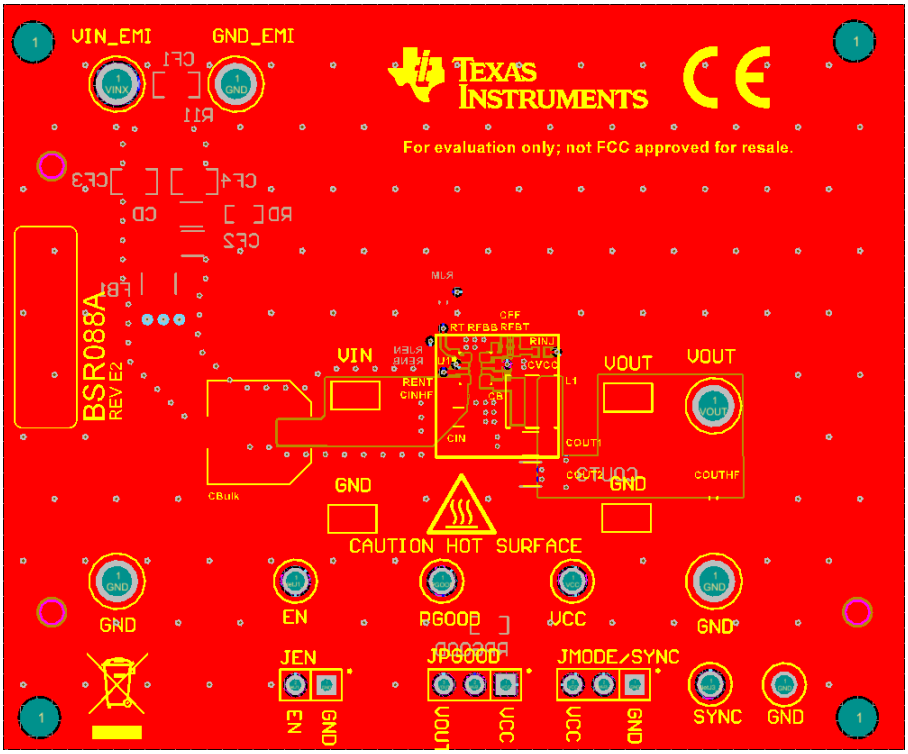

Figure 4-1. Top View of EVM

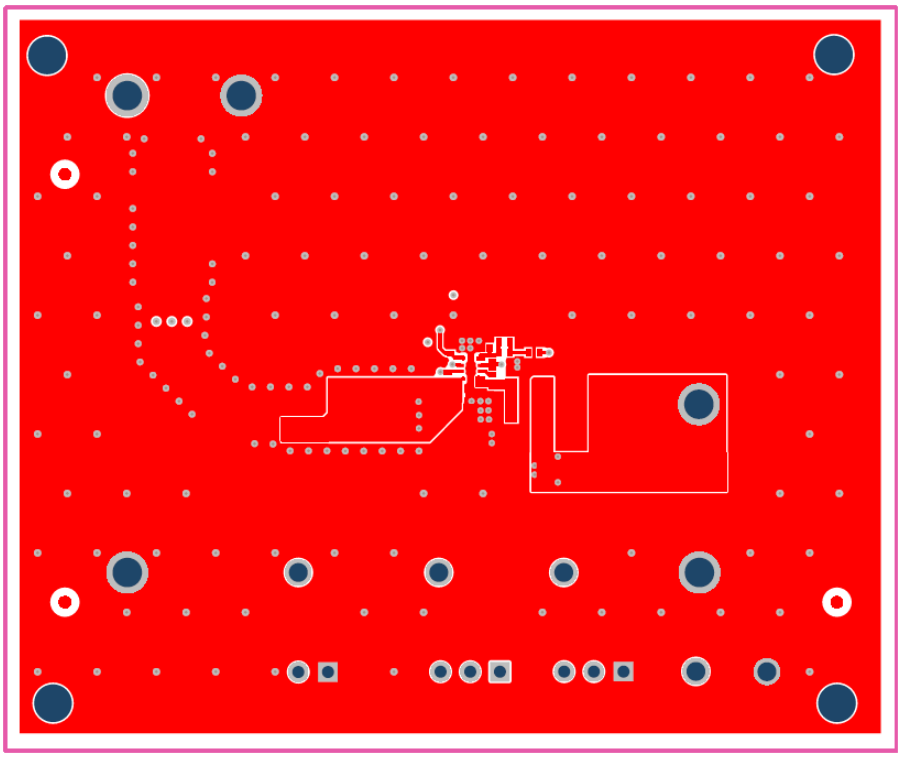

Figure 4-2. EVM Top Copper Layer

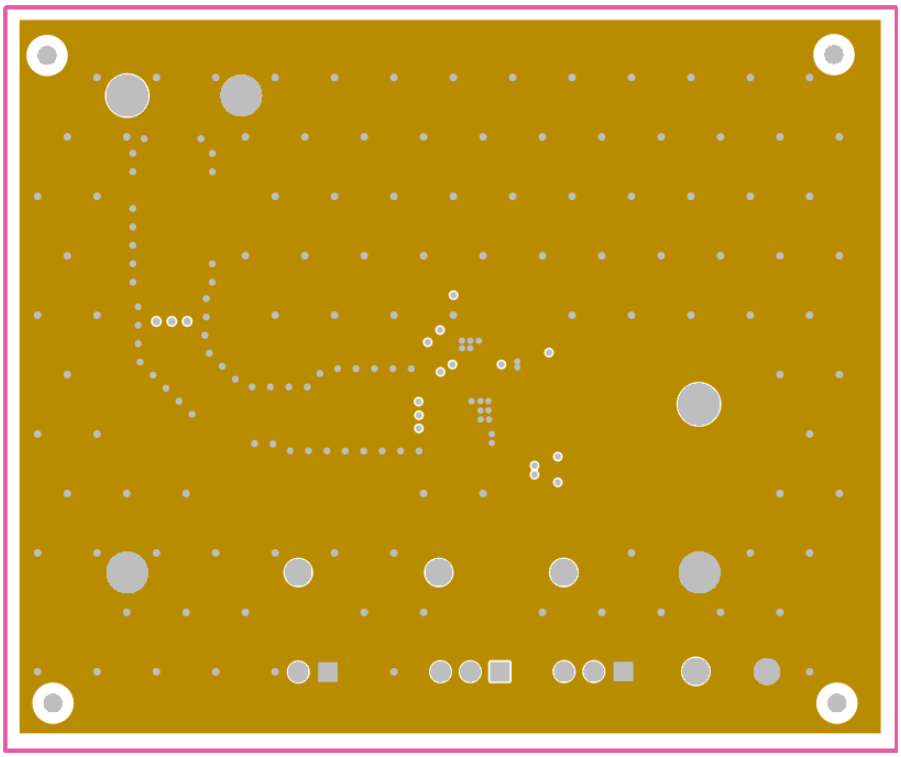

Figure 4-3. Mid-Layer One

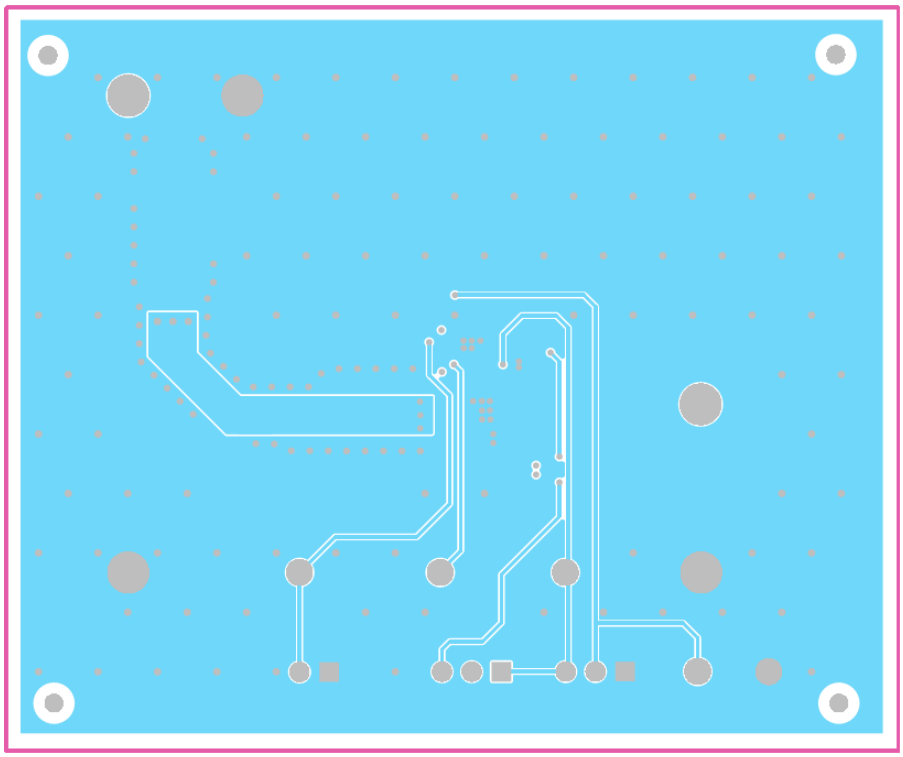

Figure 4-4. Mid-Layer Two

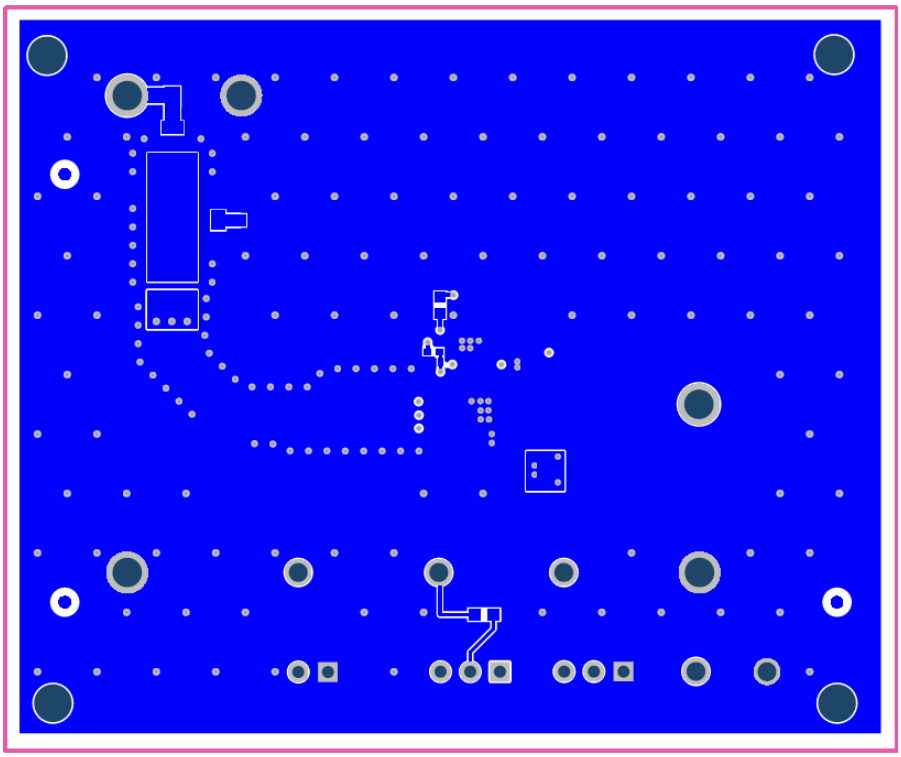

Figure 4-5. EVM Bottom Copper Layer

5 Bill of Materials

Table 5-1. Bill of Materials

DESIGNATOR	COMMENT	DESCRIPTION	MANUFACTURER	PART NUMBER	QTY
C1	CB	CAP, CERM, 0.1 µF, 25 V, ±20%, X7R, 0402	TDK	C1005X7R1E104M050BB	1
C2	CBulk	CAP, AL, 47 µF, 80 V, ±20%, 1.3 Ω, AEC-Q200, SMD	Panasonic	EEE-FN1K470UP	1
C3	CD	CAP, CERM, 1 µF, 100 V, ±10%, X7R, 1206	TDK	C3216X7R2A105K160AA	0
C4	CF2	CAP, CERM, 2.2 µF, 100 V, ±10%, X7S, AEC-Q200 Grade 1, 1206	TDK	CGA5L3X7S2A225K160AB	1
C5, C6	CF3, CF4	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, AEC-Q200 Grade 1, 0805	TDK	CGA4J2X7R2A104K125AA	2
C7	CIN	CAP, CERM, 4.7 µF, 50 V, ±10%, X7R, 1206	MuRata	GRM31CR71H475KA12L	1
C8	CINHF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0402	MuRata	GCM155R71H104KE02D	1
C9	CF1	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, AEC-Q200 Grade 1, 0805	TDK	CGA4J2X7R2A104K125AA	0
C10	CVCC	CAP, CERM, 1 µF, 16 V, ±10%, X7R, 0603	Wurth Elektronik	885012206052	1
C11, C12	COUT1, COUT2	Chip Multilayer Ceramic Capacitors for General Purpose, 1206, 22 µF, X6S, 22%, 10%, 25 V	Murata	GRM31CC81E226KE11L	2
C13	COUT3	CAP, CERM, 10 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 1206	TDK	CGA5L1X7R1H106K160AC	0
C14	CFF	CAP, CERM, 22 pF, 50 V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0402	TDK	CGA2B2NP01H220J050BA	0
C15	COUTHF	CAP, CERM, 1000 pF, 100 V, ±10%, X7R, 0603	MuRata	GRM188R72A102KA01D	1
FB1	FB1	Ferrite Bead, 600 Ω at 100 MHz, 3 A, 1210	Taiyo Yuden	FBMH3225HM601NT	1
FID1, FID2, FID3, FID4, FID5, FID6	Fiducial	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	0
J1	JEN	Header, 100mil, 2x1, Gold, TH	Samtec	HTSW-102-07-G-S	1
J2, J3	JPGOOD, JMODE/SYNC	Header, 100 mil, 3x1, Gold, TH	Samtec	HTSW-103-07-G-S	2
L1	XAL4030-332MEB	Inductor, Shielded, Composite, 3.3 µH, 5.5 A, 0.026 Ω, SMD	Coilcraft	XAL4030-332MEB	1
LBL1	THT-14-423-10	Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	Brady	THT-14-423-10	1
R1	RENT	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402100KFKED	1
R2	RD	RES, 4.99, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06034R99FKEA	0
R3	RENB	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402100KFKED	0
R4, R5, R10	RINJ, RFBT, RJEN	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04020000Z0ED	3
R6	RFBB	RES, 24.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040224K9FKED	0
R7	RPGOOD	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100KFKEA	1
R8	RT	RES, 6.49 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04026K49FKED	0
R9	RJM	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06030000Z0EA	1
R11	RFILTJ	RES, 0, 1%, 0.5 W, 1206	Keystone	5108	1
SH-J1	SNT-100-BK-G	Shunt, 100 mil, Gold plated, Black	Samtec	SNT-100-BK-G	1
TP1, TP3, TP6, TP8	VIN, VOUT, GND, GND	Test Point, Miniature, SMT	Keystone	5015	4
TP2, TP4, TP5, TP7, TP9	VIN_EMI, VOUT, GND_EMI, GND, GND	Terminal, Turret, TH, Double	Keystone	1502-2	5

Table 5-1. Bill of Materials (continued)

DESIGNATOR	COMMENT	DESCRIPTION	MANUFACTURER	PART NUMBER	QTY
TP10, TP11, TP12, TP14	PGOOD, SYNC, EN, VCC	Test Point, Multipurpose, White, TH	Keystone	5012	4
TP13	GND	Test Point, Multipurpose, Black, TH	Keystone	5011	1
U1	LMR43620MSC3RPERQ1	36-V, 2-A Buck Converter with 1.5-µA IQ in 2-mm × 2-mm HotRod QFN	Texas Instruments	LMR43620MSC3RPERQ1	1

6 Test Results

6.1 LMR43620MQ3EVM-2M Test Results

The LMR43620MQ3EVM-2M variant is used for the following images.

6.1.1 Efficiency and Load Regulation

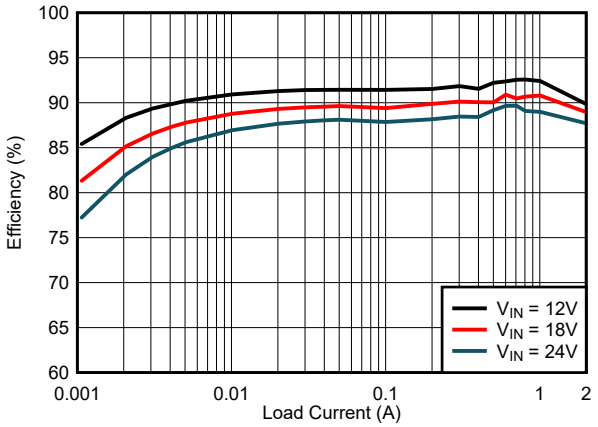

Figure 6-1. 3.3 V_{OUT}, 2.2-MHz Efficiency

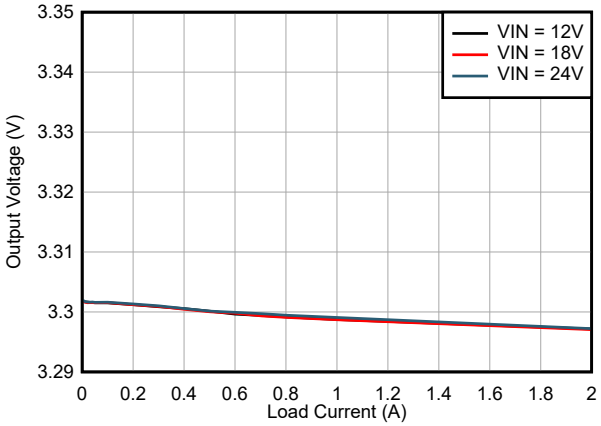

Figure 6-2. 3.3 V_{OUT}, 2.2-MHz Load Regulation

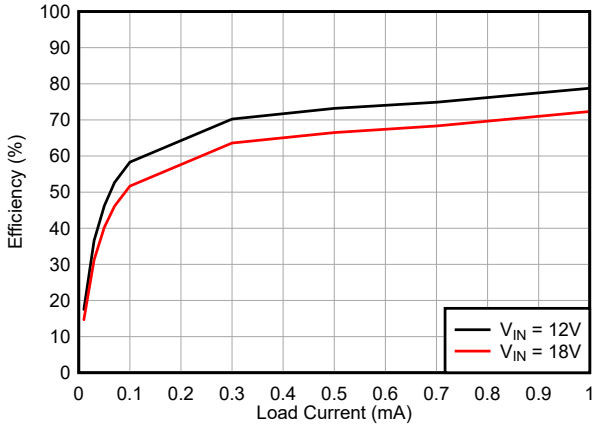

Figure 6-3. 3.3 V_{OUT}, Light Load Efficiency

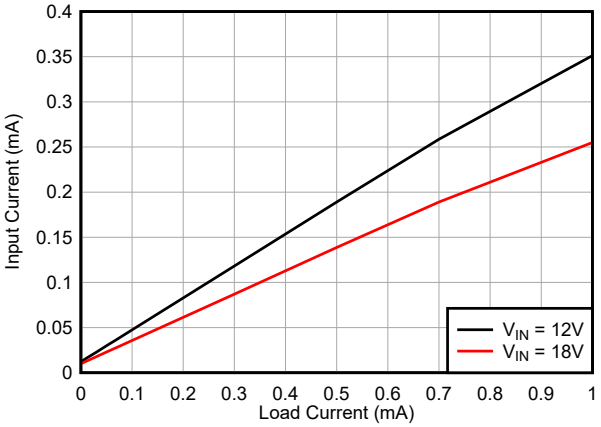

Figure 6-4. Input Current vs Load Current for 3.3 V_{OUT}

6.1.2 Load Transients

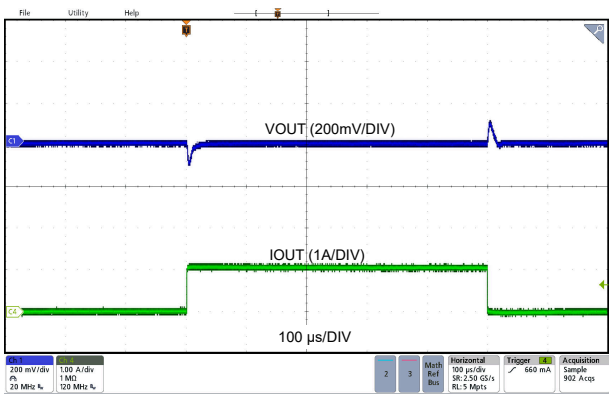

Figure 6-5. Load Transient 12 V_{IN}, 3.3 V_{OUT}, I_{OUT} = 0 A to 1 A, Slew Rate = 1 A/µs (FPWM)

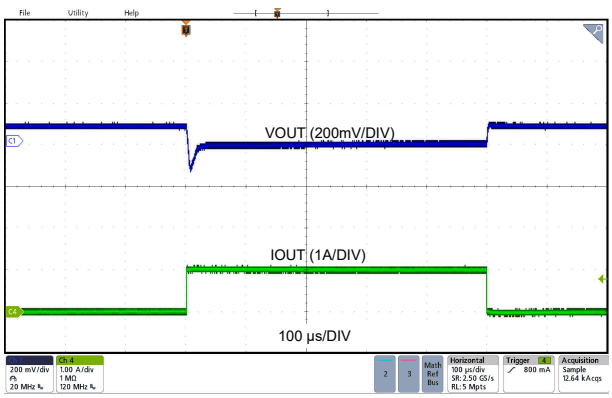

Figure 6-6. Load Transient 12 V_{IN}, 3.3 V_{OUT}, I_{OUT} = 0 A to 1 A, Slew Rate = 1 A/µs (AUTO)

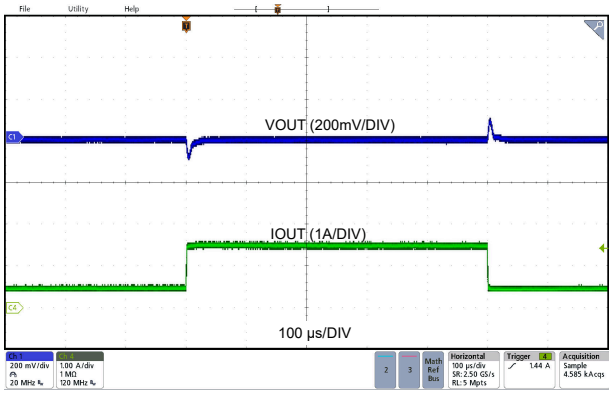

Figure 6-7. Load Transient 12 V_{IN}, 3.3 V_{OUT}, I_{OUT} = 0.5 A to 1.5 A, Slew Rate = 1 A/µs (FPWM)

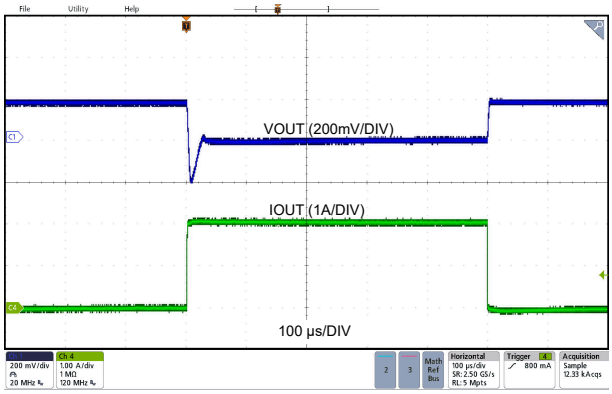

Figure 6-8. Load Transient 12 V_{IN}, 3.3 V_{OUT}, I_{OUT} = 0 A to 2 A, Slew Rate = 1 A/µs (AUTO)

6.1.3 Output Ripple and Thermal Picture

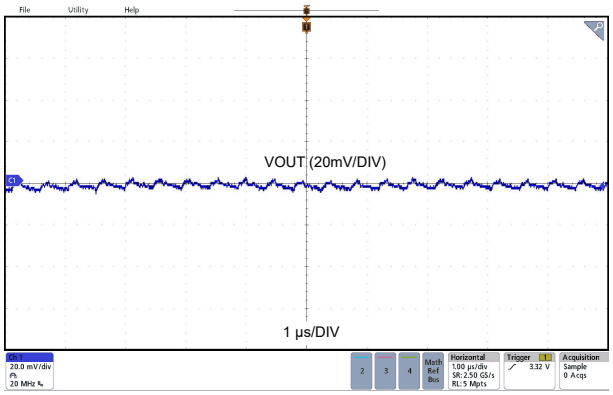

Figure 6-9. Output Ripple at 12 V_{IN}, 3.3 V_{OUT} (Fixed), 2-A Load

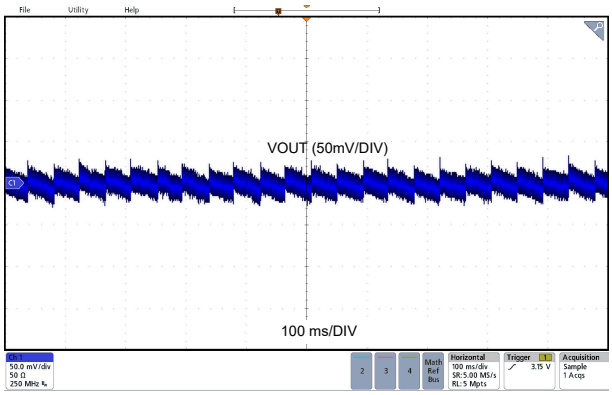

Figure 6-10. Output Ripple at 12 V_{IN}, 3.3 V_{OUT} (Fixed), No Load

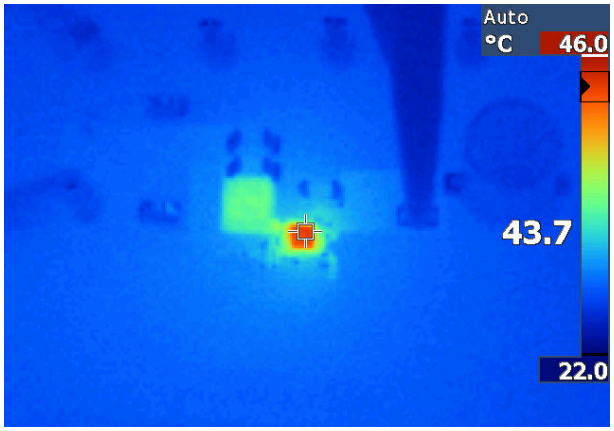

Figure 6-11. Thermal Capture, 12 V_{IN}, 3.3 V_{OUT}, 2-A Load, 2.2 MHz, Θ_{JA}≅ 46°C/W

6.1.4 Conducted EMI

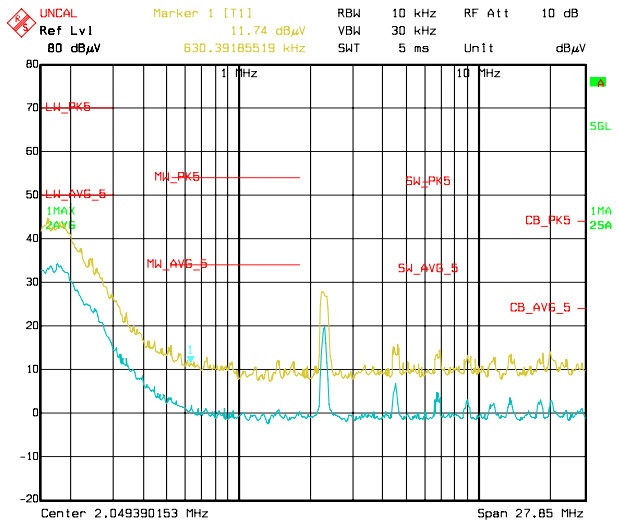

Figure 6-12. LMR43620MQ3EVM-2M Low Frequency Conducted EMI Results 13.5 V_{IN}, 3.3 V_{OUT}, I_{OUT} = 2 A (Blue-Average Scan and Yellow-Peak Scan)

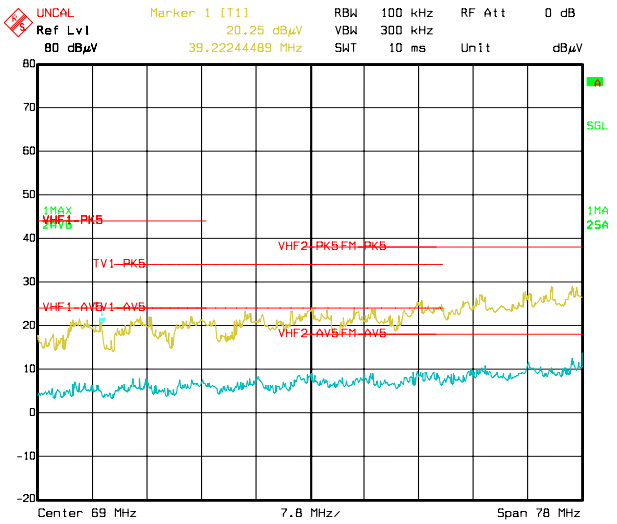

Figure 6-13. LMR43620MQ3EVM-2M High Frequency Conducted EMI Results 13.5 V_{IN}, 3.3 V_{OUT}, I_{OUT} = 2 A (Blue-Average Scan and Yellow-Peak Scan)

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2021) to Revision B (December 2021)	Page
• Updated EVM schematic, BoM, and test results for RTM release	3

Changes from Revision * (February 2020) to Revision A (July 2021)	Page
• First public release	3
• Changed instances of LMR43620 to LMR43620-Q1	3
• Updated images throughout document	3
• Updated PGOOD test point description	3
• Updated JPGOOD and JMODE/RT jumper descriptions	4
• Updated Table 5-1	10
• Added Section 6	12

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