User's Guide
SNVU582A–September 2018–Revised October 2018

LP8733-Q1 and LP8732-Q1 Configuration Guide

This configuration guide is designed to help users understand how to use a microcontroller unit (MCU) to configure an LP8733-Q1 or LP8732-Q1 PMIC. Instead of requiring a new program in one-time programmable (OTP) memory for each design, a specific program described in this configuration guide can be configured at startup to meet design requirements.

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1 Introduction

The LP8733-Q1 or LP8732-Q1 is a PMIC with two programmable step-down DCDC converters, and two programmable LDO regulators. Typically the settings for the LP8733-Q1 or LP8732-Q1 PMIC are programmed during manufacturing into one-time programmable (OTP) memory. However, with a microcontroller unit (MCU) this device can also be configured after each start up to fit different design requirements.

This guide explains how to set up an LP8733-Q1 or LP8732-Q1 PMIC to be configured at start up so that it can be used in different designs without the need for a new OTP. The OTP version 0x00 has been designed to allow the PMIC to be easily configured at start up. Refer to the *LP8732x-Q1 Dual High-Current Buck Converter and Dual Linear Regulator* data sheet and *LP8733x-Q1 Dual High-Current Buck Converter and Dual Linear Regulator* data sheet for device specifications and detailed functionality.

2 Setup

There are a few important connections to make sure that the LP8733-Q1 or LP8732-Q1 PMIC is configured correctly. This section describes these important connections. Figure 1 shows a good example of how to connect an MCU to the LP8733-Q1 or LP8732-Q1 PMIC.

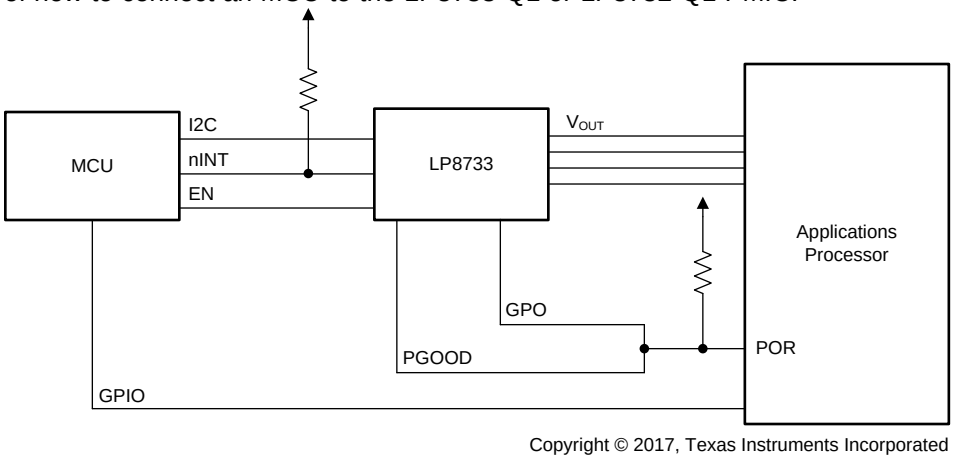

Figure 1. Typical MCU Connection to LP8733-Q1 or LP8732-Q1 for Startup Configuration

2.1 SCL and SDA Pins

The SCL and SDA lines (pins 17 and 18, respectively) are used to communicate between the MCU and the LP8733-Q1 or LP8732-Q1 PMIC using an I^2C-compatible Interface. The I^2C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed on the line and remain HIGH even when the bus is idle. The LP8733-Q1 or LP8732-Q1 PMIX supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz). For all I^2C protocol details refer to the device data sheets.

2.2 EN Pin

The EN pin (pin 6) is used to enable/disable all of the regulators and the GPO on the LP8733-Q1 or LP8732-Q1 PMIC. It is recommended that the EN pin be driven low to disable all of the regulators and the GPO until the device is configured to the desired settings. Drive this pin low to disable and high to enable.

2.3 nINT Pin

The nINT pin (pin 9) is an open-drain, active low output from the LP8733-Q1 or LP8732-Q1 PMIC, and should be connected to a pull-up resistor. In the 0x00 OTP an interrupt is generated on this pin whenever the RESET_REG_INT bit is set high. The RESET_REG_INT bit is set high when either the VANA supply voltage has decreased below the undervoltage threshold level or the host has requested a reset using the SW_RESET bit in the RESET register. By monitoring the nINT pin, the MCU will know when the PMIC registers are reset to the values determined by the 0x00 OTP, and can take the necessary actions to ensure that the PMIC is configured as needed.

After a power-on reset the LP8733-Q1 or LP8732-Q1 PMIC requires a delay of 1.2ms before there can be any communication through the I^2C interface. This required delay can be ensured by monitoring the nINT pin. After a power-on reset the nINT pin is driven high while the registers are reset and the OTP is read to set the registers to their initial values. After 1.2ms the nINT pin is driven low, signaling that the registers have been reset and can be configured to fit the design requirements.

NOTE: To monitor the nINT pin correctly, the MCU must clear all interrupts before enabling all of the outputs on the LP8733-Q1 or LP8732-Q1 PMIC. Write a 1 to the RESET_REG_INT bit in the INT_TOP_2 register to clear this interrupt. If all interrupts are not cleared before enabling the LP8733-Q1 or LP8732-Q1 PMIC outputs, then there will be no change on the nINT pin when an interrupt is generated and the MCU will not be able to detect a register reset.

3 Configuration

This section describes the default 0x00 OTP settings, and how to configure these settings to meet your design requirements.

3.1 Configuration Sequence

Using the setup described in Section 2 lets the MCU easily configure the LP8733-Q1 or LP8732-Q1 PMIC after a power-on reset, or after any event causing a register reset. To make sure that this is done correctly follow the sequence described in this section. Do these steps after a power-on reset or a register reset to make sure that the LP8733-Q1 or LP8732-Q1 PMIC is configured correctly:

1. Turn on the PMIC. (VANA > $VANA_{UVLO}$)
2. Wait for the nINT line to be set low. (Check RESET_REG_INT bit, and set EN pin low if necessary)
3. Set the new configuration using I^2C communication in the recommended order (see Section 3.3):
    1. Voltage settings
    2. Current limit/regulator settings
    3. GPO settings
    4. Clock sync functions
    5. PGOOD settings
    6. Interrupt settings
    7. Startup/shutdown settings
    8. Set EN_PIN_CTRL bits
    9. Set EN bits
4. Clear Interrupts.
5. Set EN pin high.

Upon a power-on reset, waiting for the nINT line to be set low ensures that the PMIC is ready for I^2C communication. Waiting for the nINT line to be set low at any other time allows the PMIC to know when a register reset has occurred. The timing diagrams in Figure 2 and Figure 3 show how to configure the LP8733-Q1 or LP8732-Q1 PMIC after a power-on reset or register reset has occurred. When all of the I^2C writes are finished the interrupts should be cleared and the PMIC enabled by the MCU. The MCU can do this by writing a 1 to the RESET_REG_INT bit to clear the interrupt and by pulling the EN pin high to turn on the PMIC outputs.

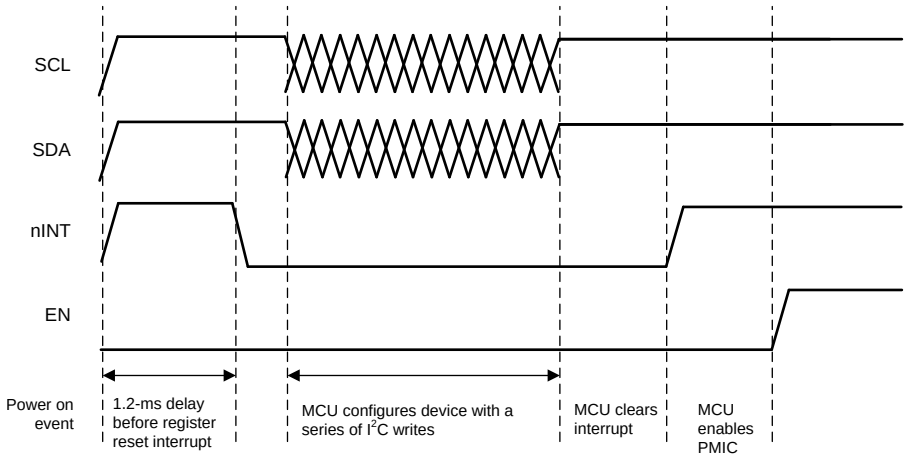

Figure 2. Configuration Sequence During Startup

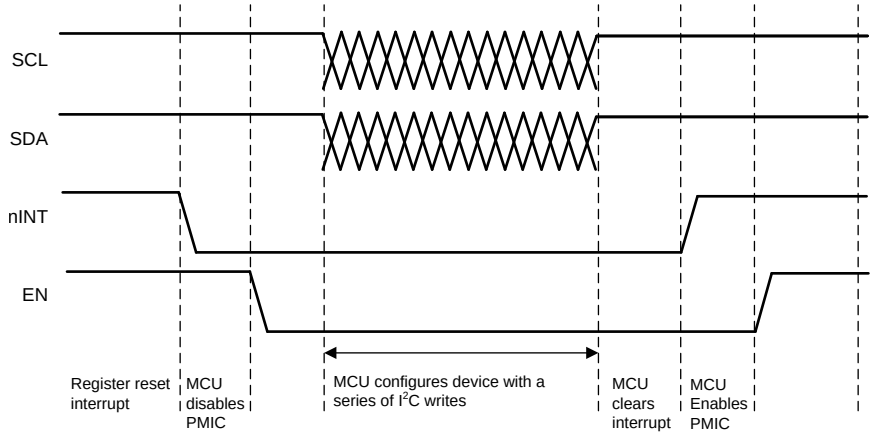

Figure 3. Configuration Sequence During Reset

3.2 0x00 OTP BOOT Configuration

All LP8733-Q1 or LP8732-Q1 PMIC resource settings are stored in the form of registers. These settings define, for example, BUCK or LDO default voltages, GPIO functionality, and power-up and power-down sequences. The 0x00 OTP by default has no sequencing so that the user can configure the desired sequence. Refer to the data sheet for a full list of the resource setting registers.

Each device has predefined values stored in OTP which control the default configuration of the device. The tables in this section list the OTP-programmed values for each device, distinguished by the OTP_ID.

Table 1 lists the device settings for BUCK0 and BUCK1. The maximum allowed slew-rate for BUCKx depends on the output capacitance. Refer to the device data sheets for output capacitance boundary conditions.

Table 1. BUCK0 and BUCK1 OTP Settings

	Description	Bit Name	LP873300-Q1	LP873200-Q1	Configurable
	Buck phase configuration (2 single phase Bucks or combined 2 phase, denoted as 1+1 or 2-phase)		1 + 1	1 + 1	No
	Switching frequency		2 MHz	2 MHz	No
	Spread spectrum	EN_SPREAD_SPEC	No	No	Yes

Table 1. BUCK0 and BUCK1 OTP Settings (continued)

	Description	Bit Name	LP873300-Q1	LP873200-Q1	Configurable
BUCK0	Output voltage	BUCK0_VSET	0.7 V	0.7 V	Yes
	Enable, EN-pin or I²C register	BUCK0_EN_PIN_CTRL	I²C	I²C	Yes
	Control for BUCK0	BUCK0_EN	Low	Low	Yes
	Force PWM mode or auto mode	BUCK0_FPWM	auto	auto	Yes
	Peak current limit	BUCK0_ILIM	4 A	3 A	Yes
	Slew rate	BUCK0_SLEW_RATE	3.8 mV/µs	3.8 mV/µs	Yes
	Startup Delay	BUCK0_ STARTUP_ DELAY	0 ms	0 ms	Yes
	Shutdown Delay	BUCK0_ SHUTDOWN_ DELAY	0 ms	0 ms	Yes
BUCK1	Output voltage	BUCK1_VSET	0.7 V	0.7 V	Yes
	Enable, EN-pin or I²C register	BUCK1_EN_PIN_CTRL	I²C	I²C	Yes
	Control for BUCK1	BUCK1_EN	Low	Low	Yes
	Force PWM mode or auto mode	BUCK1_FPWM	auto	auto	Yes
	Peak current limit	BUCK1_ILIM	4 A	3 A	Yes
	Slew rate	BUCK1_SLEW_RATE	3.8 mV/µs	3.8 mV/µs	Yes
	Startup Delay	BUCK1_ STARTUP_ DELAY	0 ms	0 ms	Yes
	Shutdown Delay	BUCK1_ SHUTDOWN_ DELAY	0 ms	0 ms	Yes

Table 2 lists the device settings for LDO0 and LDO1.

Table 2. LDO0 and LDO1 OTP Settings

	Description	Bit Name	LP873300-Q1	LP873200-Q1	Configurable
LDO0	Output voltage	LDO0_VSET	0.8 V	0.8 V	Yes
	Enable, EN-pin or I²C register	LDO0_EN_PIN_CTRL, LDO0_EN	I²C	I²C	Yes
	Control for LDO0	LDO0_EN	Low	Low	Yes
	Startup Delay	LDO0_ STARTUP_ DELAY	0 ms	0 ms	Yes
	Shutdown Delay	LDO0_ SHUTDOWN_ DELAY	0 ms	0 ms	Yes
LDO1	Output voltage	LDO1 _VSET	0.8 V	0.8 V	Yes
	Enable, EN-pin or I²C register	LDO1_EN_PIN_CTRL, LDO1_EN	I²C	I²C	Yes
	Control for LDO1	LDO1_EN	Low	Low	Yes
	Startup Delay	LDO1_ STARTUP_ DELAY	0 ms	0 ms	Yes
	Shutdown Delay	LDO1_ SHUTDOWN_ DELAY	0 ms	0 ms	Yes

Table 3 lists the device settings for GPIOs.

Table 3. EN, CLKIN and GPIO Pin Settings

	Description	Bit Name	LP873300-Q1	LP873200-Q1	Configurable
EN pin	EN pin pulldown resistor enable or disable	EN_PD	Enabled	Enabled	Yes
CLKIN pin	CLKIN or GPO2 mode selection	CLKIN_PIN_SEL	GPO2	GPO2	Yes
	CLKIN pin pulldown resistor enable or disable (applicable for both CLKIN and GPO2 modes)	CLKIN_PD	Enabled	Enabled	Yes
	Frequency of external clock when connected to CLKIN	EXT_CLK_FREQ	2 MHz	2 MHz	Yes
	Enable for the internal PLL. When PLL disabled, internal RC OSC is used	EN_PLL	Disabled	Disabled	Yes

Table 3. EN, CLKIN and GPIO Pin Settings (continued)

	Description	Bit Name	LP873300-Q1	LP873200-Q1	Configurable
GPO	GPO output type (push-pull or open drain)	GPO_OD	OD	OD	Yes
	Enable, EN-pin or I^2C register	GPO_EN_PIN_CTRL, GPO_EN	I^2C	I^2C	Yes
	Control for GPO	GPO_EN	Low	Low	Yes
	Startup Delay	GPO_ STARTUP_ DELAY	0 ms	0 ms	Yes
	Shutdown Delay	GPO_ SHUTDOWN_ DELAY	0 ms	0 ms	Yes
GPO2	GPO2 output type (push-pull or open drain)	GPO2_OD	OD	OD	Yes
	Enable, EN-pin or I^2C register	GPO2_EN_PIN_CTRL	I^2C	I^2C	Yes
	Control for GPO2	GPO2_EN	Low	Low	Yes
	Startup Delay	GPO2_ STARTUP_ DELAY	0 ms	0 ms	Yes
	Shutdown Delay	GPO2_ SHUTDOWN_ DELAY	0 ms	0 ms	Yes

Table 4 lists the device settings for PGOOD.

Table 4. PGOOD OTP Settings

	Description	Bit Name	LP873300-Q1	LP873200-Q1	Configurable
Signals monitored by PGOOD	BUCK0 output voltage	EN_PGOOD_BUCK0	Yes	Yes	Yes
	BUCK1 output voltage	EN_PGOOD_BUCK1	Yes	Yes	Yes
	LDO0 output voltage	EN_PGOOD_LDO0	Yes	Yes	Yes
	LDO1 output voltage	EN_PGOOD_LDO1	Yes	Yes	Yes
	Thermal warning	EN_PGOOD_TWARN	Yes	Yes	Yes
PGOOD mode selections	PGOOD thresholds for BUCK0, BUCK1 (Undervoltage / Window (undervoltage and overvoltage))	PGOOD_WINDOW_BUCK	Window	Window	Yes
	PGOOD thresholds for LDO0, LDO1 (Undervoltage / Window (undervoltage and overvoltage))	PGOOD_WINDOW_LDO	Window	Window	Yes
	PGOOD operating mode (detecting UNUSUAL situations / detecting UNVALID situations)	PGOOD_MODE	Detecting UNVALID situations	Detecting UNVALID situations	Yes
	PGOOD signal mode (status / latched until fault source read)	PG_FAULT_GATES_PGOOD	Status	Status	Yes
	PGOOD output mode (push-pull or open drain)	PGOOD_OD	OD	OD	Yes
	PGOOD polarity (active high/ active low)	PGOOD_POL	Active high	Active high	Yes

Table 5 lists the device settings for thermal warning. Also refer to Table 4 for PGOOD and Table 7 for interrupts.

Table 5. Protections OTP Settings

	Description	Bit Name	LP873300-Q1	LP873200-Q1	Configurable
Protections	Thermal warning level (125°C or 137°C)	TDIE_WARN_LEVEL	137°C	137°C	Yes
	Input overvoltage protection	(Hidden from customer, always enabled)	Enabled	Enabled	No

Table 6 lists the device settings for I^2C and OTP revision ID values.

Table 6. Device Identification and I^2C Settings

	Description	Bit Name	LP873300-Q1	LP873200-Q1	Configurable
I^2C address			0x60	0x61	No
I2C speed default	Set Hs-mode I^2C by default		No	No	No
DEVICE_ID	Device specific ID code	DEVICE_ID	0x0	0x1	No
OTP_ID	Identification code for OTP version	OTP_ID	0x00	0x00	No

Table 7 lists the device settings for interrupts. When an interrupt from an event is unmasked, an interrupt is generated to nINT pin.

Table 7. Interrupt Mask Settings

	Interrupt event	Bit Name	LP873300-Q1	LP873200-Q1	Configurable
General	PGOOD pin changing active to inactive	PGOOD_INT_MASK	Masked	Masked	Yes
	Sync clock appears or disappears	SYNC_CLK_MASK	Masked	Masked	Yes
	Thermal warning	TDIE_WRN_MASK	Masked	Masked	Yes
	Load measurement ready	I_MEAS_MASK	Masked	Masked	Yes
	Register reset	RESET_REG_MASK	Unmasked	Unmasked	Yes
BUCK0	Buck0 PGood active	BUCK0_PGR_MASK	Masked	Masked	Yes
	Buck0 PGood inactive	BUCK0_PGF_MASK	Masked	Masked	Yes
	Buck0 current limit	BUCK0_ILIM_MASK	Masked	Masked	Yes
BUCK1	Buck1 PGood active	BUCK1_PGR_MASK	Masked	Masked	Yes
	Buck1 PGood inactive	BUCK1_PGF_MASK	Masked	Masked	Yes
	Buck1 current limit	BUCK1_ILIM_MASK	Masked	Masked	Yes
LDO0	LDO0 PGood active	LDO0_PGR_MASK	Masked	Masked	Yes
	LDO0 PGood inactive	LDO0_PGF_MASK	Masked	Masked	Yes
	LDO0 current limit	LDO0_ILIM_MASK	Masked	Masked	Yes
LDO1	LDO1 PGood active	LDO1_PGR_MASK	Masked	Masked	Yes
	LDO1 PGood inactive	LDO1_PGF_MASK	Masked	Masked	Yes
	LDO1 current limit	LDO1_ILIM_MASK	Masked	Masked	Yes

3.3 Recommended Order of Configuring Registers Through I²C

This section describes the main settings that can be changed to fit a specific design, in the recommended order. Refer to the data sheets and Section 3.2 for all of these settings and their corresponding bits and registers.

3.3.1 Voltage Settings

By default all of the voltage settings for the 0x00 OTP are set to their smallest values. These settings can be changed by writing to these fields:

- BUCK0_VSET field in BUCK0_VOUT register
- BUCK1_VSET field in BUCK1_VOUT register
- LDO0_VSET field in LDO0_VOUT register
- LDO1_VSET field in LDO1_VOUT register

Refer to the data sheets to see how the values of these registers correspond to different voltages.

3.3.2 Current Limit and Other Regulator Settings

Each BUCK has two CTRL registers that can be used to set their current limits as well as enable their output discharge resistors or set auto/forced PWM mode. Each LDO also has a CTRL register to enable their output discharge resistors. Included in these registers is an EN_PIN_CTRL and EN bit for each regulator. It is recommended to set the EN_PIN_CTRL and EN bits last to avoid any regulators turning on before configuration is complete. These regulator setting fields are summarized in Table 8. Refer to the data sheets for a full description of all registers and their settings.

Table 8. Regulator Control Settings Registers

Regulator	Register	Fields That Should be Configured	Fields That Should Not be Configured Until the PMIC is Ready to be Powered Up (Section 3.3.8)
BUCK0	BUCK0_CTRL_1	BUCK0_FPWM, BUCK0_RDIS_EN	BUCK0_EN_PIN _CTRL, BUCK0_EN
	BUCK0_CTRL_2	BUCK0_ILIM, BUCK0_SLEW_RATE	
BUCK1	BUCK1_CTRL_1	BUCK1_FPWM, BUCK1_RDIS_EN	BUCK1_EN_PIN _CTRL, BUCK1_EN
	BUCK1_CTRL_2	BUCK1_ILIM, BUCK1_SLEW_RATE	
LDO0	LDO0_CTRL	LDO0_RDIS_EN	LDO0_EN_PIN _CTRL, LDO0_EN
LDO1	LDO1_CTRL	LDO1_RDIS_EN	LDO1_EN_PIN _CTRL, LDO1_EN

3.3.3 GPO Settings

The LP8733-Q1 or LP8732-Q1 PMIC supports the use of two GPOs, GPO and GPO2. GPO2 can also be used as a CLKIN input. The selection between CLKIN and GPO2 pin function is set with CLKIN_PIN_SEL bit in the CONFIG register. Set CLKIN_PIN_SEL low to configure the pin as GPO2. Both GPOs can be set as open drain or push-pull outputs and can be controlled using the GPO_CTRL register. Refer to the data sheets for more information on each of the fields in the GPO_CTRL register.

3.3.4 Clock Sync Functions

When the CLKIN_PIN_SEL bit is set high, the CLKIN input can be used to synchronize the switching clock of the buck regulators with an external clock. The EN_PLL bit in the PLL_CTRL register must also be set high to synchronize to an external clock. The nominal frequency of the external input clock is set by the EXT_CLK_FREQ[4:0] bits in the PLL_CTRL register, and can be from 1 MHz to 24 MHz with 1-MHz steps. The external clock must be inside accuracy limits (–30%, +10%) of the selected frequency for valid clock detection. Refer to the data sheets for more information on this function.

3.3.5 PGOOD Settings

The PGOOD output can be used to monitor several signals and has multiple settings to configure which are:

- Monitoring of regulator output voltage (Individual regulators can be selected)
- Monitoring of input supply overvoltage
- Monitoring of thermal warning/shutdown
- Push-pull or open drain output
- Gated or continuous operating mode
- Undervoltage only or undervoltage and overvoltage monitoring
- Adjustable polarity

All of the PGOOD settings can be configured using the PGOOD_CTRL_1 and PGOOD_CTRL_2 registers, with the exception of the thermal shutdown and input supply overvoltage monitoring. Refer to the data sheets for more information on the PGOOD signal functionality.

3.3.6 Interrupt Settings

The LP8733-Q1 or LP8732-Q1 PMIC has many interrupt signals that can be used to indicate different events including regulator over-current events, regulator PGOOD events, regulator short-circuit events, and clock events. The registers containing all of these interrupts:

- INT_TOP_1 register
- INT_TOP_2 register
- INT_BUCK register
- INT_LDO register

These interrupts can all be masked or unmasked using these registers:

- TOP_MASK_1 register
- TOP_MASK_2 register
- BUCK_MASK register
- LDO_MASK register

By default the 0x00 OTP has only RESET_REG_INT unmasked to allow the MCU to know when the PMIC registers are reset to the values determined by the 0x00 OTP, so the MCU can take the necessary actions to ensure that the PMIC is configured as needed. Other interrupts can be unmasked as is needed. However, unmasking other interrupts will mean that when an interrupt is generated on the nINT line, the interrupt registers will need to be read to determine what caused the interrupt.

3.3.7 Startup and Shutdown Sequence

Each of the LDOs, BUCKs and GPOs on the LP8733-Q1 or LP8732-Q1 can be set to startup and shutdown in a specific sequence. To configure the desired sequence the STARTUP_DELAY and SHUTDOWN_DELAY fields for each output need to be set to a value between 0x0 and 0xF. The delay time that this value corresponds to depends on the STARTUP_DELAY_SEL bit and the SHUTDOWN_DELAY_SEL bit located in the CONFIG register. A value of 0 on one of these bits will allow a delay ranging from 0 ms to 7.5 ms with 0.5-ms steps, and a value of 1 on one of these bits will allow a delay ranging from 0 ms to 15 ms with 1-ms steps. Figure 4 shows an example of how these delays can be used to configure a startup and shutdown sequence. Refer to the data sheets for a full description of all registers and their settings.

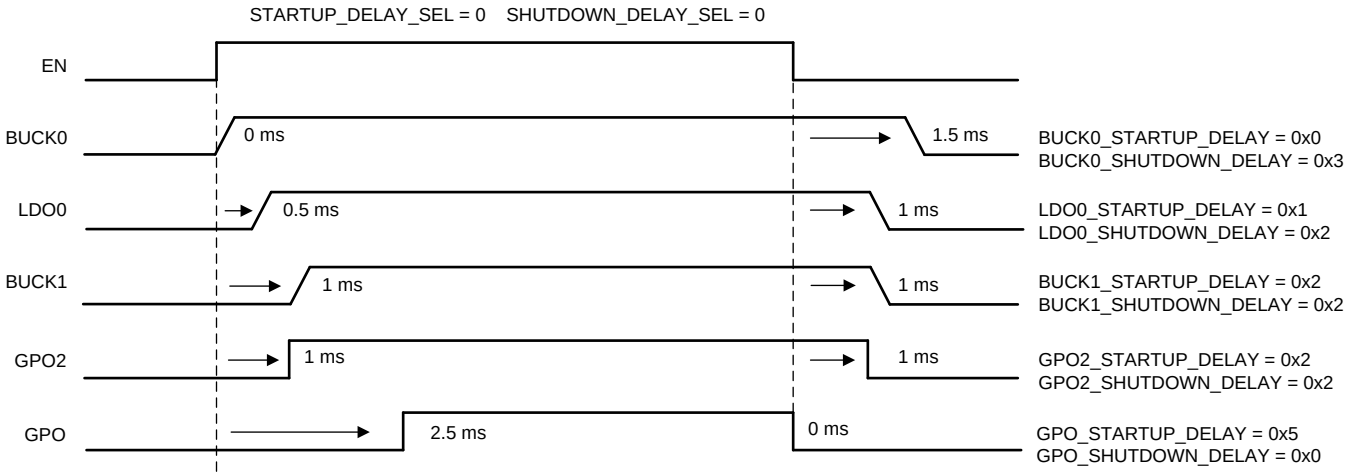

Figure 4. Startup and Shutdown Sequence Timing Diagram

3.3.8 Set EN_PIN_CTRL Bits

Each output can be controlled by either I^2C communication, or a combination of I^2C communication and the EN pin, as determined by the EN_PIN_CTRL bit of each output. When controlled by I^2C (EN_PIN_CTRL = 0) each output is turned on using their corresponding EN bits. When controlled using a combination of I^2C an the EN pin (EN_PIN_CTRL = 1), both the EN pin and the corresponding EN bit must be set high in order to turn on an output. By default the 0x00 OTP has the EN bit and EN_PIN_CTRL bit set low for each output. This prevents the EN pin from accidentally setting an output high, and lets the user choose which outputs to turn on with the EN pin.

When all of the other device settings have been set, the EN_PIN_CTRL bit should be set high for each output that needs to be turned on for the design, allowing the EN pin to control each desired output.

3.3.9 Set EN Bits

When the EN_PIN_CTRL bits are set high for each output that needs to be turned on for the design, the EN bits for each corresponding output can also be set high. It is important that the EN_PIN_CTRL bits are set before the EN bits so that no outputs are turned on accidentally. When the EN bits are set high the MCU should be finished with the required I^2C commands and can move on to clearing interrupts and setting the EN pin high as described in Section 3.1.

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