User's Guide
SNVU576C–September 2017–Revised November 2018

LP8733-Q1 and LP8732-Q1 User's Guide to Power DRA78x, and TDA3x

This user's guide can be used as a guide for powering DRA78x, and TDA3x with the LP8733-Q1 and LP8732-Q1 power devices.

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Trademarks

1 Introduction

This user's guide can be used as a guide for powering DRA78x, and TDA3x with LP8733-Q1 and LP8732-Q1 power devices.

This user's guide describes the platform connections as well as the power-up and power-down sequences along with the OTP configurations. This user's guide does not provide details about the power resources, external components, or the functionality of the device. For such information, refer to *LP87332A-Q1 Dual High-Current Buck Converter and Dual Linear Regulator* and *LP87322B/D/E/F-Q1 Dual High-Current Buck Converter and Dual Linear Regulator*.

In the event of any inconsistency between the official specification and any user's guide, application report, or other referenced material, the datasheet specification will be the definitive source.

2 Device Versions

Three OTP settings for LP8733-Q1 and LP8732-Q1 are described in this document. The LP87332A-Q1 device should be used with one LP87322x-Q1 device to power the DRA78x, or TDA3x processor based on DDR memory type, as shown in Table 1.

In addition, power solutions are available using TPS65919-Q1 or TPS65917-Q1 as described in the *TPS65919-Q1 and TPS65917-Q1 User's Guide to Power TDA3x*. See Table 1 to determine the recommended part number based on the DDR memory type and the Vdd_dspeve current requirement of the processor.

Texas Instruments recommends having 15% margin in the load current. Therefore the current requirements listed in Table 1 are 15% lower than the maximum capability of the regulator. If the Vdd_dspeve current in the application is unknown, select the TPS65919-Q1 configuration because it supports the maximum performance of the processors. For systems requiring functional safety, the TPS65919-Q1 and TPS65917-Q1 devices comply with applicable ISO 26262 ASIL-B requirements.

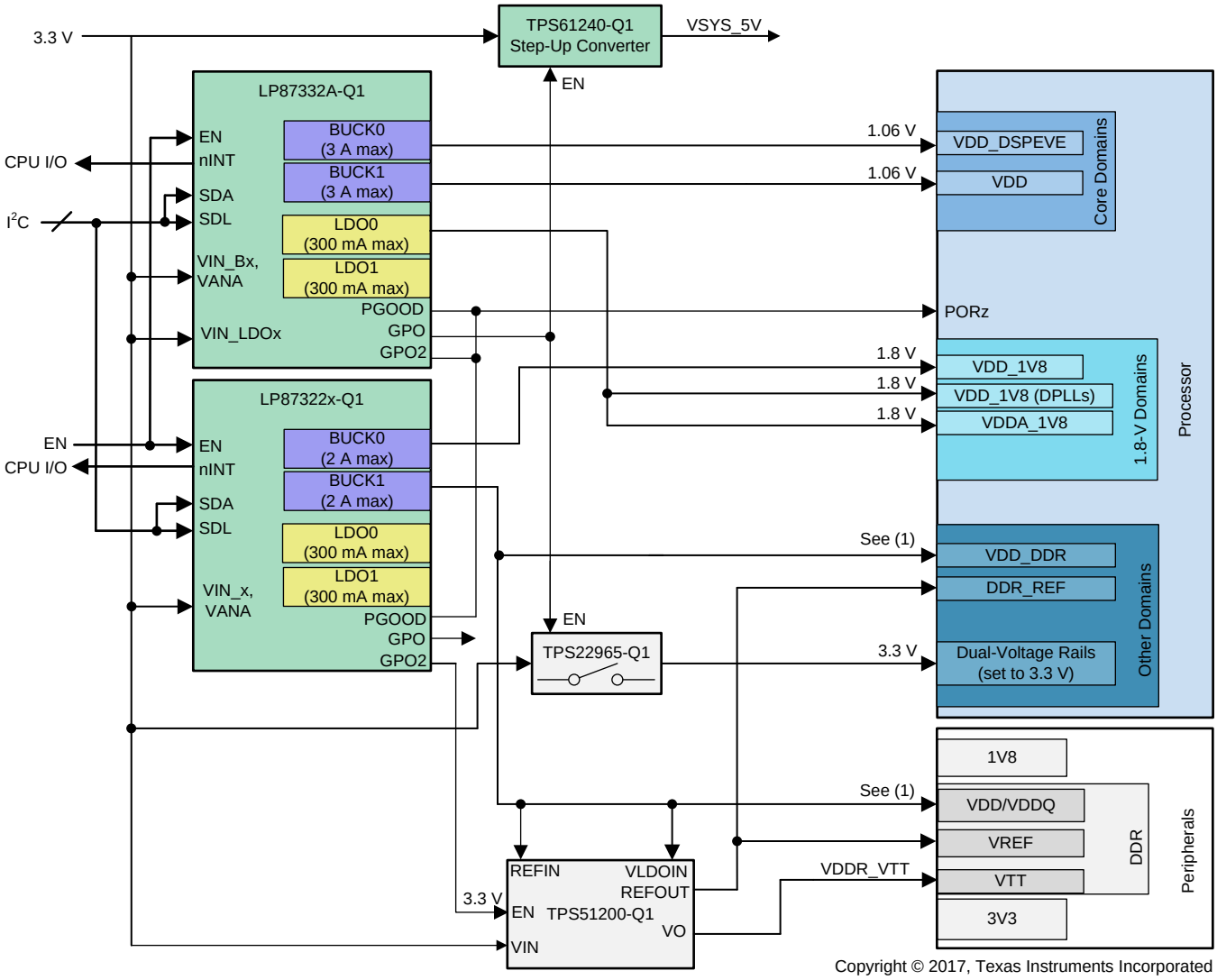
Table 1. OTP Settings Differentiation

DDR Memory Type	Vdd_dspeve Current Requirement	PMIC Selection	Content Of OTP_REV Register
DDR3L	Vdd_dspeve < 2.55 A	LP87332ARHDRQ1 + LP87322ERHDRQ1	0x2A, 0x2E
DDR3	Vdd_dspeve < 2.55 A	LP87332ARHDRQ1 + LP87322FRHDRQ1	0x2A, 0x2F
DDR3, DDR3L	Vdd_dspeve < 3 A	O919A152TRGZRQ1	See User's Guide
DDR3, DDR3L	Vdd_dspeve > 3 A	O917A152TRGZRQ1	

3 Platform Connection

shows the detailed connections between the processor and LP8733-Q1 and LP8732-Q1.

- PGOOD outputs of LP8733-Q1 and LP8732-Q1 are combined together with GPO2 of LP8733-Q1 to create PWR_PORz signal.
- GPO of LP8732-Q1 is available for system control, see Figure 1.



(1) See Table 2.

Figure 1. Processor Connection With LP8733-Q1 and LP8732-Q1

4 BOOT OTP Configuration

All LP8733-Q1 and LP8732-Q1 resource settings are stored in the form of registers. Therefore, all platform-related settings are linked to an action altering these registers. This action can be a static update (register initialization value) or a dynamic update of the register (either from the user or from a power sequence).

Resources and platform settings are stored in nonvolatile memory (OTP). These settings are defined as follows:

Static platform settings — These settings define, for example, BUCK or LDO default voltages, and GPIO functionality. Most static platform settings can be overwritten by a power sequence or by the user.

Sequence platform settings — These settings define the LP8733-Q1 and LP8732-Q1 power -up and power-down sequences. The power sequence is composed of several register accesses that define which resources (and the corresponding registers) must be updated during the respective state transition. The state of these resources can be overwritten by the user when the power sequence completes execution.

5 OTP Memory Configuration, Static Platform Settings

Each device has predefined values stored in OTP which control the default configuration of the device. The tables in this section list the OTP-programmed values for each device, distinguished by the OTP_REV. Power-up and power-down sequences are described in the next chapter.

Table 2 shows device settings for BUCK0 and BUCK1. Maximum allowed slew-rate for BUCKx depends on the output capacitance. BUCK1 of LP8732-Q1 is supply for memory where larger capacitance is expected to be used and because of ths slew-rate is set to lower value. Refer to the device data sheets for output capacitance boundary conditions.

Table 2. BUCK0 and BUCK1 OTP Settings

	Description	Bit Name	LP87332A	LP87322B	LP87322D	LP87322E	LP87322F	Notes
	Buck configuration		1 + 1	1 + 1	1 + 1	1 + 1	1 + 1	2-phase or 1 + 1
	Switching frequency		2 MHz	2 MHz	2 MHz	2 MHz	2 MHz	
	Buck force sink		No	No	No	No	No	Yes / No
	Spread spectrum	EN_SPREAD_SPEC	No	No	No	No	No	Yes / No
BUCK0	Output voltage	BUCK0_VSET	1.06 V	1.8 V	1.8 V	1.8 V	1.8 V	
	Enable, EN-pin or I²C register	BUCK0_EN_PIN_CTRL, BUCK0_EN	EN	EN	EN	EN	EN	EN or I²C
	Force PWM	BUCK0_FPWM	No	No	No	No	No	Yes / No
	Peak current limit	BUCK0_ILIM	4 A	3 A	3 A	3 A	3 A	
	Slew rate	BUCK0_SLEW_RATE	10 mV/µs	10 mV/µs	10 mV/µs	10 mV/µs	10 mV/µs	
BUCK1	Output voltage	BUCK1_VSET	1.06 V	1.2 V	1.8 V	1.35 V	1.5 V	
	Enable, EN-pin or I²C register	BUCK1_EN_PIN_CTRL, BUCK1_EN	EN	EN	EN	EN	EN	EN or I²C
	Force PWM	BUCK1_FPWM	No	No	No	No	No	Yes / No
	Peak current limit	BUCK1_ILIM	4 A	3 A	3 A	3 A	3 A	
	Slew rate	BUCK1_SLEW_RATE	10 mV/µs	7.5 mV/µs	7.5 mV/µs	7.5 mV/µs	7.5 mV/µs	

Table 3 lists the device settings for LDO0 and LDO1.

Table 3. LDO0 and LDO1 OTP Settings

	Description	Bit Name	LP87332A	LP87322B	LP87322D	LP87322E	LP87322F	Notes
LDO0	Output voltage	LDO0_VSET	1.8 V	1.0 V	1.0 V	1.0 V	1.0 V	
	Enable, EN-pin or I²C register	LDO0_EN_PIN_CTRL, LDO0_EN	EN	I²C	I²C	I²C	I²C	EN or I²C
LDO1	Output voltage	LDO1 _VSET	2.5 V	1.8 V	1.8 V	1.8 V	1.8 V	
	Enable, EN-pin or I²C register	LDO1_EN_PIN_CTRL, LDO1_EN	I²C	I²C	I²C	I²C	I²C	EN or I²C

Table 4 lists the device settings for GPIOs.

Table 4. EN, CLKIN and GPIO Pin Settings

	Description	Bit Name	LP87332A	LP87322B	LP87322D	LP87322E	LP87322F	Notes
EN pin	EN pin pulldown resistor enable or disable	EN_PD	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled / disabled

Table 4. EN, CLKIN and GPIO Pin Settings (continued)

	Description	Bit Name	LP87332A	LP87322B	LP87322D	LP87322E	LP87322F	Notes
CLKIN pin	CLKIN or GPO2 mode selection	CLKIN_PIN_SEL	GPO2	GPO2	GPO2	GPO2	GPO2	
	CLKIN pin pulldown resistor enable or disable (applicable for both CLKIN and GPO2 modes)	CLKIN_PD	Disabled	Disabled	Disabled	Disabled	Disabled	Enabled / disabled
	Frequency of external clock when connected to CLKIN	EXT_CLK_FREQ	2 MHz	2 MHz	2 MHz	2 MHz	2 MHz	
	Enable for the internal PLL. When PLL disabled, internal RC OSC is used	EN_PLL	Disabled	Disabled	Disabled	Disabled	Disabled	Enabled / disabled
GPO	GPO output type	GPO_OD	OD	OD	OD	OD	OD	PP / OD
	Enable, EN-pin or I^{2}C register	GPO_EN_PIN_CTRL, GPO_EN	EN	EN	EN	EN	EN	
GPO2	Control for GPO	GPO_EN	High	High	High	High	High	Low / High
	GPO2 output type	GPO2_OD	OD	OD	OD	OD	OD	PP / OD
	Enable, EN-pin or I^{2}C register	GPO2_EN_PIN_CTRL	EN	EN	EN	EN	EN	EN or I^{2}C
	Control for GPO2	GPO2_EN	High	High	High	High	High	Low / High

Table 5 shows device settings for PGOOD.

Table 5. PGOOD OTP Settings

	Description	Bit Name	LP87332A	LP87322B	LP87322D	LP87322E	LP87322F	Notes
Signals monitored by PGOOD	BUCK0 output voltage	EN_PGOOD_BUCK0	Yes	Yes	Yes	Yes	Yes	Yes / No
	BUCK1 output voltage	EN_PGOOD_BUCK1	Yes	Yes	Yes	Yes	Yes	Yes / No
	LDO0 output voltage	EN_PGOOD_LDO0	Yes	No	No	No	No	Yes / No
	LDO1 output voltage	EN_PGOOD_LDO1	No	No	No	No	No	Yes / No
	Thermal warning	EN_PGOOD_TWARN	Yes	Yes	Yes	Yes	Yes	Yes / No
PGOOD mode selections	PGOOD thresholds for BUCK0, BUCK1	PGOOD_WINDOW_BUCK	Window	Window	Window	Window	Window	Undervoltage / Window (undervoltage and overvoltage)
	PGOOD thresholds for LDO0, LDO1	PGOOD_WINDOW_LDO	Window	Window	Window	Window	Window	Undervoltage / Window (undervoltage and overvoltage)
	PGOOD operating mode	PGOOD_MODE	Detecting UNUSUAL situations	Detecting UNUSUAL situations	Detecting UNUSUAL situations	Detecting UNUSUAL situations	Detecting UNUSUAL situations	UNUSUAL / UNVALID
	PGOOD signal mode	PG_FAULT_GATES_PGOOD	Status	Status	Status	Status	Status	Status / Latched until fault source read
	PGOOD output mode	PGOOD_OD	OD	OD	OD	OD	OD	OD / PP
	PGOOD polarity	PGOOD_POL	Active high	Active high	Active high	Active high	Active high	Active (power valid) high / low

Table 6 lists the device settings for thermal warning. Also refer to for PGOOD and for interrupts.

Table 6. Protections OTP Settings

	Description	Bit Name	LP87332A	LP87322B	LP87322D	LP87322E	LP87322F	Notes
Protections	Thermal warning level	TDIE_WARN_LEVEL	137°C	137°C	137°C	137°C	137°C	125°C or 137°C
	Input overvoltage protection	(Hidden from customer, always enabled)	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled / disabled

Table 7 shows device settings for I^{2}C and OTP revision ID values.

Table 7. Device Identification and I²C Settings

	Description	Bit Name	LP87332A	LP87322B	LP87322D	LP87322E	LP87322F	Notes
I²C address			0x60	0x61	0x61	0x61	0x61	
I2C speed default	Set Hs-mode I²C by default		No	No	No	No	No	Yes / No
DEVICE_ID	Device specific ID code	DEVICE_ID	0x0	0x1	0x1	0x1	0x1	
OTP_ID	Identification code for OTP version	OTP_ID	0x2A	0x2B	0x2D	0x2E	0x2F	

Table 8 lists device settings for interrupts. When interrupt from an event is unmasked, an interrupt is generated to nINT pin.

Table 8. Interrupt Mask Settings

	Interrupt event	Bit Name	LP87332A	LP87322B	LP87322D	LP87322E	LP87322F	Notes
General	PGOOD pin changing active to inactive	PGOOD_INT_MASK	Masked	Masked	Masked	Masked	Masked	Masked / Unmasked
	Sync clock appears or disappears	SYNC_CLK_MASK	Masked	Masked	Masked	Masked	Masked	Masked / Unmasked
	Thermal warning	TDIE_WRN_MASK	Unmasked	Unmasked	Unmasked	Unmasked	Unmasked	Masked / Unmasked
	Load measurement ready	I_MEAS_MASK	Unmasked	Unmasked	Unmasked	Unmasked	Unmasked	Masked / Unmasked
	Register reset	RESET_REG_MASK	Masked	Masked	Masked	Masked	Masked	Masked / Unmasked
BUCK0	Buck0 PGood active	BUCK0_PGR_MASK	Masked	Masked	Masked	Masked	Masked	Masked / Unmasked
	Buck0 PGood inactive	BUCK0_PGF_MASK	Masked	Masked	Masked	Masked	Masked	Masked / Unmasked
	Buck0 current limit	BUCK0_ILIM_MASK	Unmasked	Unmasked	Unmasked	Unmasked	Unmasked	Masked / Unmasked
BUCK1	Buck1 PGood active	BUCK1_PGR_MASK	Masked	Masked	Masked	Masked	Masked	Masked / Unmasked
	Buck1 PGood inactive	BUCK1_PGF_MASK	Masked	Masked	Masked	Masked	Masked	Masked / Unmasked
	Buck1 current limit	BUCK1_ILIM_MASK	Unmasked	Unmasked	Unmasked	Unmasked	Unmasked	Masked / Unmasked
LDO0	LDO0 PGood active	LDO0_PGR_MASK	Masked	Unmasked	Unmasked	Unmasked	Unmasked	Masked / Unmasked
	LDO0 PGood inactive	LDO0_PGF_MASK	Masked	Unmasked	Unmasked	Unmasked	Unmasked	Masked / Unmasked
	LDO0 current limit	LDO0_ILIM_MASK	Unmasked	Unmasked	Unmasked	Unmasked	Unmasked	Masked / Unmasked
LDO1	LDO1 PGood active	LDO1_PGR_MASK	Unmasked	Unmasked	Unmasked	Unmasked	Unmasked	Masked / Unmasked
	LDO1 PGood inactive	LDO1_PGF_MASK	Unmasked	Unmasked	Unmasked	Unmasked	Unmasked	Masked / Unmasked
	LDO1 current limit	LDO1_ILIM_MASK	Unmasked	Unmasked	Unmasked	Unmasked	Unmasked	Masked / Unmasked

6 OTP Memory Configuration, Power-Up and Power-Down Sequence Settings

A power sequence is an automatic preprogrammed sequence handled by the LP8733-Q1 and LP8732-Q1 devices to configure the device resources: BUCKs, LDOs and GPOs into ON or OFF state.

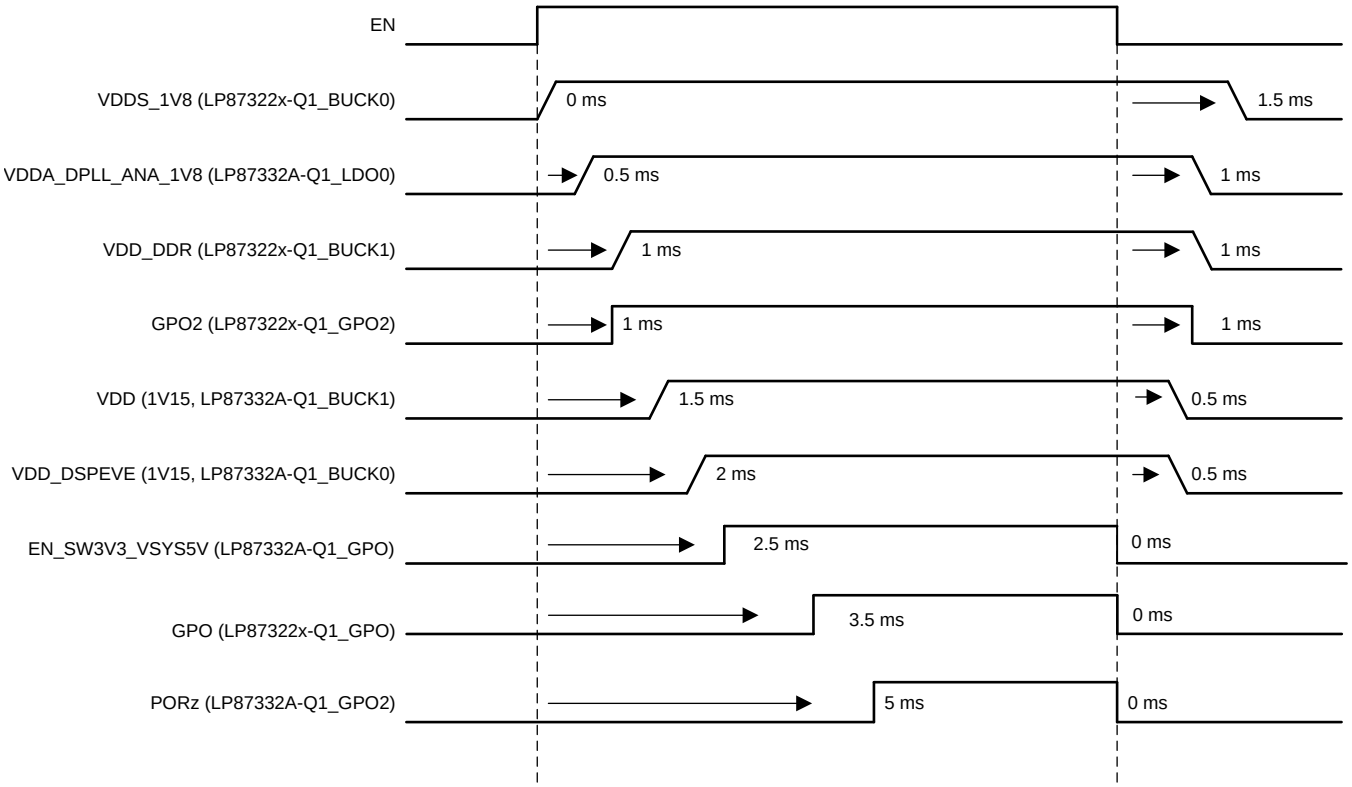


Figure 2. Power-Up and Power-Down Sequence

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (December 2017) to B Revision	Page

Changes from Original (September 2017) to A Revision **Page**

- Added TPS65917-Q1 and TPS65919-Q1 solution information and link to user's guide 2

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