Application Note

Design Guide for Inverting Buck-Boost for OLED Panel Applications Using LM61495

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ABSTRACT

This application note describes design considerations to achieve Inverting Buck-Boost (IBB) topology using standard buck converter for display applications especially OLED panel. OLED panel normally requires positive and negative voltage power rails which is called ELVDD and ELVSS to light OLED. To make the design simple, it is common to implement IBB topology using standard buck converter to source negative voltage also considering PCB size, BOM cost. This application note uses the TI's reference design PMP23333 using LM61495. LM61495 can operate under a wide input voltage range for 3V to 36V and 10A load capability which is good enough to design IBB converter for OLED panel. This design is not only limited to OLED panel applications but also telecom application or other applications requiring negative output power.

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1 OLED Driving Scheme

OLED (Organic Lighting-Emitting Diode) is made by organic materials that emit light when current is applied. Each pixel can emit light, so OLED does not have a problem of light from backlight leaking through the display. The basic structure of OLED pixel is shown in Figure 1-1. Scan line is used for pixel selection to turn on T1 to allow data to be written to T2. Vg from Data line can control the gray scale. Data storage capacitor keeps Vg constant during frame time. In general, driving OLED requires bipolar voltage rails like ELVDD(Positive), ELVSS(Negative). Once T2 is turned on, current can be driven from ELVDD(Positive) to ELVSS(Negative). The luminous brightness is adjusted by changing the voltage across OLED.

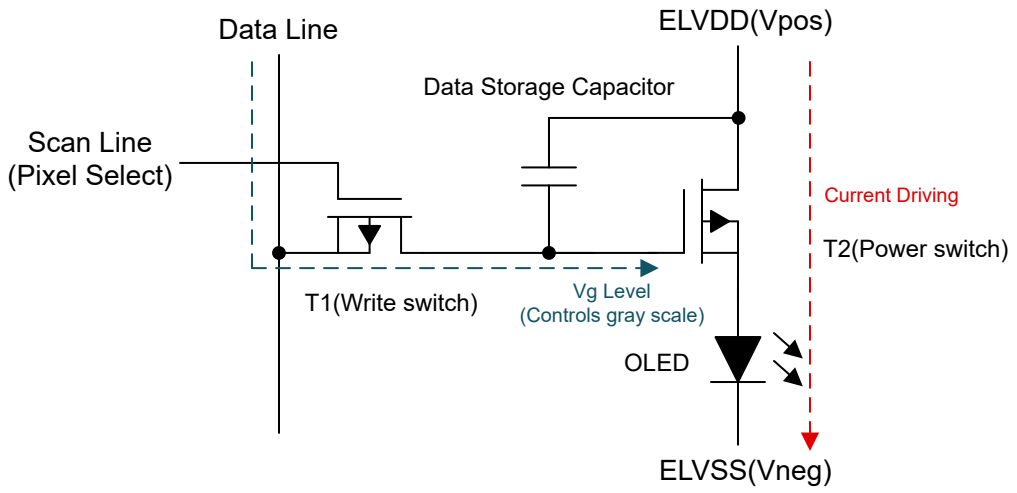

Figure 1-1. Basic Structure of OLED Pixel

Simply the ground can be used for ELVSS rather than negative output voltage. But recently, the panel makers use negative output voltage for ELVSS to minimize flickering issue. Most applications using OLED panel such as monitors support VRR (Variable Refresh Rate) feature to synchronize the display refresh rate with the video input frame rate. VRR can eliminate the stuttering or tearing of the image and enable smooth display of the source. However, as the refresh rate is changed within VRR range such as 30Hz – 140Hz, the charging speed of data line can be impacted. This changes the charging level of the data storage capacitor, which can cause the current of OLED to be changed accordingly. VRR causes the luminance to vary depending on the frequency (refresh rate) even though the same luminance is the target. This phenomenon has been considered as the flickering issue by users. To prevent and minimize this flickering issue, ELVDD voltage level or internal compensation circuit of OLED can be tuned. But it is sometimes limited and complex. So this becomes popular to simply use negative output voltage for ELVSS to minimize the flickering issue. The voltage level is decided by the characteristics of OLED and internal compensation circuit. Therefore, the requirement of panel makers is very important.

The power supply for ELVDD and ELVSS need to have sufficient current capability to drive OLED pixels. Higher current capability is required if OLED panel size is bigger which can contain more pixels. This means negative output power also need to cover high current capability as much positive output power can do. Therefore inverting buck-boost for negative voltage become popular than charge pump design which has limited current capability. Also IBB design can help designer achieve lower BOM cost and small PCB size design.

2 Inverting Buck-Boost Concept

For the standard buck converter, the inductor is connected to V_{OUT} and the switch pin (SW). To change a standard buck converter to an inverting buck-boost, reassign the buck converter V_{OUT} to system ground, and the old buck system ground to - V_{OUT}. The input capacitor needs to be reconnected to the new system ground, and a new bypass capacitor, C_{IO}, is needed between V_{IN} and -V_{IN}.

The positive input and the feedback resistors remains the same as in the buck converter. To adjust the output of the inverting buck-boost, calculate the feedback resistor values as if the feedback resistor was a buck converter. The schematics in Figure 2-1 show the changes that have to be made when configuring the standard buck converter as an inverting buck-boost converter. This inverting topology allows the output voltage to be inverted and always lower than the ground.

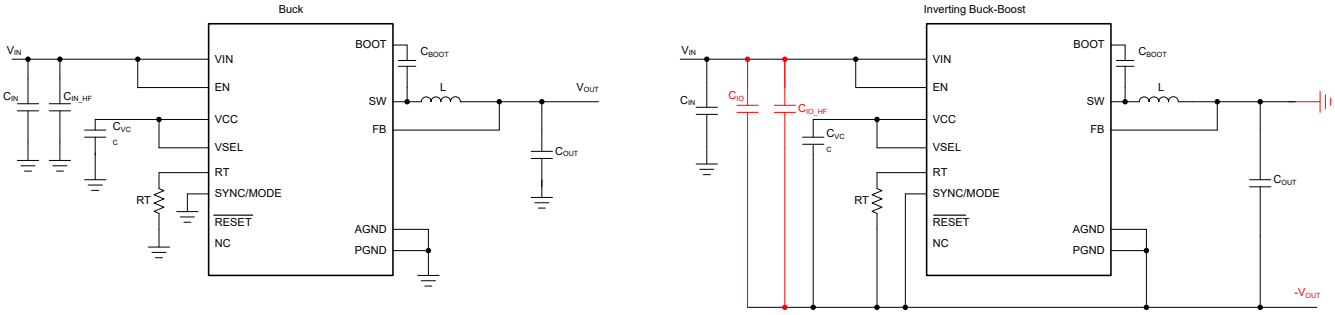

Figure 2-1. Converting From Buck to Inverting Buck-Boost Topology

The circuit operation is different in the inverting buck-boost topology than in the buck topology. Figure 2-2 shows that the output voltage terminals are reversed, though the components are wired the same as a buck converter. As Figure 2-3 shows, during the ON-time of the control MOSFET, the inductor is charged with current while the output capacitor supplies the load current. The inductor does not provide current to the load during this time.

During the OFF-time of the control MOSFET and the ON-time of the synchronous MOSFET shown in Figure 2-4, the inductor provides current to the load and the output capacitor. These changes affect many parameters, which the following subsections describe in further detail.

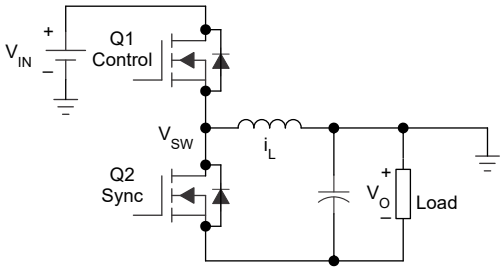

Figure 2-2. Inverting Buck-Boost Configuration

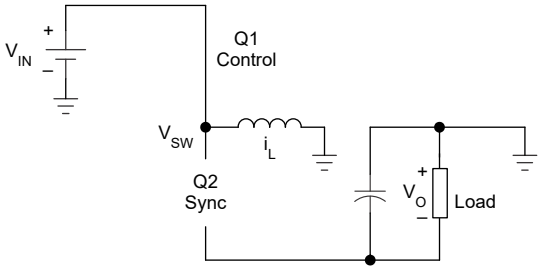

Figure 2-3. ON-Time of IBB Configuration

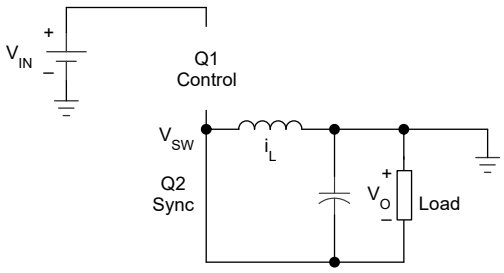

Figure 2-4. OFF-Time of IBB Configuration

3 PMP23333 Introduction

This application note uses TI's reference design PMP23333. PMP23333 design used LM61495 synchronous buck regulator, with internal top and bottom FETs, which is configured as a synchronous inverting buck-boost converter. The LM61495 is regulator that provide either fixed or adjustable output voltage that can be set from 1V to 95% of expected input voltage. LM61495 can operate under a wide input voltage range from 3V to 36V and have transient tolerance up to 42V which can give proper design flexibility to designers.

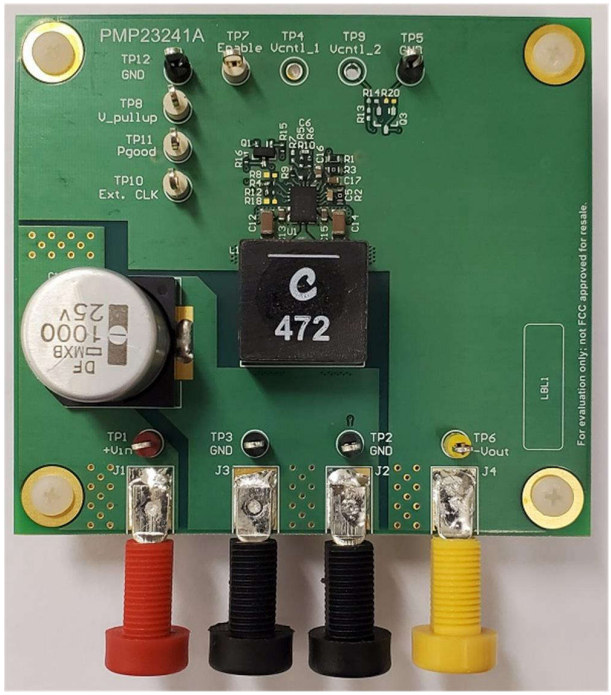

Figure 3-1. PMP23333 (Top) Board Image

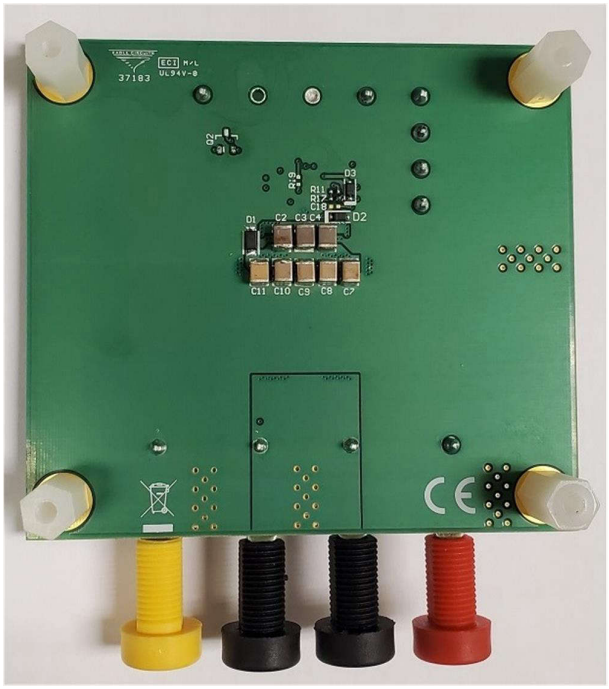

Figure 3-2. PMP23333 (Bottom) Board Image

Table 3-1. Voltage and Current Requirements of PMP23333

Parameter	Specifications
V_{IN}	12 VDC ±10%
V_{OUT}	–8 VDC
I_{OUT}	2.7A continuous (4A peak)
F_{SW}	400kHz nominal

This design generates an output of –8V, capable of delivering 2.7A continuous (4A peak) of current to the load, from a +12V, ±10% input. The design covers up to 32W power rating. So PMP23333 can be a great start point of design to cover up to 49 inch OLED panel for monitor, small TV applications. As described in Section 1, $-V_{OUT}$ can be decided by OLED characteristics. $-V_{OUT}$ value can be set by configuration of feedback resistors as shown in Figure 3-3, PMP23333 schematic. If designer requires higher power rating for bigger OLED panel, controller design needs to be considered due to current, thermal limitations, and so on.

3.1 PMP23333 Schematic

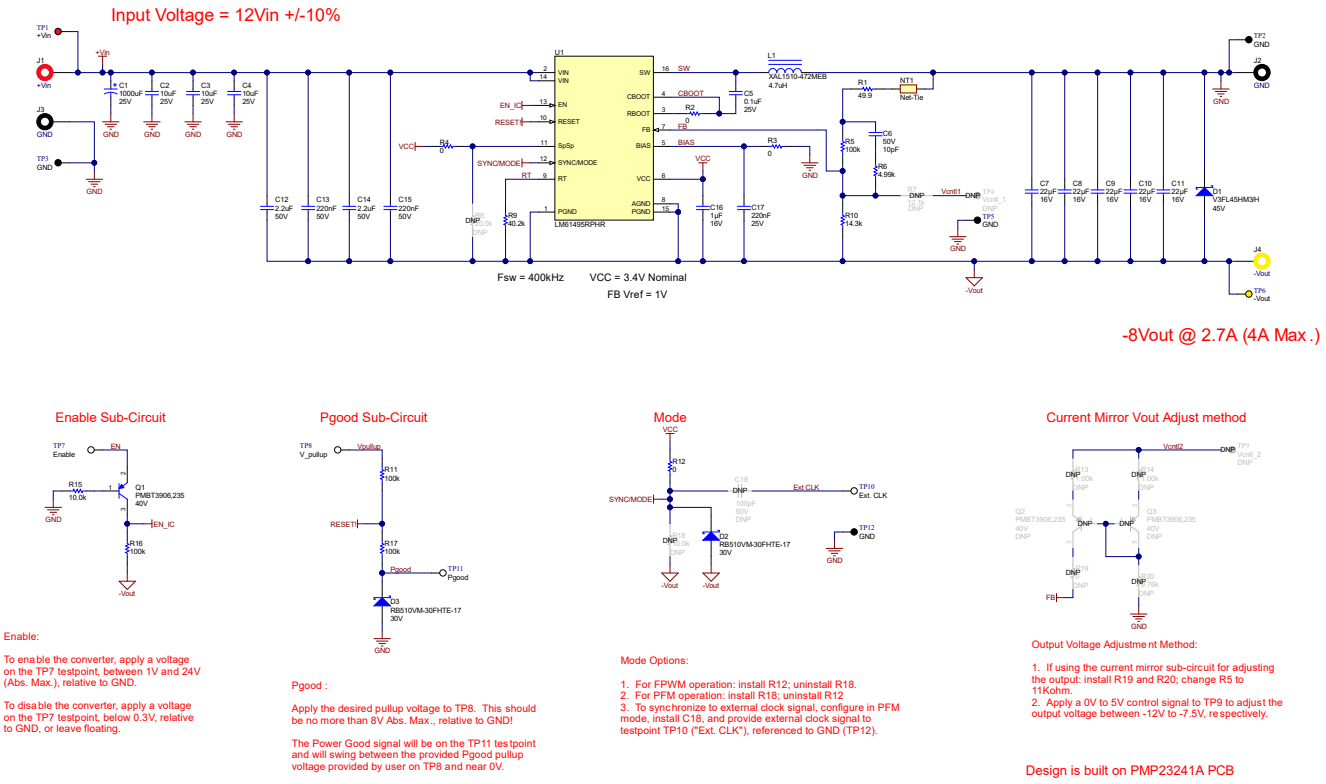

Figure 3-3. PMP23333 Schematic

4 Design Considerations

4.1 VIN, VOUT Range

The input voltage that can be applied to an integrated circuit (IC) operating in the inverting buck-boost topology is less than the input voltage for the same IC operating in the buck topology. The reason for this difference is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is V_{IN} to V_{OUT}, not V_{IN} to ground. Thus, the input voltage range which needs to be considered for this design is 13.2V – (– 8V) = 21.2V.

LM61495 is good enough to cover 21.2V input voltage range since LM61495 can cover up to 36V. The output voltage range is the same as when configured as a standard buck converter, but negative. The output voltage for the inverting buck-boost topology must be set between 1V and 95% of expected input voltage following LM61495 specification. At this time, expected input voltage for LM61495 can be V_{IN} – (– V_{OUT}) for IBB implementation

The output voltage is set in the same way as the buck configuration, with two resistors connected to the FB pin. This design sets the output voltage at –8V, which gives an input voltage range of 21.2V. LM61495 uses a 1V reference for control to derive Equation 1. This equation can be used to determine R_{FBB} for a desired output voltage and a given R_{FBT}. In this design, R_{FBT} = 100kohm. Therefore R_{FBB}= 14.3k to set –V_{OUT} = -8V.

$$R_{FBB} = \frac{R_{FBT}}{V_{OUT} - 1} \quad (1)$$

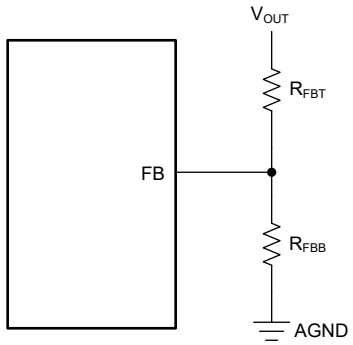

Figure 4-1. Setting Output Voltage of Adjustable Versions

4.2 Inductor Selection and Maximum Output Current

The average inductor current is affected in this topology. In the buck configuration, the average inductor current is equal to the average output current because the inductor always supplies current to the load during both the ON- and OFF-times of the control MOSFET. However, in the inverting buck-boost configuration, only the output capacitor supplies the load with current, while the load is completely disconnected from the inductor during the ON-time of the control MOSFET. During the OFF-time, the inductor connects to both the output capacitor and the load (see Figure 2-2 to Figure 2-4). Because the OFF-time is 1 – D of the switching period, the average inductor current in Equation 2 is calculated as:

$$I_{L(Avg)} = \frac{I_{OUT}}{(1 - D)} \tag{2}$$

The duty cycle for the typical buck converter is simply V_{OUT} / (V_{IN} × η), but the calculation of the duty cycle in Equation 3 for an inverting buck-boost converter becomes:

$$D = \frac{|V_{OUT}|}{|V_{OUT}| + (V_{IN} \times \eta)} \tag{3}$$

Equation 4 provides the peak-to-peak inductor ripple current:

$$\Delta I_L = \frac{V_{IN} \times D}{f_S \times L} \tag{4}$$

where,

- ΔI_L (A): Peak-to-peak inductor ripple current
- D: Duty cycle
- f_S (Hz): Switching frequency
- L (H): Inductor value
- V_{IN} (V): Input voltage with respect to ground, not with respect to the device ground or V_{OUT}

In the inverting buck-boost topology, the maximum output current is reduced as compared to the buck topology. This reduction is a result of the peak inductor current being higher.

The inductor for the IBB is selected based on the desired ripple current, much like any other DC/DC converter. Typically a value of between 20% and 40% of the load current is used for ΔI_L. Equation 5 can be derived by Equation 4 to determine the value of L along with the maximum inductor current. This information is used to select a standard inductor that is designed for the application.

$$L = \frac{VIN}{f_S \times \Delta I_L} \times \frac{|V_{OUT}|}{|V_{OUT}| + (VIN \times \eta)} \tag{5}$$

4.7µH inductor is selected in PMP23333 design. For an output voltage of – 8V and input voltage of + 12V ± 10%, the following calculations produce the maximum allowable output current that can make sure is based on the LM61495 minimum valley current limit value of 9.8A which is described in the data sheet. Due to increased duty cycles when operating at high load current, the duty cycle used for the following maximum output current calculation in Equation 6 be increased by 5% for these conditions, which provides a more accurate maximum output current calculation.

$$D = \frac{|V_{OUT}|}{|V_{OUT}| + (VIN \times \eta)} \times 1.05 = \frac{8}{8 + (10.8 \times 0.9)} \times 1.05 = 0.47 \tag{6}$$

$$\Delta I_L = \frac{VIN \times D}{f_S \times L} = \frac{10.8 \times 0.47}{400kHz \times 4.7\mu H} = 2.7A \tag{7}$$

$$I_{L(Avg)} = \frac{I_{OUT}}{(1 - D)} = \frac{4}{(1 - 0.47)} = 7.547A \tag{8}$$

$$I_{L(Peak)} = I_{L(Avg)} + \frac{\Delta I_L}{2} = 8.897A \quad (9)$$

$$I_{L(Valley)} = I_{L(Avg)} - \frac{\Delta I_L}{2} = 6.197A \quad (10)$$

Figure 4-2 and Figure 4-3 shows the switching voltage and inductor current waveforms under - 2.7A, - 4A load conditions and shows that the calculation almost matches with real values.

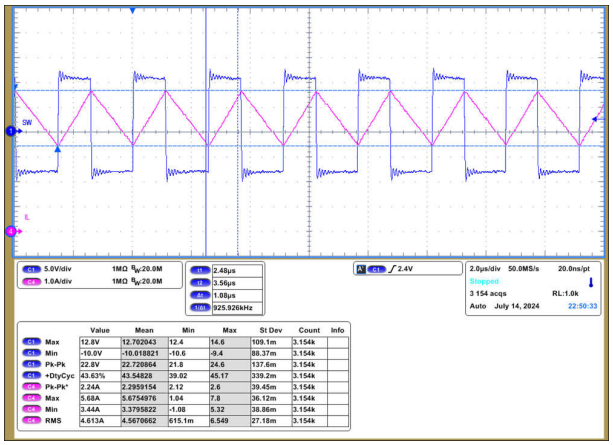

Figure 4-2. SW and IL Waveforms Under I_{OUT} = - 2.7A

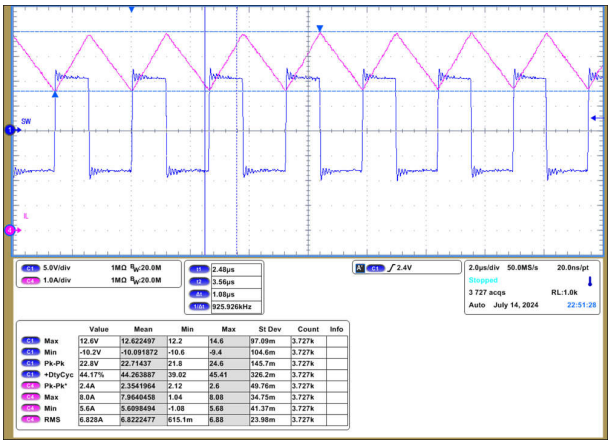

Figure 4-3. SW and IL Waveforms Under I_{OUT} = - 4A

To calculate allowable maximum current, $I_{L(Valley)}$ needs to be less than 9.8A as shown in Equation 11. Therefore, I_{OUT_MAX} needs to be less than 5.9A as calculated in Equation 12. Even though, I_{OUT_MAX} can be increased to 5.9A, Texas Instruments does not recommend to use higher load than 4A in this design since the higher load can cause IC thermal rising significantly.

$$I_{L(Avg)} - \frac{\Delta I_L}{2} = \frac{I_{OUT\_MAX}}{(1-D)} - \frac{\Delta I_L}{2} = \frac{I_{OUT\_MAX}}{0.53} - 1.35A < 9.8A \quad (11)$$

$$I_{OUT\_MAX} < 5.9A \quad (12)$$

4.3 Capacitor Selection

Figure 4-4 shows how capacitors are placed for both input and output side of IBB converter. The input capacitor, C_{IN} is required to provide a low-impedance input voltage source to the converter. A low equivalent series resistance (ESR) X5R or X7R ceramic capacitor is best for input voltage filtering and minimizing interference with other circuits. As shown in Figure 3-3, PMP23333 uses 3 x 10µF ceramic capacitors (C2, C3, C4) from V_{IN} to ground (system ground, not $–V_{OUT}$). Note that C1 is only used for validation. The C_{IN} capacitor value can be increased without any limit for better input voltage filtering.

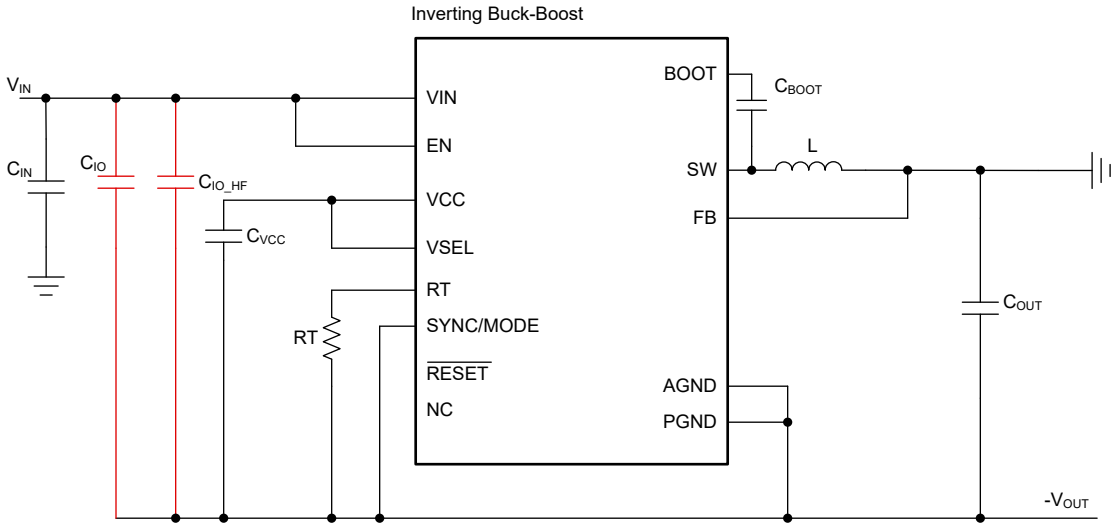

Figure 4-4. Inverting Buck-Boost with Additional Capacitors C_{IO}, C_{IO_HF}

There is importance to place new bypass capacitors C_{IO}, C_{IO_HF} for IBB topology to provide a low impedance source for the internal gate drivers. C_{IO}, C_{IO_HF} can be connected from V_{IN} to $-V_{OUT}$. Therefore, the capacitors must be properly sized for the voltage difference between V_{IN} and $-V_{OUT}$. The values for the bypass capacitance, C_{IO}, C_{IO_HF} can be chosen using input capacitance recommendations from the buck converter data sheet. These bypass capacitors provide an AC path from V_{IN} to $-V_{OUT}$. When V_{IN} is applied to the circuit, this dV/dt across the capacitor from V_{IN} to $-V_{OUT}$ creates a current that must return to ground (the return of the input supply) to complete the loop.

PMP23333 uses 2 x 2.2uF, 2 x 220nF (C12 approximately C15) as input bypass capacitors. As shown in Figure 4-5 to Figure 4-10, installing bypass capacitors can reduce the input, output voltage ripple and improve the transient response. Without the bypass capacitors, the converter cannot filter the switching noise which is around 400kHz in PMP2333 design. It also causes worse transient performance which can impact to the system. Therefore, installing proper C_{IO}, C_{IO_HF} can reduce the size of C_{IN}, C_{OUT} with optimization.

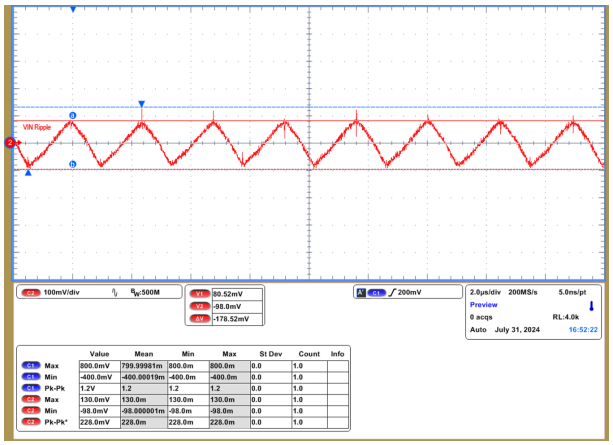

Figure 4-5. V_{IN} Ripple Waveform With C12 - C15

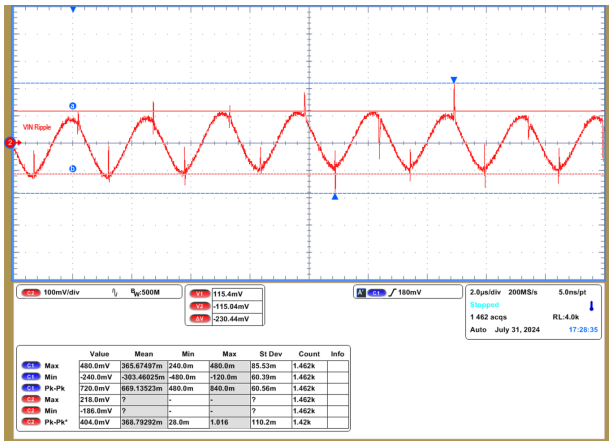

Figure 4-6. V_{IN} Ripple Waveform Without C12 - C15

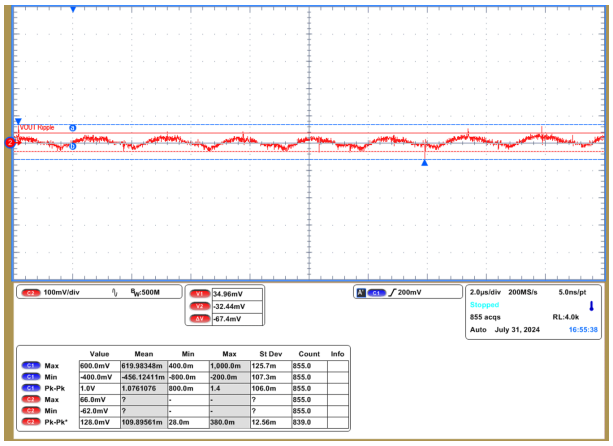

Figure 4-7. V_{OUT} Ripple Waveform With C12 - C15

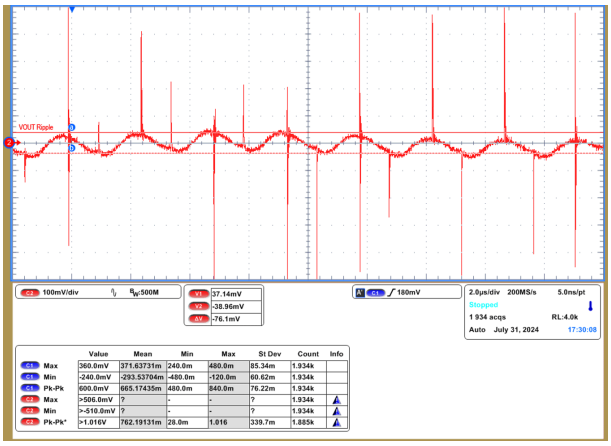

Figure 4-8. V_{OUT} Ripple Waveform Without C12 - C15

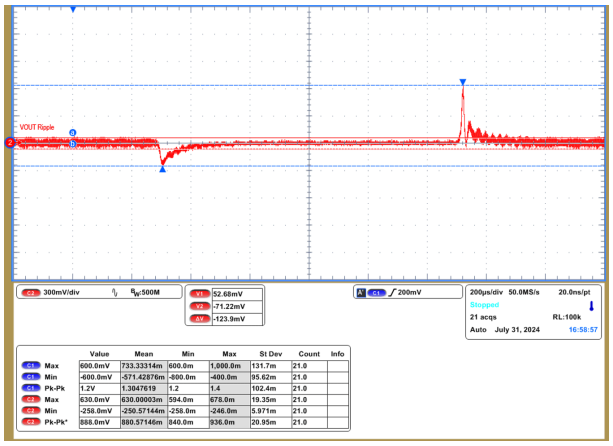

Figure 4-9. V_{OUT} Transient Waveform (0-2.7A) With C12 - C15

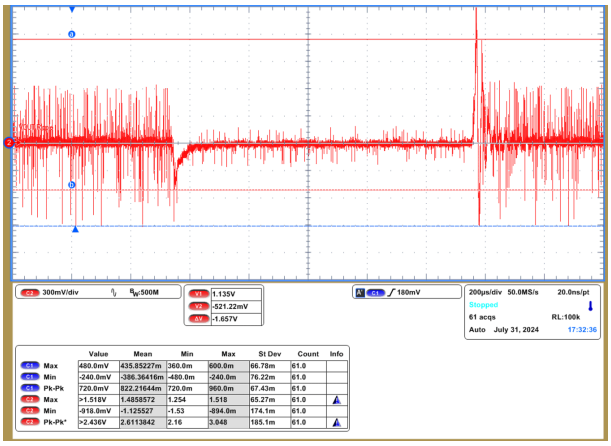

Figure 4-10. V_{OUT} Transient Waveform (0-2.7A) Without C12 - C15

In IBB converter, the output current is discontinuous. The output capacitors supply energy to the load during the on time when energy stored in the inductor is increasing. During the off time, the inductor is delivering energy to both load and the output capacitors. The output capacitance can also follow buck converter data sheet recommendation. PMP23333 uses 5 x 22uF. The output capacitance can be increased or reduced by the output ripple and transient requirements.

4.4 Efficiency and Thermal Considerations

As described in previous sections so far, the power loss of IBB converter can be greater than the standard buck converter due to larger voltage and current stresses. This means that the efficiency of the IBB can be less than that of a buck under similar conditions. Estimating the efficiency before the IBB is designed and tested is not easy. Therefore, the best plan is to take a conservative approach to calculating the maximum operating currents when choosing a buck converter.

The increased power dissipation compared to the standard buck converter also has consequences for increasing die temperature. Every regulator has a maximum rated die temperature that must not be exceeded. Since the IBB has more dissipation than the equivalent buck, the extra heat needs to be removed or the die temperature can get too high. This means that the total θ_{JA} of the application can have to be lowered.

The maximum allowed IC junction temperature is 150°C as stated in the LM61495 data sheet. To calculate the IC temperature for different conditions, multiply the power loss of the LM61495 device by the θ_{JA} of PMP23333 PCB, and add this value to the ambient temperature. Since PMP23333 does not specify the θ_{JA} of PCB, we can estimate the θ_{JA} by checking actual efficiency and thermal results. Figure 4-11 and Figure 4-12 show the thermal results under - 2.7A, - 4A conditions when V_{IN} = 12V, V_{OUT} = -8V. Even though higher load can be used like described in Section 4.2 Texas Instruments does not recommend to increase the load more than – 4A in PMP23333 design since IC temperature can get to be too high.

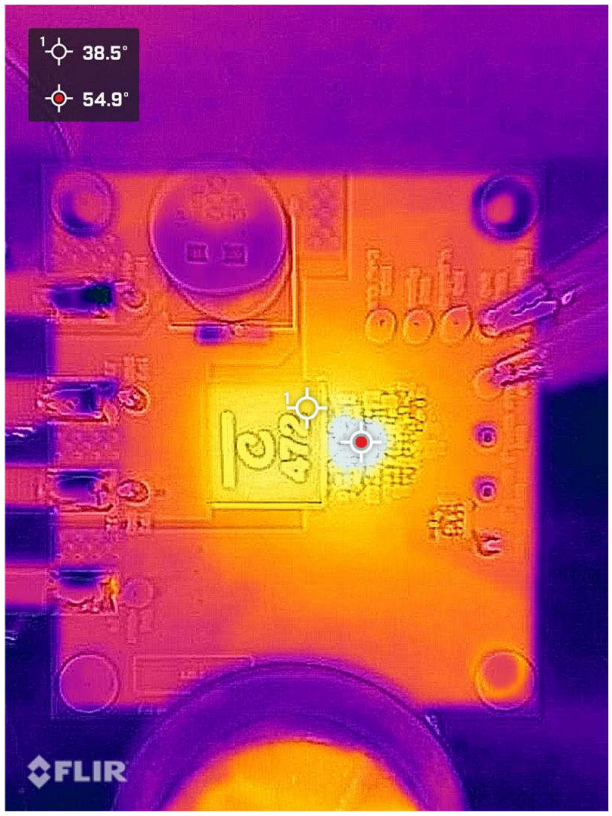

Figure 4-11. Thermal Result When I_{OUT} = - 2.7A

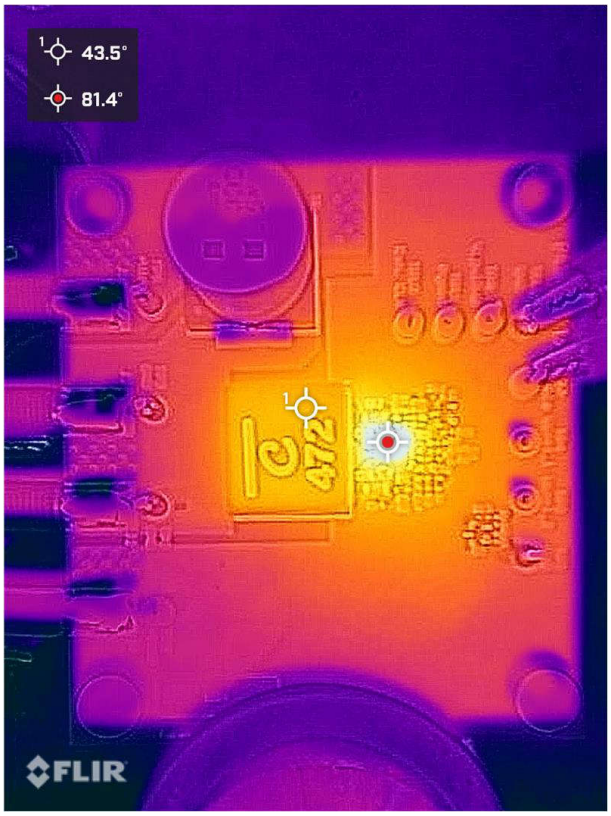

Figure 4-12. Thermal Result When I_{OUT} = - 4A

4.5 Optional Enable (EN) Level Shifter

Since the ground of the buck converter IC is now referenced to the negative output voltage, a level shifter is required if a control signal is to be used on the enable pin. An example circuit is shown in Figure 4-13 that can be used to level shift an incoming enable signal. While the circuit requires two transistors, the circuit has no hysteresis and requires no current from the control signal. If the enable pin is not rated for the full input voltage range, then a Zener diode must be used to clamp the enable pin below the maximum voltage. The enable pin needs to be configured properly even without a control signal, and the buck converter data sheet can be referenced for the proper connection of the EN pin.

When the enable signal is pulled low, then the NMOS switch is turned off, pulling the gate of the PMOS to VIN. The PMOS then turns off, pulling the enable pin below the high-level threshold. When the enable signal is pulled high, the NMOS switch is turned on, pulling the gate of the PMOS low. The PMOS then turns on, pulling the enable pin above the high level threshold from VIN.

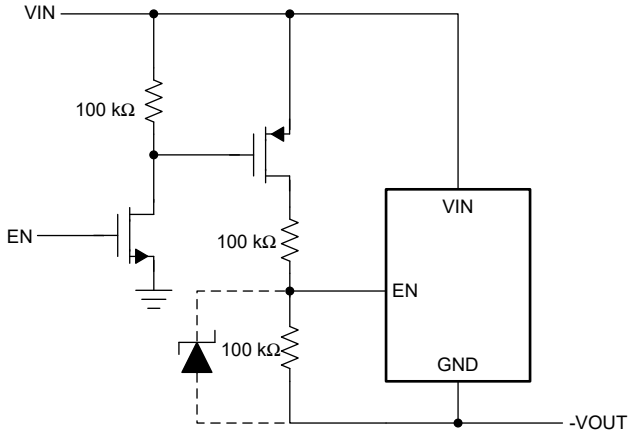

Figure 4-13. EN Pin Level Shifter

5 Summary

Due to the trend of using negative output voltage for ELVSS power rail in OLED panel, Inverting Buck-Boost (IBB) topology gets more common for the applications such as monitor, TV using OLED panel. This application note addresses the key design considerations to achieve IBB topology using standard buck converter. TI reference design PMP23333, *Synchronous Inverting Buck-Boost Converter Reference Design for Communications Equipment* using L61495 is utilized. LM61495 is a good option for IBB design since LM61495 can operate under a wide input voltage range from 3V to 36V and have transient tolerance up to 42V which can give proper design flexibility to designers. Designers can refer to this application note as a start point to design the IBB converter. This application note is not only limited to OLED panel applications but also telecom application or other applications requiring negative output power.

6 References

- Texas Instruments, *Working With Inverting Buck-Boost Converters,* application note.
- Texas Instruments, *Inverting Buck-Boost Application for the LM63615-Q1,* application note.
- Texas Instruments, *LM62460, LM61480, and LM61495 Pin-Compatible 6-A/8-A/10-A Buck Converter Optimized for Power Density and Low EMI,* data sheet.
- Texas Instruments, *Synchronous Inverting Buck-Boost Converter Reference Design for Communications Equipment*, design guide.

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