Application Note

Power Supply Design for AMD Versal™ AI Edge Series

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ABSTRACT

This application note details the design considerations and power tree design needed to support the VE2302 device. The publication can also be used as a foundation for designing the power tree for other devices of the AI Edge series.

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Trademarks

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1 Introduction

The original power source for this system can be either a battery or a power supply that is typically between 8 Vin to 18 Vin and capable of delivering about 50 W of power.

This power source is fed to an optional front-end protection (FEP) sub-circuit, controlled by the LM74910 integrated circuit (IC), that acts as a programmable electronic safety switch with numerous safety features.

Following the FEP there exists a LM25148 Buck converter, referred to as the 5V Pre-Regulator, that accepts the higher voltage input, and generates a well-regulated 5V voltage level. This 5V rail, in turn, supplies the main point-of-load (POL) converters, which regulate the various voltages needed to supply the VE2302 device's many rails. Two TPS6287B25 regulator ICs are used to have a dual-phase converter that supplies the main digital core rail. A variety of TPS62830x variant regulator ICs are used for most of the other rails. The TPS74615 low dropout linear regulator (LDO) is used to supply one of the low-power rails, while the TLV76033 LDO is used to supply an *always-ON* bias supply, which powers a number of sub-circuits, such as the voltage supervisor and sequencer ICs. If a 3.3V always-ON power supply already exists in the system, then the TLV76033 LDO is not needed.

The TPS389006 multi-rail voltage supervisor IC monitors and communicates that all of the rails are within their respective acceptable voltage levels. The TPS38700S sequencer IC controls the correct desired order of each rail getting enabled upon system turn-ON and disabled during system turn-OFF.

The power design exhibits how the required power rails for the VE2302 device can be powered by TI regulator ICs. This design follows AMD's Minimum Rails power consolidation of supplies. Please see AMD's Power Design Manager (PDM) tool for all available power consolidation options. PDM needs to be used when estimating power for any application. This reference design uses example power estimations.

2 Design Parameters

Table 2-1 show the power rails specifications including voltages and tolerances, load currents, and sequence order for each rail. This reference design has been designed to meet all AI Edge Series power delivery specifications.

Table 2-1. VE2302 Device Power Rail Specifications.

Rail Name	Voltage	DC Spec.	AC Spec.	Current	Step	Sequence #
VCCINT/VCC_PMC/VCC_PSFP/ VCCPSLP/VCC_RAM/VCC_SOC/ VCC_IO	0.8V	±1%	±17mV	39A	33%	2
VCCO	1.5V	±1%	±5%	3A	100%	1
VCCAUX/VCCAUX_PMC/ VCCAUX_SMON	1.5V	±1%	10mVpp	1.1A	100%	3
GTAVCC	0.88V	±2%	10mVpp	0.7A	70%	4
GTAVTT	1.2V	±2%	10mVpp	1.3A	70%	6
GTAVCCAUX	1.5V	±2%	10mVpp	0.05A	70%	5

Figure 2-1 shows the block diagram of the power tree for the VE2302 device.

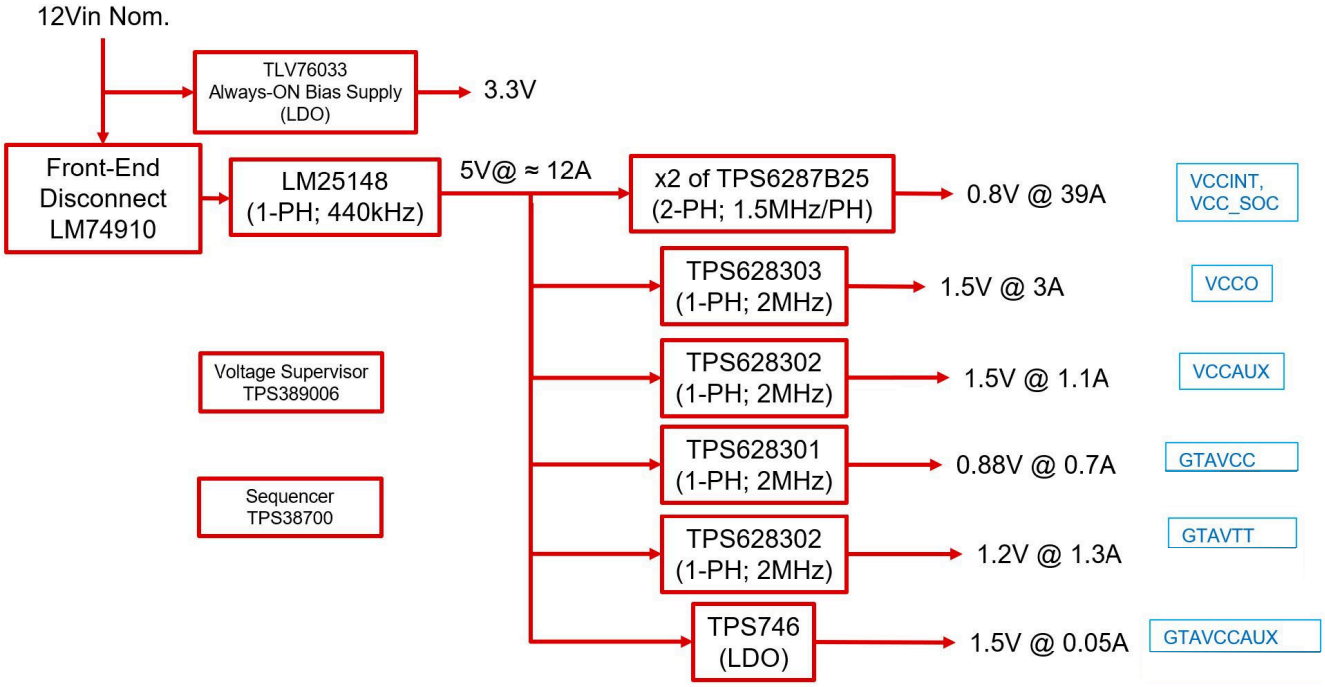

Figure 2-1. VE2302 Device Minimum Rails Configuration Power Tree Block Diagram

3 Schematics

Figure 3-1 shows the LM74910 schematic with critical components. For layout guidance, see the corresponding device data sheet and EVM user guide.

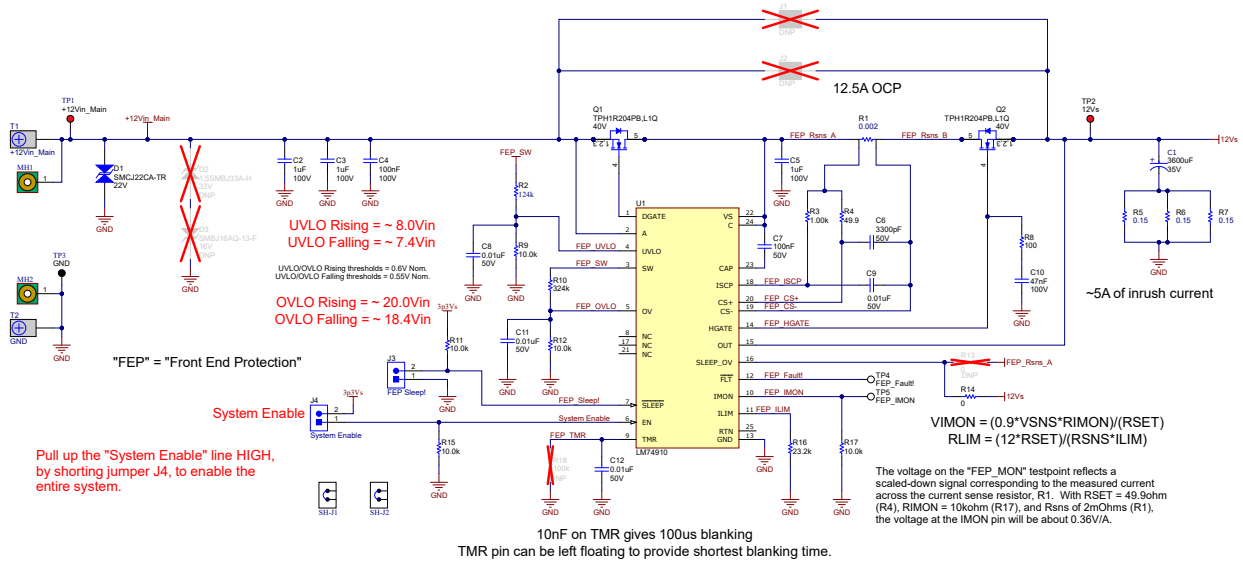

Figure 3-1. LM74910 Schematic for Front-End Protection

Figure 3-2 shows the TLV76033 schematic with critical components. For layout guidance, see the corresponding device data sheet and EVM user guide.

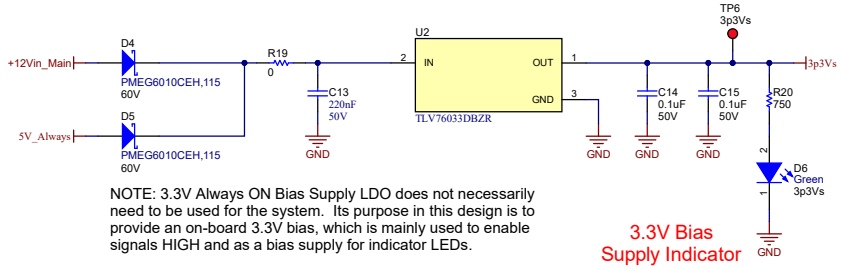

Figure 3-2. TLV76033 Schematic for 3.3V Always-ON Bias Supply

Figure 3-3 shows the LM25148 schematic with critical components. For layout guidance, see the corresponding device data sheet and EVM user guide.

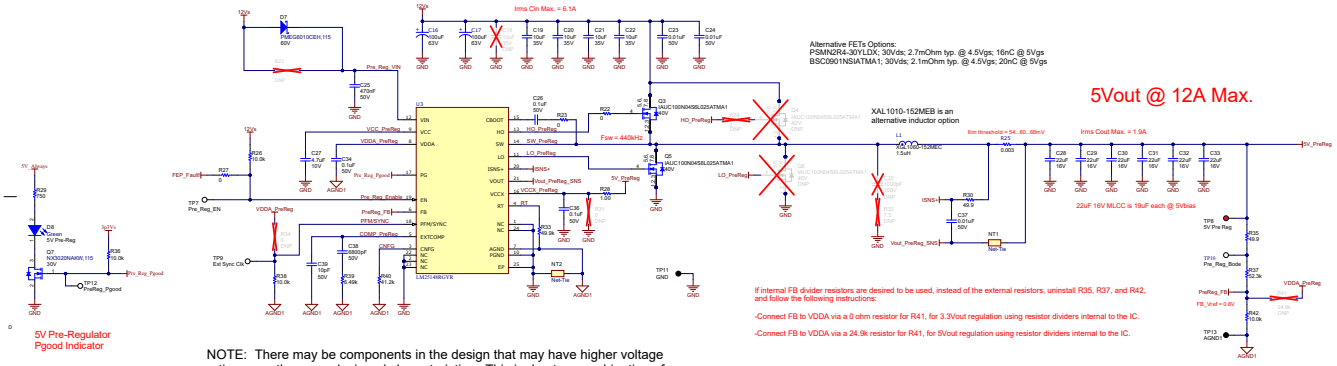

Figure 3-3. LM25148 Schematic for 5V Pre-Regulator Buck Converter

Figure 3-4 shows the TPS6287B25 schematic with critical components. For layout guidance, see the corresponding device data sheet and EVM user guide.

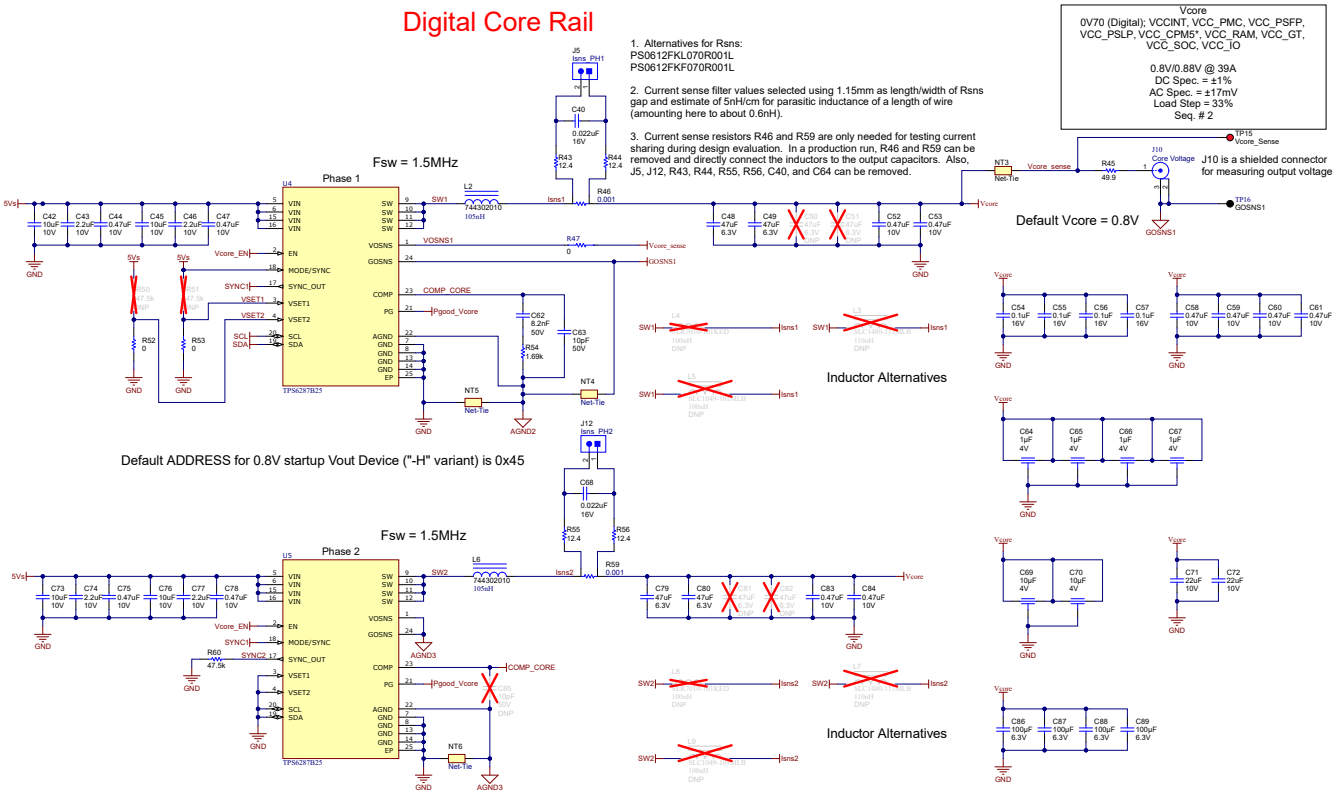

Figure 3-4. TPS6287B25 Schematic for Digital Core Rail

Figure 3-5 shows the TPS62830x schematic with critical components. For layout guidance, see the corresponding device data sheet and EVM user guide.

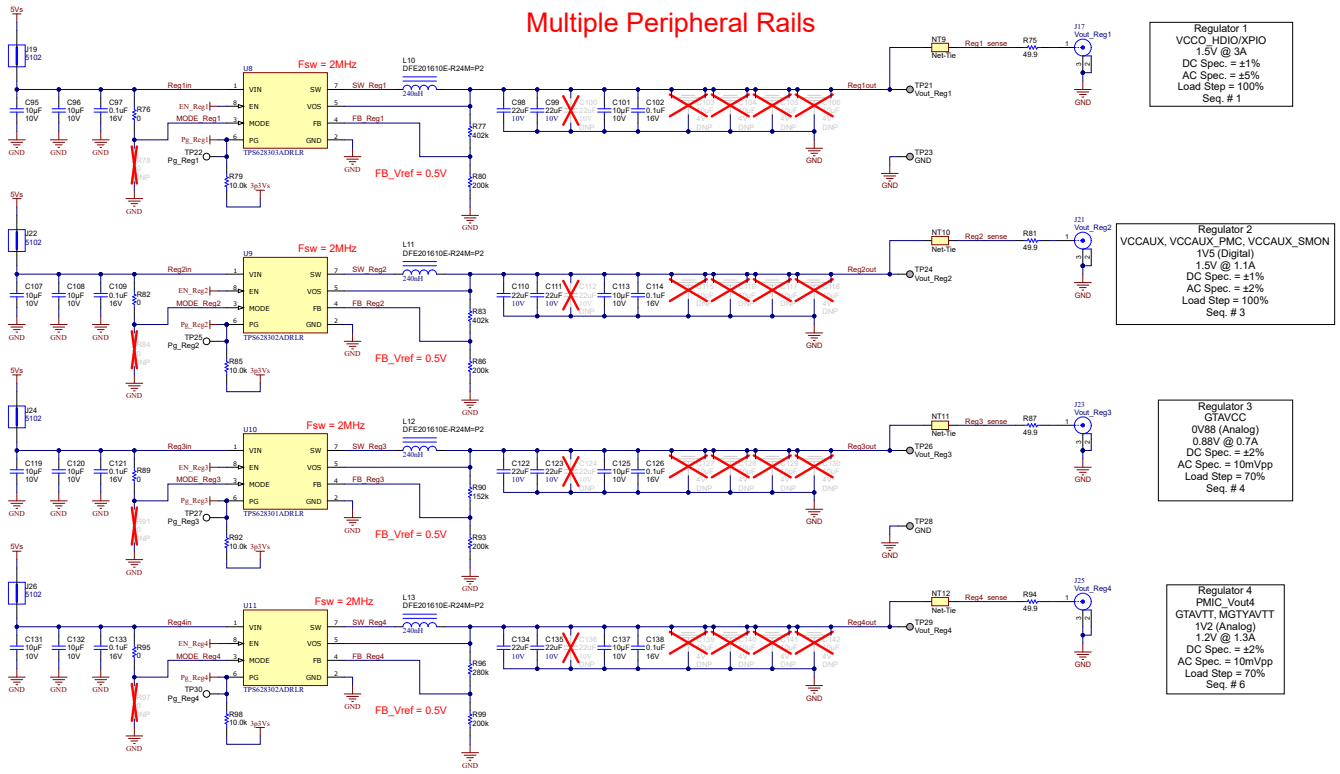

Figure 3-5. TPS62830x Schematics for Multiple Peripheral Rails

Figure 3-6 shows the TPS746 schematic with critical components. For layout guidance, see the corresponding device data sheet and EVM user guide.

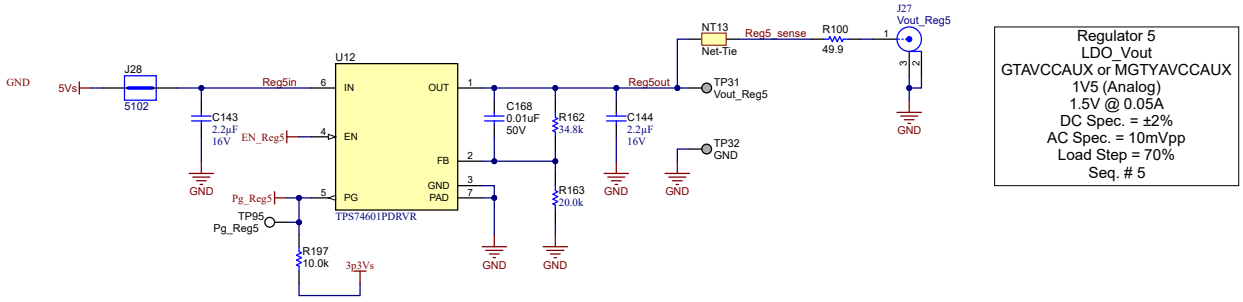

Figure 3-6. TPS746 Schematic for GTAVCCAUX Rail

Figure 3-7 shows the TPS389006 and TPS38700S schematics with critical components. For layout guidance, see the corresponding device data sheet and EVM user guide.

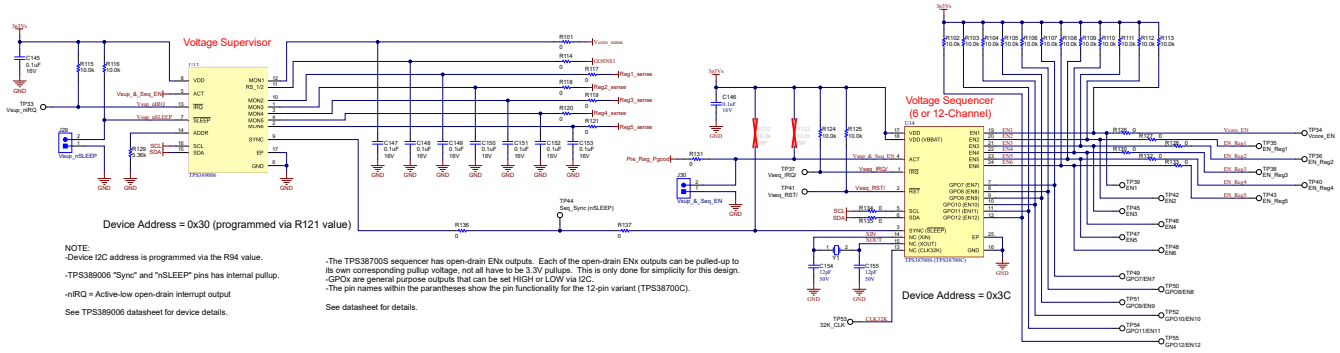

Figure 3-7. TPS389006 and TPS38700S Schematics of Voltage Supervisor and Sequencer

4 Design Considerations

A more detailed description of each sub-circuit is discussed herein.

5 Front-End Protection

A LM74910 front-end protection (FEP) circuit is found at the main input of the circuit where the main power source connects. This FEP controller provides features such as:

- Reverse-polarity protection
- Programmable over-current protection (OCP) disconnect (through R1, R16, and R4 component values)
- Programmable under-voltage disconnect/lockout protection (through R2 and R9 divider values)
- Programmable over-voltage disconnect/lockout protection (through R10 and R12 divider values)
- Programmable output-voltage ramp/slew time, which enables a controlled current into bulk capacitance, upon startup (through R8 and C10 component values)
- Programmable protection/fault delay time (through a resistor or capacitor, R18 or C12, from the *TMR* pin to GND)
- Current monitoring (through R1, R17, and R4 components values)

For details on the functionality mentioned and other features, please see corresponding sections of the LM74910 data sheet.

Other options are available for the front-end protection IC, aside from the LM74910. Please see the Texas Instrument website and search in the *Ideal diode/ORing controllers* section for alternatives.

If a front-end protection is not needed, omit the entire LM74910 sub-circuit (everything to the right of *TP1* and to the left of *TP2*) and, in this circuit depiction, connect the main input supply *+12Vin_Main* to the *12Vs* node by installing J1 and J2 jumpers.

6 3.3V Always-ON Bias Supply

A simple wide input voltage LDO is used to provide an always-ON 3.3V bias supply. This is used mainly to power the on-board voltage supervisor and sequencer ICs, as well as make available a positive supply for high level pull-up or enable signals. If the system already has a voltage rail that is independent of the rails in this application brief, with a value of 3.3V or similar low voltage that can be used to supply the voltage supervisor and sequencer ICs, then this LDO is no longer necessary.

7 5V Pre-Regulator Buck Converter

All of the Point-of-Load (POL) converters in this system regulate relatively low voltages. To have a solution that optimizes for size, cost, and complexity, it is more viable to use POL converters that are optimized for low-voltage applications, which can usually accept maximum input voltages of around 5V. This brings in the need to have a pre-regulator converter that accepts a wide input voltage and regulates the intermediary voltage of 5V. The LM25148, a wide-input synchronous buck controller IC, is used for this purpose. The LM25148 is set to run at a switching frequency of 440kHz. The LM25148 includes features such as dithering or spread-spectrum for improved EMI performance, integrated bootstrap diode for the high-side driver supply, the capability of programming the output voltage without the use of feedback resistor dividers, and other features that can be found in the device data sheet.

8 Low-Voltage High-Current Core Rail Buck Converter

For the low-voltage core rail, a 2-phase interleaved synchronous Buck converter is implemented using two of the TPS6287B25 regulator IC. This device can be used as a single-phase converter, or can be daisy-chained with other TPS6287B25 ICs to work together as an interleaved system. For the VE2302 device, a 2-phase TPS6287B25 design is implemented, with each phase switching at 1.5MHz. Phase 2 can be programmed to have a 180-degree phase shift from Phase 1, leading to an interleaved design, with an effective switching frequency of 3MHz. The TPS6287B25 has I2C capability, which can be used to program various features, functions, and parameters (see device data sheet for details). When configured as a multi-phase converter, the first phase device in the chain of devices becomes the main controller. This is the device that I2C communication is made with, as well as sets and dictates to the other phases, the output voltage setpoint, the compensation voltage, and main synchronization clock. To be able to provide significant amount of current in a very short time window, features like droop compensation implemented in TPS6287B25, selectable through I2C, helps to reduce

overshoot and undershoot of the core voltage during steep load variations. Table 8-1 shows the IC pin functions for the primary/control phase device and the non-primary phase devices.

Alternative inductor options include: SLC1480-111MLB, SLR7010-101KED, SLC1049-101MLB

Table 8-1. TPS6287B25 Primary Phase and Non-Primary Phase Pin Functions

Pin Name	Primary Phase/Device Function	Non-Primary Phase/Device Function
VIN	Input voltage; connect to Vin	Input voltage; connect to Vin
EN	Enable pin; gang all phase EN pins together	
MODE/SYNC	Sets the operating mode for all phases	Switching clock input received from preceding phase
SYNC_OUT	Switching clock output to drive next phase	Switching clock output to drive next phase unless no other phases to drive
VSET1	Configures and sets default output voltage	No function; GND this pin
VSET2	Configures and sets default output voltage	No function; GND this pin
SCL	I2C clock	No function; GND this pin
SDA	I2C data	No function; GND this pin
SW	Switch node; connect to power inductor	
VOSNS	Output rail positive node remote sense	Output rail positive node remote sense; connect to positive of local output capacitor
GOSNS	Output rail GND node remote sense	Output rail GND node remote sense; connect to GND of local output capacitor
COMP	Compensation network pin; gang all COMP pins together	
PG	*Power good* output; gang all PG pins together	
AGND	Analog ground; perform proper connection as shown in data sheet or evaluation board	
GND	Power ground; perform proper connection as shown in data sheet or evaluation board	
EP	Exposed pad; connect to power ground and flood GND polygon pour to dissipate heat; see data sheet or evaluation board for details	

9 On-Board Core Rail Output Load Transient Stepper

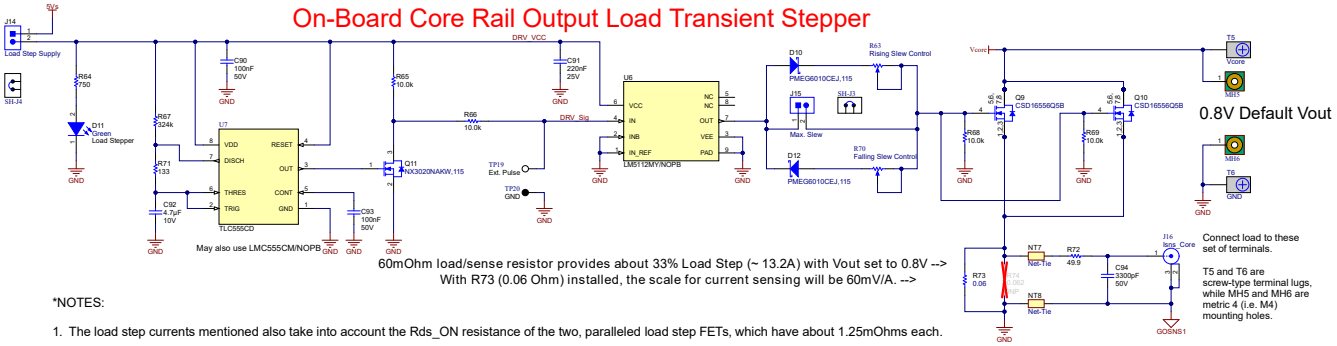

Figure 9-1. On-Board Core Rail Output Load Transient Stepper Sub-Circuit Schematic

The on-board load transient stepper shown is intended to be used with the low-voltage core rail buck converter. The benefit of having a dedicated, on-board load stepper is for faster load transient slew rates. This is achieved by having the load stepping FETs and current sense resistor as close to the converter output as possible, thus reducing parasitic trace inductance as much as possible.

This sub-circuit is comprised of a pulse generator, a FET gate driver, FET switches and a load resistor, which also serves as a current sense resistor. The load stepper pulses are generated by a TLC555 timer, configured as an astable multivibrator or oscillator, generating a free-running train of load step pulses. The HIGH pulse time is approximately programmed to be 1ms, which takes place about once every second. If desired, this on-board timer output can be overridden by an external load step signal provided by the user, at the TP19 *Ext. Pulse* test-point. Make sure the load step pulse duration and duty cycle do not exceed the safe operating area and

thermal limits of the power FETs and the current sense resistor of the load stepper. The load step current can be set by using an appropriately selected load resistor value for R73, or R74. Remember to account for the total equivalent Rds_ON of the FET(s) used, since these are in series to the current sense resistor. The load current can be measured using an oscilloscope connected to the J16 *Isns_Core* connector and is represented as a voltage across the current sense resistor. The load current will essentially be determined by dividing this measured voltage by the load resistor value. For example, in the provided schematic, with the current sense resistor of 0.06Ω, the scale will be 60mV/A, or another way is to look at it as an inverse, that is 16.7A/V. The load step rising-and-falling edge slew rates can each be controlled/adjusted (within limits) by the R63 and R70 potentiometers. The fastest possible for both rising and falling pulse edges can be achieved by installing/shorting the J15 jumper, essentially bypassing the two potentiometers.

10 Multiple Peripheral Rail Buck Converters Sub-Circuits Schematic

Regulators *Reg1* through *Reg4* use different variants of the TPS62830x regulators, each with a different current rating: available in 1-A, 2-A, and 3-A capable options. TPS62830x provide a fast transient response with small output capacitance. However, depending on the output ripple and load transient requirements, more output capacitors can be added. The total effective output capacitance for each TPS62830x regulator must not exceed 200µF. See data sheet for alternative inductor options, as well as other details.

Additionally, this device family has an excellent EMI performance due to the integrated on-chip noise-filtering capacitors.

At the point-of-load, it can be desired to populate as many of the 3-terminal output capacitors, as needed. 3-terminal output capacitors are not necessarily required, but these tend to have lower parasitic inductance, which can help with high slew rate load steps. These capacitors should be placed close to the point of load (in this test case, near the load board connectors, J18 and J20).

The total *effective* output capacitance for each TPS62830x regulator should not exceed 200µF. See data sheet for alternative inductor options, as well as other details.

Currently, the Regulator 5 rail for GTAVCCAUX rail is implemented using the TPS74615 linear regulator. The power loss, which is entirely dissipated in the part, at the full load of 50mA is 175mW. If a lower power dissipation (for example, higher efficiency and lower temperature rise) is desired, two Buck switching regulator alternatives to consider using are: TPS629203DRL and TPS62A01ADRL.

11 Voltage Supervisor and Sequencer

TPS389006 is a programmable 6-channel voltage supervisor. The RS_1/2 is a remote ground sense pin that can be connected to the local ground terminal of either the MON1 or MON2 voltage rails. This type of ground sensing provides a precision, differential voltage sensing of that rail. If the RS_1/2 pin is not used, all six voltage sense lines can share the same common ground. This device contains numerous registers that can be programmed via I2C. Programmable parameters include, voltage threshold levels, hysteresis levels, and glitch immunity times. The *IRQ/* pin output can be used as a system *Power Good*. The device I2C address can be programmed using a resistor from the *ADDR* pin to GND. With the 5.36 k resistor depicted in the schematic, the address is programmed to 0x30.

The TPS389006 used in Figure 3-7 depicts the adjustable variant of the device, which can require a resistor voltage divider at the input of each sense line to adjust the voltage threshold. If the design does not permit the use of resistor voltage dividers, please use these devices for evaluation purposes, then contact a TI representative to discuss a one-time programmable (OTP) variant, to set the required thresholds as default for each sense pin.

The TPS38700S is a 6-channel sequencer IC used to turn each regulator ON and OFF in a particular sequence with programmable delays between each event. Both the TPS389006 voltage supervisor and TPS38700S sequencer can either be used independently or in tandem with one another. In this design example, the two ICs are implemented to be used together. In this configuration, when the devices are enabled, their *ACT* pins go HIGH, enabling the first regulator in the system. When the measured voltage of this first rail is within the programmed power good voltage window, the supervisor communicates a toggle signal to the sequencer. Once this signal is received, the sequencer can set HIGH the next enable signal in the sequence, *after* the programmed delay time elapses. This continues to take place until all sequences are enabled and all six

regulators are enabled. When the sequence is disabled, the same operation takes place, except this time in the opposite order.

12 12-Channel Sequencer Alternative

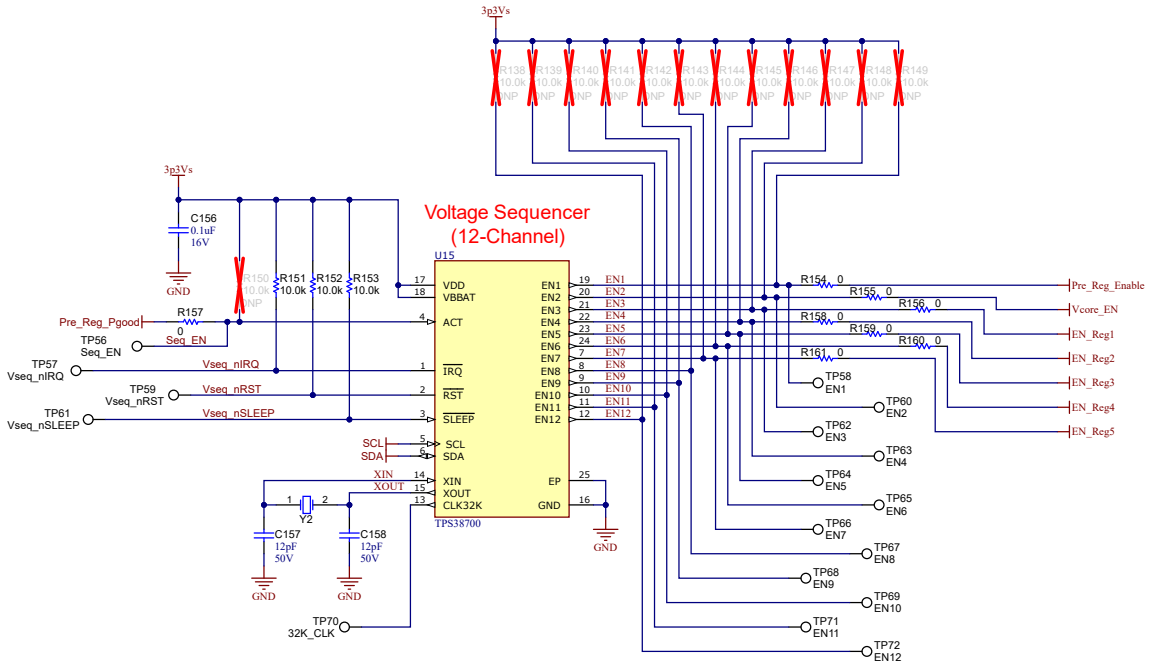

Figure 12-1. 12-Channel Sequencer Sub-Circuit Schematic

An alternative, expanded option to the 6-channel TPS38700S sequencer is the 12-channel TPS38700C. Though this device has double the enable channels, the device3 does not have the communication capability with the TPS389006 supervisor through a *SYNC* pin. The TPS38700C that is currently available has push-pull outputs, however there can be open-drain output variants made available sometime in the future. The sub-circuit depicted in Figure 12-1 schematic shows the capability of using both output variants: use the pull-up resistors with the open-drain output variant and omit these when using the push-pull output variant. If the open-drain output variant of the device is used, each of the *ENx* outputs can be pulled up to their corresponding HIGH-level voltage. All *ENx* pins are pulled up to the same 3.3V supply for simpler demonstration purposes.

The TPS38700CxxxRGER sequencer IC is a generic placeholder. The part can be factory trimmed to accommodate custom specifications. Contact a Texas Instruments representative to discuss customization offerings.

13 Summary

The design outlined in this application note, using the LM74910, TLV76033 (optional), LM25148, TPS6287B25, TPS62830x, TPS74615, TPS389006, and TPS38700S ICs, provides the power requirements for the VE2302 device while maintaining good efficiency. The I2C control of the TPS6287B25 regulator and TPS389006 voltage supervisor allow for a large amount of control and the ability to configure the system through a single serial communication line.

14 References

- Texas Instruments, *LM74910-Q1: Automotive ideal diode with circuit breaker, 200-kHz ACS and under- and overvoltage protection* product page
- Texas Instruments, *TLV760: 100-mA, 30-V, low-dropout voltage regulator* product page
- Texas Instruments, *LM25148: 42-V synchronous buck DC/DC controller with ultra-low IQ* product page
- Texas Instruments, *TPS6287B25: 2.7-V to 6-V Input, 10-A,15-A, 20-A, 25-A, Fast Transient Synchronous Step-Down Converter With I2C Interface* product page
- Texas Instruments, *TPS628303: 2.25-V to 5.5-V, 3-A step-down converter with 1% accuracy in small QFN and SOT583 packages* product page
- Texas Instruments, *TPS746: 1-A, low-IQ, high-accuracy, adjustable ultra-low-dropout voltage regulator with power good & enable* product page
- Texas Instruments, *TPS389006: Multichannel overvoltage and undervoltage I²C programmable voltage supervisor* product page
- Texas Instruments, *TPS38700S-Q1: Automotive power-supply sequencer with I²C support for up to six-channels* product page

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