Application Note

Implementing Bootstrap Overcharge Prevention in GaN Half-bridge Circuits

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ABSTRACT

GaN FETs offer many benefits over MOSFETs in terms of switching characteristics. However, GaN FETs also come with some unique challenges that must be solved to achieve the best performance. One of these challenges is bootstrap overcharge in half-bridge topologies.

There are a variety of methods used by circuit designers to solve bootstrap overcharge. This document compares these methods of bootstrap overcharge prevention, including methods integrated in half-bridge GaN drivers such as LMG1205, LM5113-Q1, and LMG1210.

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1 Introduction

The industry is increasingly adopting GaN FETs to improve switching characteristics over silicon MOSFETs in electric vehicles, server power supplies, and motor drivers. GaN FETs enable operation at higher switching frequencies, which can help to reduce system size, cost, and weight.

The 48-V to 12-V DC/DC converter plays a vital role in many power applications and is often achieved using an LLC, synchronous buck, or buck-boost topology. One common factor between these half-bridge topologies is that the topologies require dead time, or nonconducting time, where both the high-side and low-side FETs are off.

The load current (IL) must continue circulating during the dead time. This mode of operation, where the FET Vgs is 0 V and a negative current is flowing, is called the *third quadrant* operation. For more details about third quadrant operation, see *Does GaN Have a Body Diode?—Understanding the Third Quadrant Operation of GaN*. Figure 1-1 shows an example half-bridge buck converter with the relevant parameters. Figure 1-2 shows the main issue; a large negative voltage is created on HS during the dead time.

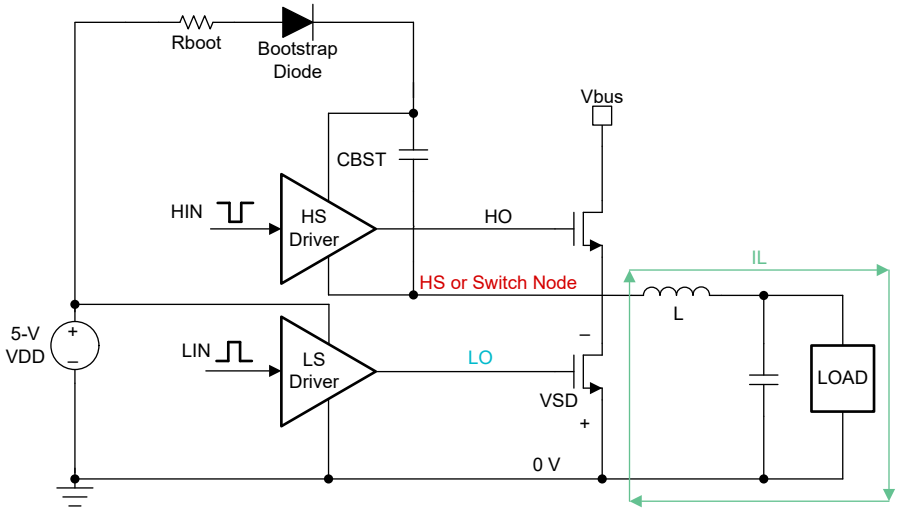

Figure 1-1. Simplified Schematic of a Half-bridge Buck Converter Showing the Relevant Parameters to Bootstrap Overcharge

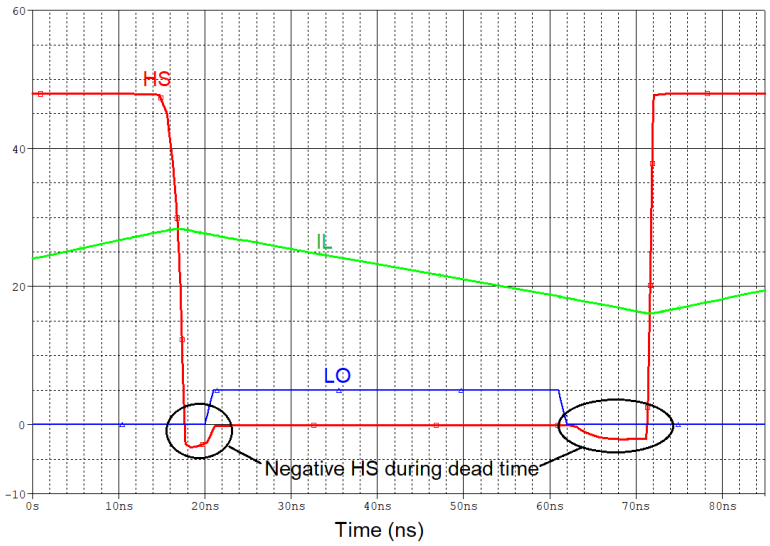

Figure 1-2. Waveform Capture Showing the Relationship Between IL, Dead Time, and Negative HS Voltage

This negative voltage has to do with the properties of GaN FETs. Unlike silicon power FETs, GaN FETs do not have a parasitic P–N junction that creates a *body diode*. In a MOSFET, the body diode handles the third-quadrant operation, acting like a diode with a forward voltage (VF) of approximately 0.7 V. The negative voltage created on HS when a MOSFET conducts in the third quadrant is approximately the VF of the body diode. In GaN FETs, the lack of a body diode means the behavior is different.

Third-quadrant operation happens when Vgs is low, usually at 0 V, and current is forced through the GaN FET. The FET is off in this state and is viewed as a large resistor. A voltage is created when current is forced to flow through this large resistor. This voltage is from the source to the drain of the device (VSD). The drain must be negative respective to the ground because the source is tied to the ground. The lowest voltage node acts as the source of the device because of the bidirectional characteristics of the GaN FET. The gate voltage is 0 V, and the drain (now source) is negative, so there is a Vgs created on the device. Once this Vgs exceeds the threshold voltage (Vth) of the GaN FET, the FET turns on and becomes a small resistance again. This stops the voltage increase, ultimately resulting in a negative voltage roughly equal to the Vth of the GaN FET appearing on the HS node. This process is called *self-commutation* because the device turns itself on.

Self-commutation has two main differences from the body-diode conduction of the MOSFET. The first difference is that the self-commutative current conducts in the channel of the device rather than the parasitic body diode. A reverse recovery charge (Qrr) is built into the body diode when current is conducted in the P-N body diode. However, there is no Qrr when current conducts in the channel. The second difference is that self-commutation results in a much higher negative voltage than body-diode conduction. The higher voltage is because the GaN FET Vth is much higher than a body-diode VF.

Many designers like to think of a GaN FET as having a body diode with a high forward voltage and no reverse recovery charge because of these differences. The central gap in this diode model is that the model ignores the role of Vg in determining the negative voltage. The negative HS voltage increases if designers use a negative Vgs to prevent a false turn-on, as many designers do.

Equation 1 estimates the negative HS voltage for any GaN FET. Most manufacturers include a plot for use, as shown in Figure 1-3.

$$V_{SD} = V_{th} + I_{SD} \times R_{DS(on)} - V_{G(off)} \quad (1)$$

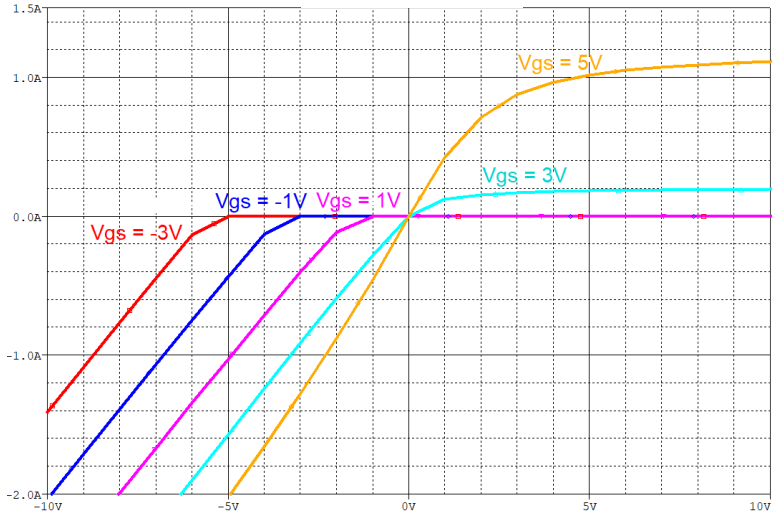

Figure 1-3. Plot Showing the Third Quadrant Vds Voltage Over Load and Different Vgs Voltages

2 Bootstrap Overcharge

The negative voltage created during the dead time has a few consequences. First, negative voltage contributes to losses as the low-side FET must dissipate VSD multiplied by IL. Second, negative voltage leads to overcharging on the bootstrap circuit, which is often used to provide bias to the high-side FET. Typically, the bootstrap capacitor (Cboot) is charged when the low-side FET is on and the HS node approaches 0 V Current (Iboot) and then flows through the bootstrap diode from VDD to charge the Cboot capacitor to VDD. See *Bootstrap Circuitry Selection for Half-Bridge Configurations* for further explanation of bootstrap circuits.

During dead time, the potential across Cboot can increase to VDD plus the negative voltage, easily exceeding 6–7 V in many cases. This means that the bootstrap capacitor is overcharged to voltages above VDD. This type of overcharging is possible in all half-bridge configurations, not just ones using GaN FETs. However, GaN FETs tend to have a sensitive gate that can handle only 6–8 V maximum, depending on the construction. Bootstrap overcharge prevention is critical in GaN half-bridges because of higher negative HS voltages and greater sensitivity to overcharging. Some half-bridge gate drivers like LM5113-Q1, LMG1205, and LMG1210 have integrated bootstrap overcharge prevention circuits.

3 Modeling Bootstrap Overcharge

One way to model bootstrap overcharge is using charge (Q). The bootstrap current charges Cboot during the charging period. Then, Cboot discharges when sourcing current to drive the high-side FET. Cboot reaches steady-state voltage when the balance of charging and discharging is equal. In Figure 3-1, the top graph shows the voltage rise and fall over the charging and discharging period. The bottom graph shows the Qin and Qout based on current.

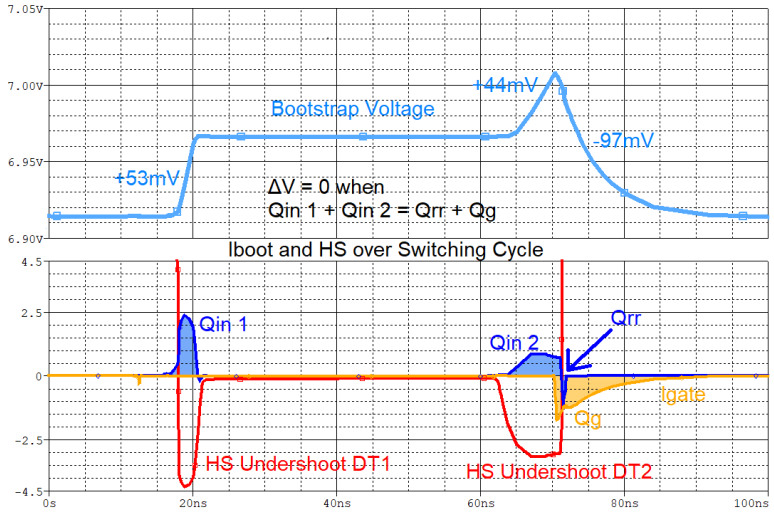

Figure 3-1. Plot From a Simulation of Bootstrap Overcharge

Figure 3-1 shows a simulation of a half-bridge where Cboot overcharges by nearly 2 V. During the dead time, a bootstrap current (Iboot) flows through Cboot due to the increased voltage potential caused by negative HS. During the normal charging period where HS is 0 V, Cboot does not charge because the voltage across Cboot is already higher than VDD. Cboot charges again during the next dead time, but slightly less as the load (IL) and HS decrease. Finally, Cboot discharges into the gate charge (Qg) of the high-side FET and the reverse recovery (Qrr) of the bootstrap diode.

The integral of Iboot gives the bootstrap charge (Qin) over time. The bootstrap discharge (Qout) can be calculated or measured. When Qin and Qout are equal, Cboot reaches steady-state voltage. As shown in Figure 3-1, the area of Qin 1 and Qin 2 equals the area of Qrr and Qg.

Equation 2 and Equation 3 describe this behavior:

$$Q_{in} = \int_{t}^{t+DT1} I_{boot}(t)\,dt + \int_{t}^{t+DT2} I_{boot}(t)\,dt \quad (2)$$

$$I_{boot}\left(t\right) = \frac{V_{DD} - V_F(t) - V_{boot}(t) + V_{SD}(t)}{R_{boot}} \quad (3)$$

Qout primarily consists of Qg to drive the high-side switch, leakage from the driver circuits, gate-source leakage of the GaN FET, and reverse recovery in the bootstrap diode. In most cases, Qg alone is sufficient to estimate Qout because Qg is the most significant factor. FET data sheets often include a *Qg versus Vgs* plot, which offers a way to estimate the steady-state voltage.

Equation 2 and Equation 3 guide understanding into the available options for addressing bootstrap overcharge. Relevant information is sometimes available late in the design process, making calculating parameters like Vf (which changes with Iboot) difficult. Additionally, the results change over load and temperature. Simulation offers a more straightforward, accurate method than calculating for determining bootstrap overcharge.

4 Changing Bootstrap Components

The simplest method to address bootstrap overcharging is making changes to the bootstrap circuit. This method includes increasing bootstrap resistance, using a higher Vf bootstrap diode, or even using a bootstrap inductor. This bootstrap method works by limiting the current that flows through the bootstrap path (Iboot) and, in return, reduces the Qin.

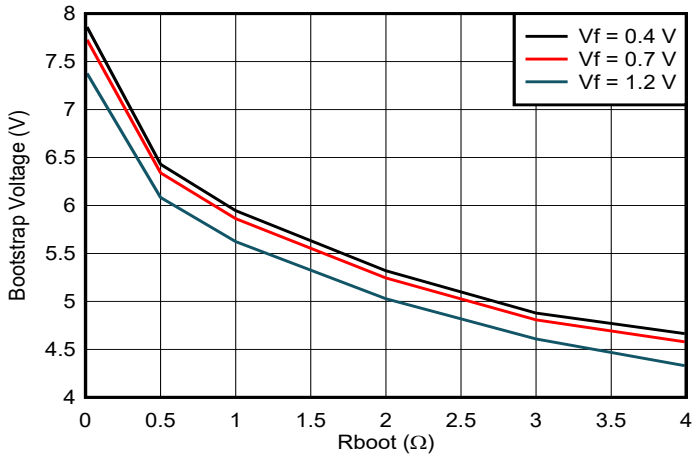

Figure 4-1. Plot Showing Steady-state Bootstrap Voltage Over Rboot and Diodes With Different Forward Voltages

The GaN FET used in this example was rated for 6 V maximum on the gate. An Rboot less than 1-Ω results in a gate voltage that exceeds the rating of the GaN FET. Adding a 2-Ω Rboot reduces overcharge to a more reasonable level, under 5.5 V. This bootstrap method is simple and effective but has some drawbacks.

Rboot and Cboot form an RC filter. The start-up time of the system is determined by the time constant of the RC filter. Increasing Rboot increases the start-up time of the system. The amount of overcharging varies over load and temperature, therefore, designing Rboot to account for the worst-case operating point is essential. To account for the worst-case, Rboot must be larger and the start-up time increases further. Alternatively, adding inductance to the bootstrap circuit limits the bootstrap current. This relationship between inductance and current is given in Equation 4:

$$V = L\frac{di}{dt} \quad (4)$$

A correctly-sized inductor limits current buildup in the short dead time without impacting normal charging. Adding inductance returns slightly higher efficiency than resistance because the process recycles some energy instead of dissipating energy. One downside is that forcing the inductor current off when HS rises generates an inductive voltage spike. In addition to the oscillating current seen on Iboot in Figure 4-2, there is a corresponding voltage spike across the bootstrap diode.

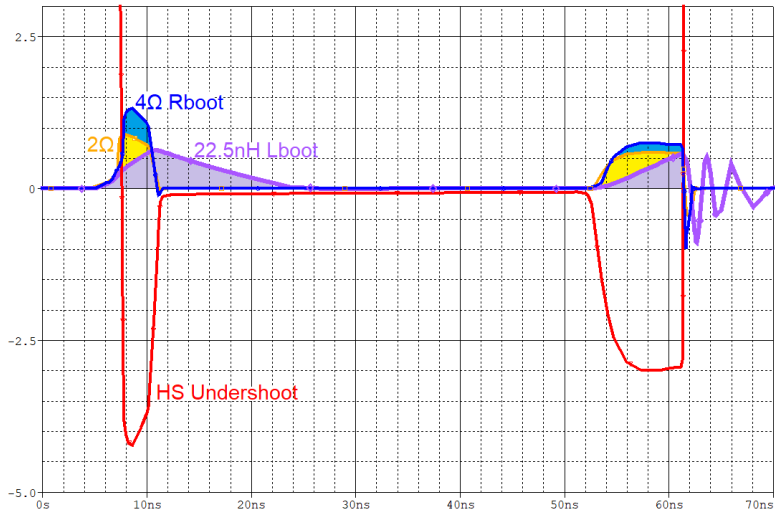

Figure 4-2. Waveform Comparing Iboot Current With a 2-Ω Resistor, 4-Ω Resistor, and 22.5nH Inductor

The potential for an inductive voltage spike requires the bootstrap diode to include a higher blocking voltage and a smaller capacitance to reduce the ringing during reverse recovery. This over sizing, combined with the higher cost of inductors versus resistors, yields a costlier option than other methods.

5 Zener Diode Method

A common, simple option to bootstrap overcharging is to place a Zener diode with approximately 5 V breakdown (Vz) parallel to Cboot. Any excess charge is dissipated in the Zener diode once Cboot is charged to Vz rather than charging Cboot.

The Zener diode method prevents the Cboot voltage from exceeding Vz in all conditions compared to the bootstrap option discussed previously. Additionally, 5-V to 6-V Zener diodes have very small temperature coefficients. Thus, the Zener diode method is reliable under different load and temperature conditions.

Another benefit to using this method is that the Zener diode allows for some overcharging. A small amount of overcharging is beneficial, as overcharging cancels the voltage drop in the bootstrap diode. Canceling the voltage drop increases the bootstrap voltage and reduces conduction losses in the high-side FET.

There are drawbacks to using the Zener diode method. First, Zener diodes do not transition instantly to and from breakdown. A Zener diode data sheet often includes a *Reverse Voltage versus Current* plot. This curve has a *knee*, which results in extreme variations of the Zener voltage depending on the current it must sink. This drawback presents trade-offs: a low Vz Zener diode has more leakage current at nominal voltage, but a higher Vz diode clamps at a higher voltage. A Zener diode with a low enough Vz to prevent overcharge always adds leakage current at nominal voltages.

Second, the Zener diode power dissipation is excessive if there is low bootstrap resistance to limit Iboot. The power dissipated by the Zener diode is the product of Vz and Iz. Iz approaches Iboot when the bootstrap voltage exceeds the breakdown voltage of the Zener diode. The instantaneous power dissipation exceeds 10 W if Iboot is more than 2 A. High power dissipation hurts efficiency and damages the Zener diode if the ratings are exceeded.

6 Schottky Diode Method

Another method for addressing bootstrap overcharge is to place a diode parallel to the lower GaN FET. In this configuration, the diode behaves like the body diode of a MOSFET. The diode limits the negative HS voltage to the VF of the diode, which is often less than 1 V. Reducing the negative voltage on HS reduces bootstrap overcharging and dead time losses in the low-side GaN FET. Schottky diodes have better reverse recovery and VF performance compared P-N diodes, and are favored in this application.

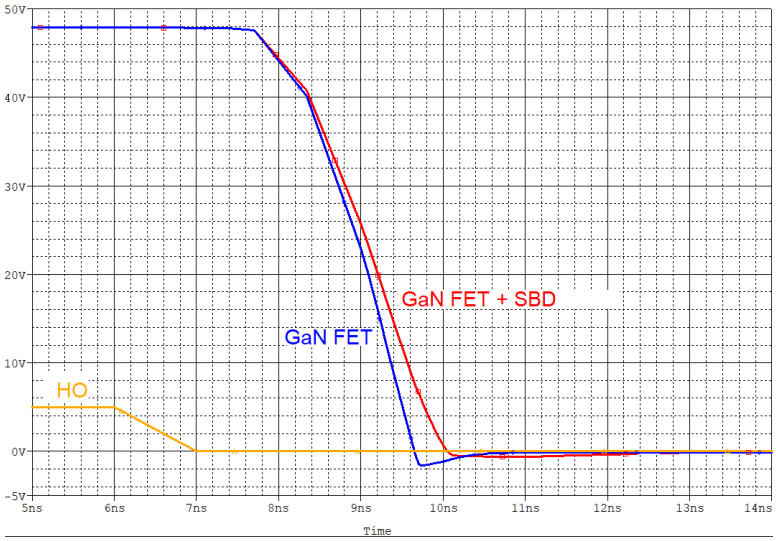

Figure 6-1. Waveform Comparing HS Slew Rate and Undershoot With and Without a Parallel Schottky Diode (SBD)

Figure 6-1shows that the GaN FET reaches a higher dv/dt and switches faster than the GaN FET with a parallel diode. The GaN FET reaches approximately –1.8 V on HS, while the GaN FET with the diode only reaches approximately –0.6 V. Therefore, the Schottky diode can effectively limit the negative HS voltage and prevent overcharge. The downside to using this Schottky diode is the addition of extra capacitance to the HS node, which results in increased switching time and losses.

Schottky diodes are less feasible in higher-voltage systems. Silicon Schottky diodes (SBDs) are available with blocking voltages of 100–200 V but start to lose their advantages over P-N diodes at higher voltages. SiC SBDs are becoming popular for higher voltages and can reach blocking voltages past 1200 V. However, these diodes have a higher forward voltage (greater than 1.3 V), which can be too high to prevent overcharge.

Systems with very high loads or load transients require special considerations. For example, in a 3-kW, 48-V to 12-V DC/DC converter, the load current is approximately 250 A, requiring a very large (and expensive) Schottky diode. Interleaving reduces the current requirement on each diode but requires more diodes. Adding Schottky diodes is very expensive in terms of cost and board size.

7 Overvoltage Clamp Method

Bootstrap overcharge is a common issue in GaN half-bridges, so half-bridge GaN gate driver ICs such as LMG1205 and LM5113-Q1 integrate overcharge protection. These devices work by adding an internal switch in series with the integrated bootstrap diode. The device senses the voltage across Cboot and opens the series switch when the voltage goes above approximately 5 V. The bootstrap path becomes high-impedance because the switch is in series with the bootstrap diode. Rboot is infinite—infinite Rboot results in 0 Iboot and no more Qin. The bootstrap voltage gradually decreases due to Qout and eventually falls below the threshold where the driver closes the switch again, restoring normal function to the bootstrap path.

The overvoltage clamp is a simple and effective option to prevent overcharging bootstrap. Like the Zener diode, the clamp allows a certain amount of productive overcharging to cancel out the bootstrap diode drop. In addition, the clamp is more efficient than the Zener diode because the clamp prevents excess charge rather than dissipating the charge as heat.

There are some downsides to this overvoltage clamp approach. First, this circuit has a response time delay. In LMG1205, the response time is approximately 250 ns. While this delay is sometimes acceptable, the response is too slow in some applications to prevent damage. This delay is especially noticeable when using a small Cboot and significant dead time. Second, the clamping threshold voltage is fixed, which limits device flexibility because the voltage cannot support both 5 V and 6 V gate GaN FETs.

8 Active Switch Method

The LMG1210 uses a different method to prevent bootstrap overcharge. Like LMG1205, LMG1210 uses a switch in series with the bootstrap diode path. However, LMG1210 switches on when the low-side output (LO) is high, unlike LMG1205, which switches only with overvoltage on Cboot.

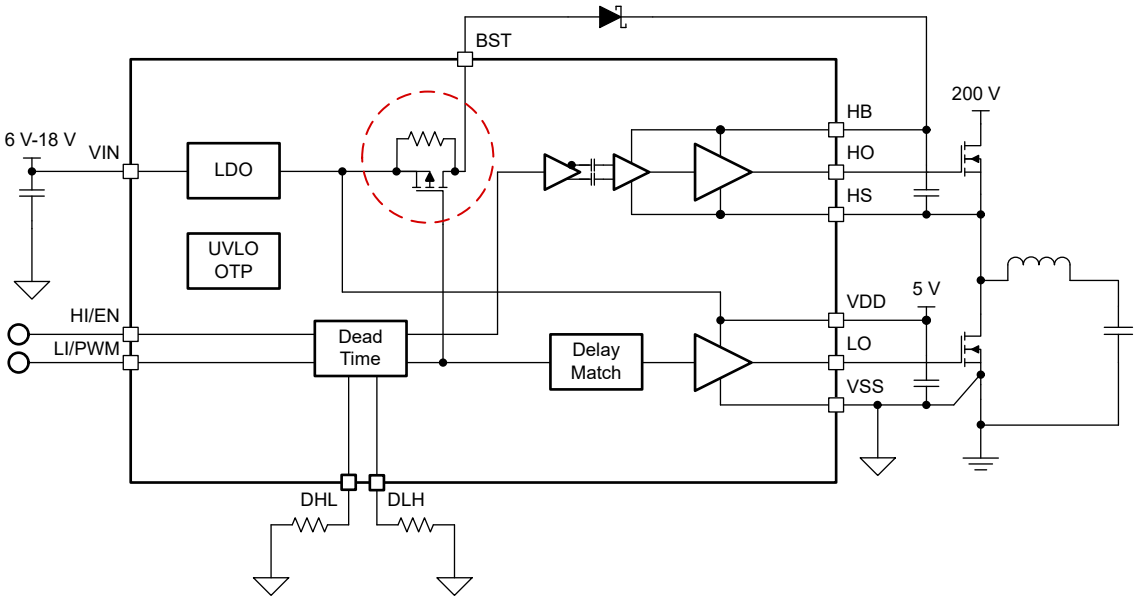

Figure 8-1. LMG1210 Functional Block Diagram Showing Series Switch Used to Prevent Bootstrap Overcharging

Bootstrap overcharging happens during the dead time because of the GaN FET third-quadrant behavior that creates large negative voltages on HS. Blocking the bootstrap diode during the dead time on every cycle prevents any possibility of overcharging. When LO is high, the dead time must be over. So, attaching the bootstrap switch state to LO consistently keeps the switch in the correct state. Figure 8-2 shows how conduction is blocked during the HS undershoot event and overcharging is prevented.

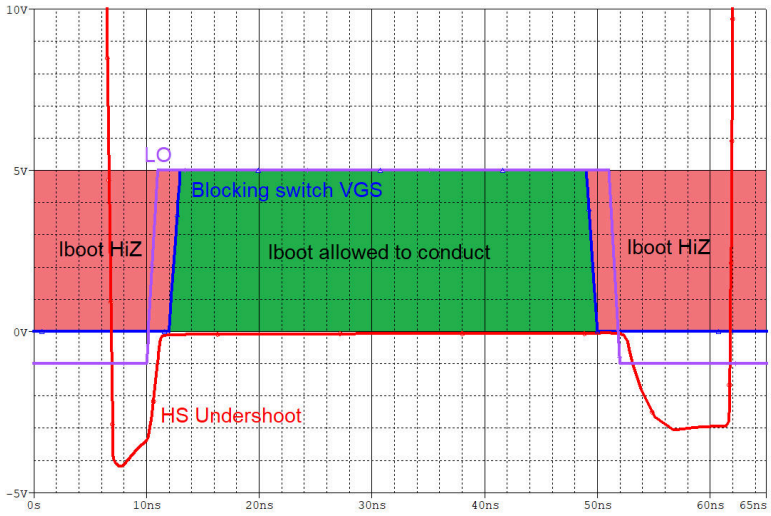

Figure 8-2. Waveform Highlighting the Bootstrap Charging Window (in Green)

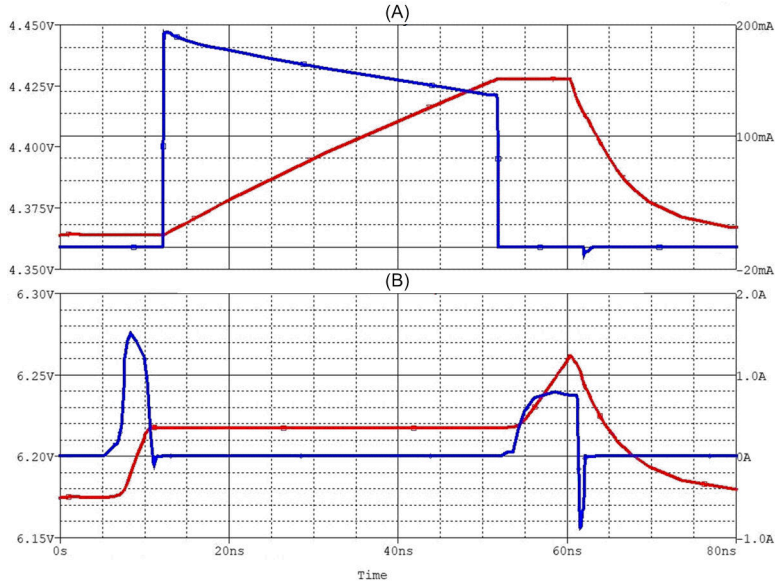

Figure 8-3. Capture Showing Bootstrap Current (blue) and Bootstrap Voltage (red) With (A) and Without (B) a Series Switch

Figure 8-3 compares the same system with and without the series switch. The system behaves correctly with the switch—where the bootstrap capacitor charges when LO is high and reaches a steady state of approximately 4.4 V. This same system overcharges without the switch past 6 V and only charges during the dead time.

One benefit of avoiding dead-time conduction is the reduction of reverse recovery of the bootstrap diode. When the bootstrap diode is permitted to conduct before HS rises, the diode builds up a significant current. The bootstrap diode has a reverse recovery event when HO is turned on and HS rises. Reference Figure 8-3, where there is nearly 1 A of reverse recovery current, as opposed to the circuit with the switch, which shows a nominal reverse current. Preventing reverse recovery events is another benefit of this active switching technique.

A downside to this active switch method is that the method does not allow productive overcharging. Therefore, the high-side GaN FET gate voltage is always VDD minus a diode drop. A lower gate voltage means the high-side GaN FET has a higher resistance and experiences more conduction losses.

The active switch method does not rely on a fixed threshold voltage and has no response time issue like the overvoltage method. Additionally, the active switch is better for supporting both 5 V and 6 V gate GaN FETs because the switch lacks a fixed threshold.

9 Synchronous GaN Bootstrap Method

The active switch method from the previous section uses a diode to block the high voltage of the HS node and a low-voltage switch in series to activate or deactivate charging. Using a single high-voltage FET to fulfill the roles of both the switch and the diode is also possible. However, one issue is that MOSFETs have body diodes, which means that when the device is turned off, the body diode can still conduct and allow overcharging during dead time.

The GaN FET lacks a body diode, conveniently presenting an opportunity to address the body diode conduction issue. The GaN FET series switch prevents bootstrap overcharge without an extra diode, as shown in Figure 9-1. As discussed, the lack of a body diode does not mean that GaN FET cannot conduct during the dead-time. However, adjusting the voltage drop of the bootstrap GaN FET to match the voltage drop of the low-side GaN FET is possible. Matching the voltage drop of each FET cancels out the negative voltage, and prevents overcharging.

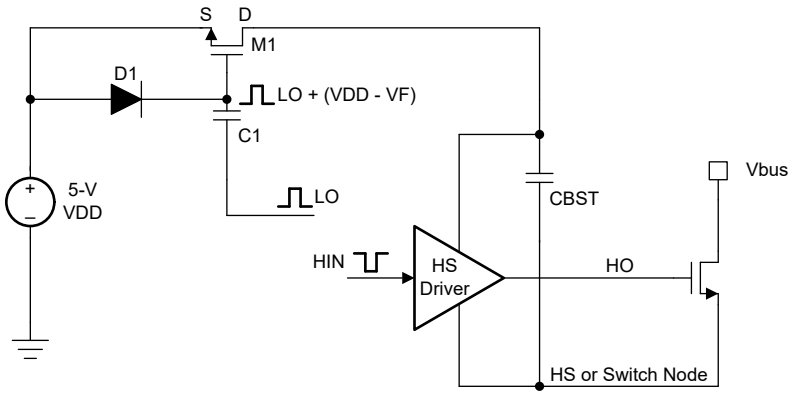

Figure 9-1. Simplified Circuit Diagram Showing the Implementation of a Synchronous GaN FET as a Bootstrap Diode Replacement.

M1 is the synchronous bootstrap GaN FET. M1 needs a blocking voltage to handle the full HS voltage, preferably with a low Coss and Cgs (for fast switching). The M1 GaN FET source is connected to VDD and driven with LO, like the LMG1210 in the previous section. In addition, a level shifter consisting of D1 and C1 steps up the LO signal above VDD. The level shifter is required because the source of the GaN FET is tied to VDD instead of 0 V, so LO needs to be higher than VDD to have a positive Vgs.

There are a few advantages to using the synchronous GaN FET bootstrap. The forward voltage drop during the normal charging period is smaller than the VF of a diode, meaning the bootstrap voltage is closer to VDD. This method also prevents bootstrap overcharge with higher efficiency due to fewer series elements. The GaN FET has no reverse recovery charge or time, which makes the design effective at high switching frequencies.

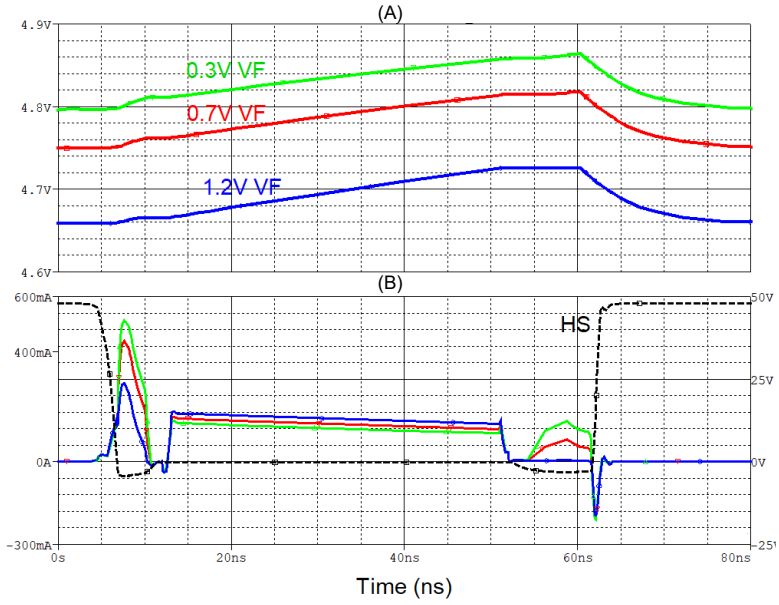

Figure 9-2. Capture showing Bootstrap Voltage (A) and Current (B) with Different Vf Level-shift Diodes

In Figure 9-2, different VF diodes were used in the level-shift circuit. A diode with a low VF of 0.3 V allows more charging in the dead time, as shown by the current spike around 10 ns. The amplitude of Iboot is related to the VF of the level-shift diode. In the second dead time around 60 ns, the 1.2 V VF diode does not allow conduction.

Equation 1 demonstrates that VGoff partially determines the VSD. The diode in the level-shift circuit has a forward voltage drop. This VF results in the effective Vgs of the GaN FET bootstrap shifting down by the diode drop. Instead of being 0 V to 5 V, the Vgs of the GaN FET is –0.7 V to 4.3 V. Therefore, the VGoff is equal to the VF of the diode. The goal is to match the VSD of the bootstrap GaN FET to the VSD of the low-side GaN FET, so selecting a diode with a different VF is an excellent tool to achieve that.

Schottky diodes and GaN FETs do not have reverse recovery. However, both have effective capacitance that requires charging and discharging every switching cycle. Charging and discharging this capacitance results in losses proportional to switching frequency. The Coss of a GaN FET is smaller than the capacitance of an equivalent Schottky diode. Therefore, a GaN FET bootstrap has less recovery losses than a Schottky diode and is more efficient at high switching frequencies.

10 Other Methods of Preventing Bootstrap Overcharge

10.1 Reducing Dead Time

Reducing the dead time duration allows less Qin. Without changing Qout, a lower Qin results in a lower steady-state voltage on Cboot. Reducing dead time is generally favorable for reducing overcharge and dead time losses. However, reducing dead time increases the risk of shoot-through, and margin is needed for load and temperature conditions. Additionally, many controllers do not have the precision to make reliable 1 ns adjustments to timing.

Given this, precise dead time control is vital for bootstrap overcharge prevention in GaN half-bridge drivers. LMG1210 has nanosecond-scale and adjustable dead time control, in addition to the built-in bootstrap overcharge prevention circuits discussed previously. Please see the *Optimizing Efficiency Through Dead Time Control With the LMG1210 GaN Driver* application note for more information.

10.2 Opting for a Bias Supply

A floating bias supply, such as UCC12041-Q1, can bias the high side instead of a bootstrap circuit. These floating bias supplies reference HS and keep Cboot consistently at the set voltage, even if HS goes negative. Floating bias supplies bypass of the overcharging issue entirely and allows for 100 percent duty cycle operation of the driver.

The bias supply option solves the problem but is potentially costlier. A bias supply is more expensive than a bootstrap circuit. Therefore, using a bias supply is rare in non-isolated gate drive circuits.

10.3 Adjusting for Gate Voltage

Negative gate voltages are popular in many high-power systems to increase the FET immunity to false turn-on. A negative gate voltage creates more margin between the off-state voltage and the threshold voltage of the FET. This voltage margin allows the FET to tolerate more miller current injection without causing a shoot-through. Negative gate voltages are popular for IGBTs and SiC FETs; many SiCFET data sheets list a negative gate bias as a requirement.

GaN FETs do not require a negative gate bias but using one offers the same benefits as SiCFETs. The downside to a negative gate voltage is that it increases the negative voltage during the dead time, which increases overcharging and losses. Using methods such as a Miller clamp, rather than a negative bias, boosts Miller immunity without having overcharging issues.

11 Summary

Bootstrap overcharge is a significant issue in GaN half-bridge circuits and other power switches. GaN half-bridge circuits have higher negative voltage and greater susceptibility to small changes in gate voltage, making them uniquely vulnerable to this issue. Many gate driver ICs offer efficient, integrated options within the gate driver and many ways to address these overcharge issues with discrete components.

12 References

- Texas Instruments, *Does GaN Have a Body Diode?—Understanding the Third Quadrant Operation of GaN*
- Texas Instruments, *Bootstrap Circuitry Selection for Half-Bridge Configurations*, application note
- Texas Instruments, *LM5113-Q1 Automotive 90-V, 1.2-A, 5-A, Half Bridge GaN Driver*, data sheet
- Texas Instruments, *LMG1205 100-V, 1.2-A to 5-A, Half Bridge GaN Driver With Integrated Bootstrap Diode*, data sheet
- Texas Instruments, *LMG1210 200-V, 1.5-A, 3-A Half-Bridge MOSFET and GaN FET Driver With Adjustable Dead Time for Applications Up to 50 MHz*, data sheet
- Texas Instruments, *UCC12041-Q1 High-Efficiency, Low-EMI, 3-kVRMS Basic Isolation DC/DC Converter*, data sheet

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