Application Note

Inverting Application for the TPSM365R6

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ABSTRACT

The TPSM365R6 is a 3.5 × 4.5 mm^2 0.6-A rated synchronous step-down power module that features a wide operating input range from 3.6 V to 65 V with an adjustable output voltage range from 1 V to 13 V. The TPSM365R6 can be configured into an inverting buck-boost (IBB) topology with the output voltage inverted with respect to input voltage. This application report shows how the TPSM365R6 EVM board can be configured for an inverting application. Additional level-shifter circuitry for the EN and PGOOD pins are also included in this application note.

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1 Inverting Buck-Boost Topology

1.1 Concept

In a standard buck configuration, the positive connection VOUT, is connected to the internal inductor, and the return connection is connected to the device ground.

In the IBB configuration, SYS_GND is connected to TPSM365R6's VOUT pin and the device return is now the negative output voltage, -VOUT. This shift in topology allows the output voltage to be inverted with respect to the input voltage. Pins connected to the TPSM365R6 IC GND in the standard buck configuration can still be referenced to the same pin in the inverting buck boost configuration. However, to use the EN and PGOOD pins, an appropriate level shifter must be added, which are detailed in the sections Section 5.1 and Section 5.2.

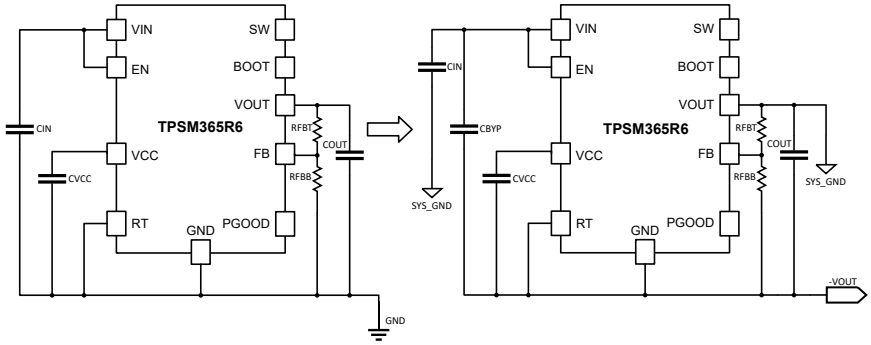

Figure 1-1. Converting From Buck to Inverting Buck-Boost Topology

1.2 Output Current Calculations

By changing the buck configuration into an IBB configuration, the average inductor current is affected. The output current capability in the IBB topology is less than the buck configuration. As a result, the maximum achievable output current is calculated using Equation 1.

$$I_{OUT(IBB)} = I_{L\_max} \times \left(1 - D\right) \tag{1}$$

- I_{L_max} is the maximum rated inductor current.
- The TPSM365R6 has an inductor with an I_{L_max} of 0.65 A.
- D is the operating duty cycle

The operating duty cycle for an inverting buck-boost converter can be found with Equation 2.

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN} \times \eta} \tag{2}$$

- In Equation 2 V_{OUT} is represented with a negative value.

The efficiency term in Equation 2 adjusts the equations in this section for power conversion losses and yields a more accurate maximum output current result. This efficiency is found by averaging the efficiency of the TPSM365R6 buck in its standard configuration. Use Equation 1 and Equation 2 to calculate the recommended maximum output current. For example, with an input voltage of 24 V, an output voltage of –12 V, and an estimated efficiency of 0.9, the duty cycle will be calculated with Equation 2 as:

$$D = \frac{-12}{-12 - 24 \times 0.9} = 0.357 \tag{3}$$

The result of Equation 4 is then used to calculate the maximum achievable output current with Equation 1:

$$I_{OUT(IBB)} = 0.65 \times \left(1 - 0.357\right) = 0.42\ A \tag{4}$$

Table 1-1 provides a general idea of the maximum output current allowed from the TPSM365R6.

Table 1-1. Recommended Maximum Output Current Calculations for TPSM365R6 in IBB Configuration

V_{OUT} (V)	V_{IN} (V)	I_{L_max} (A)	η	D	I_{OUT} (A)
–1.8	24	0.65	0.6	0.111	0.58
–2.5	24	0.65	0.7	0.130	0.57
–3.3	24	0.65	0.7	0.164	0.54
–5	24	0.65	0.8	0.210	0.52
–12	24	0.65	0.9	0.357	0.42

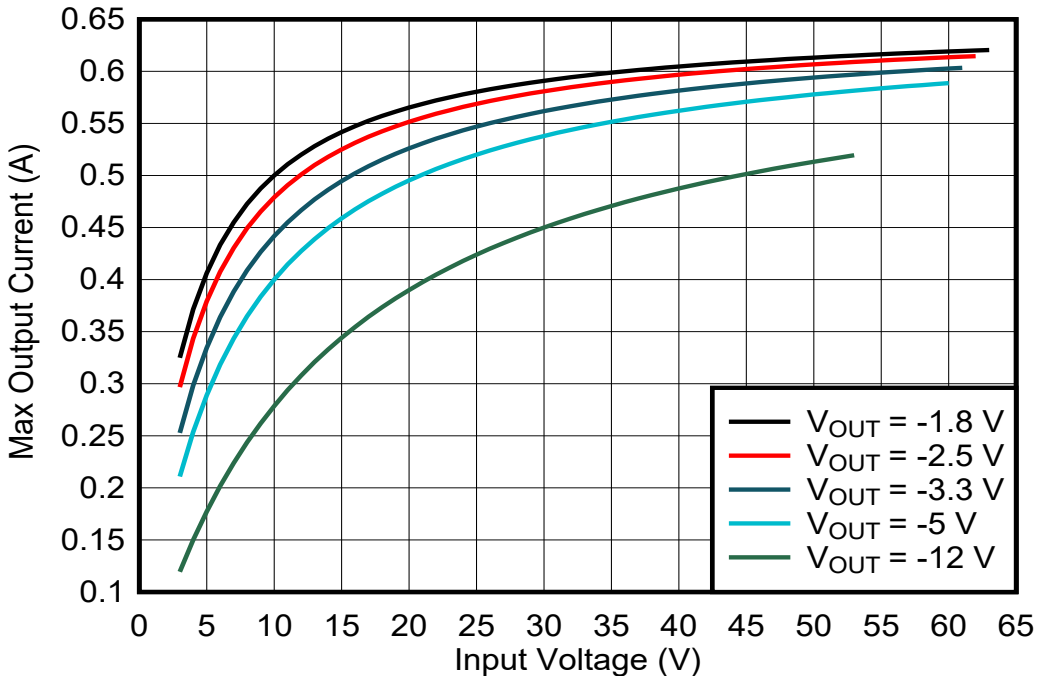

Figure 1-2. Recommended Maximum Output Current for TPSM365R6

1.3 V_{IN} and V_{OUT} Range in Inverting Configuration

In the standard configuration, the TPSM365R6 IC can tolerate a 65 V difference between its VIN and IC GND pins. In an IBB, however, TPSM365R6 IC GND is referenced to the negative output voltage pin, –VOUT, see Figure 1-1. The TPSM365R6 will experience a potential difference of VIN to –VOUT between its VIN and TPSM365R6 IC GND pins, which effectively limits the input voltage range of the TPSM365R6 module in its inverting buck-boost configuration. For example, for an output voltage of –12 V, the maximum input voltage will be 53 V, as this results in a 65 V potential difference between the TPSM365R6 IC's VIN and GND pins. The output voltage range in the TPSM365R6 IBB topology is –1.8 V to –13 V.

2 Design Considerations

2.1 Additional Bypass Capacitor and Schottky Diode

You can use a ceramic bypass capacitor, CBYP, with a minimum capacitance of 10 µF, to decrease incoming power supply noise. The voltage rating of CBYP must be taken into consideration because this capacitor will experience stress equal to the full voltage range between VIN and –VOUT. In general, use a capacitor with at least twice the voltage rating of the full expected voltage range.

However, the inclusion of the CBYP capacitor introduces an AC path from VIN to –VOUT and might worsen the transient response. When VIN is applied to the circuit, the dV/dt across the bypass capacitor creates a current that must return to ground to complete the loop. This current might flow through the internal low-side body diode of the MOSFET and the inductor to return to ground. TI recommends having a Schottky diode between the -VOUT and SYS_GND to avoid damaging the aforementioned internal low-side MOSFET. Additionally, this Schottky diode will reduce the potential positive output voltage spike at –VOUT caused by a quick VIN startup as shown in Figure 2-2. If large line transients are expected, increase the output capacitance to keep the output voltage within acceptable levels.

Note that for the system to be stable, there must be an input power supply capacitor to help dampen the high-frequency noise that can couple into the circuit. Adding an electrolytic capacitor, CBULK, with moderate ESR can help dampen any input supply ringing caused by long power leads. This CBULK capacitor should be added across V_{IN} and SYS_GND.

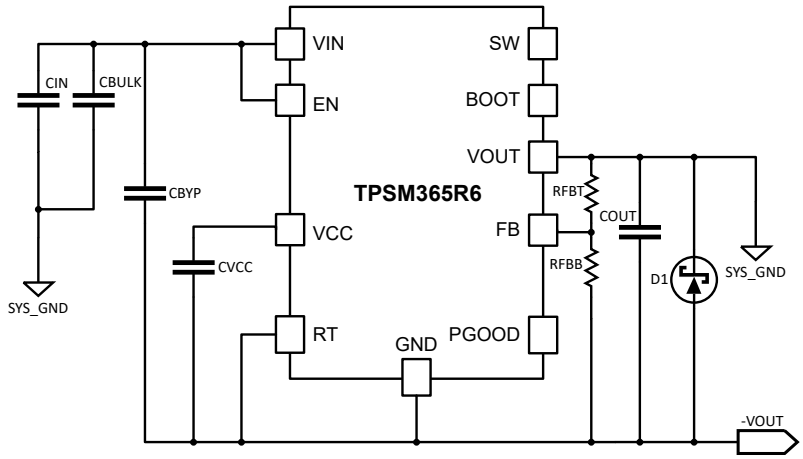

Figure 2-1. TPSM365R6 IBB with Schottky Diode and Bulk and Bypass Capacitors

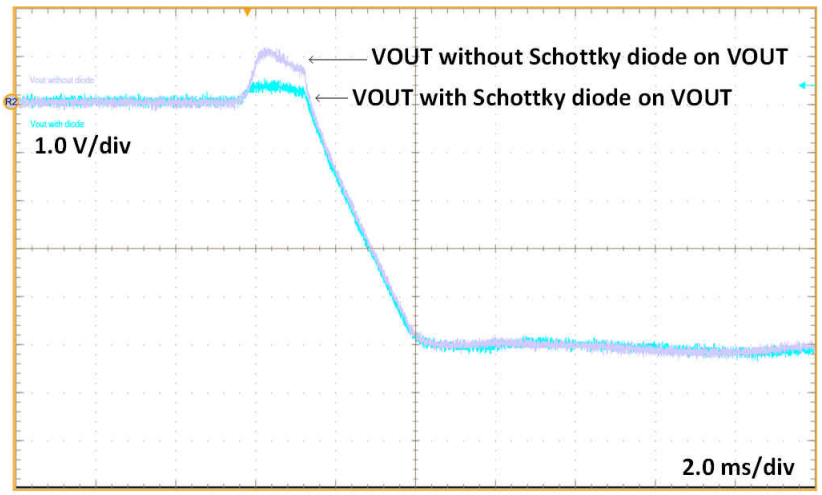

Figure 2-2. TPSM365R6 IBB Startup with Schottky Diode

2.2 Start-up Behavior and Switching Node Consideration

The voltage on the SW pin switches from VIN to –VOUT in an IBB topology instead of from VIN to TPSM365R6 IC GND in a buck application. When the high-side MOSFET turns on, the SW node sees the input voltage. When the low-side MOSFET turns on, the SW node detects the device's SYS_GND, which is tied to the negative output voltage pin, –VOUT. During start-up, VIN rises to achieve the desired input voltage. VOUT starts ramping down after the EN pin voltage exceeds its threshold level and VIN exceeds its UVLO threshold. As -VOUT continues to ramp down, the low level of the SW node follows -VOUT. Figure 2-3 shows the resulting normal, smooth start-up of the output voltage.

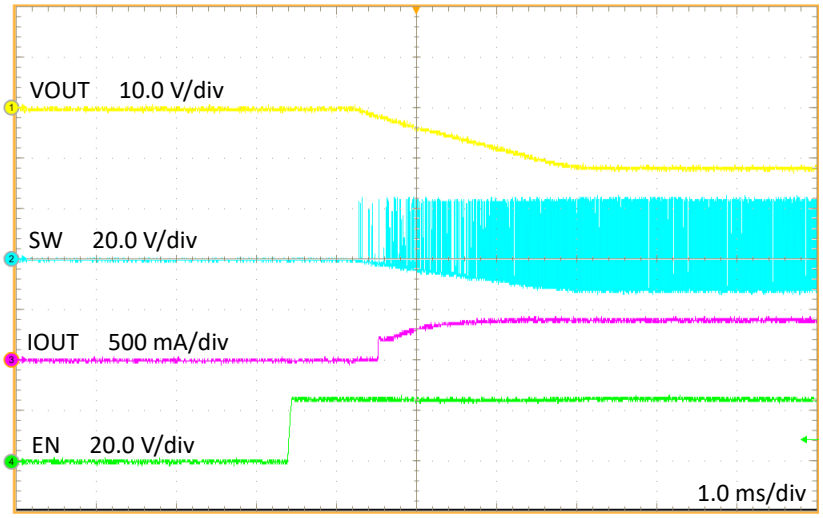

Figure 2-3. SW Node Voltage During Start-Up

3 External Components

The TPSM365R6 contains integrated power MOSFETs and a shielded inductor. As a result, the inverting buck-boost application only requires as few as four external components. The required external components are its input and output capacitance as well as an appropriately sized bypass capacitor. When using the TPSM365R6 EVM, most of these required components are already included; however a new set of input capacitors are required to be placed between the VIN and VOUT pins. TI also recommends that the bypass capacitor between the VIN and the TPSM365R6 IC GND pin be increased in capacitance to improve the inverting buck-boost's load transient performance. More information about these components can be found in Section 2.1 and Section 3.2 as well as in the *TPSM365R6's* data sheet. Performing a load-transient test and frequency sweep is recommended to evaluate stability.

3.1 Capacitor Selection

Ceramic capacitors with low equivalent series resistance (ESR) are recommended to achieve low output voltage ripple. X5R- or X7R-type dielectrics are recommended for the stable capacitance versus temperature characteristics and DC bias. The higher the DC voltage applied to the capacitor, the less the effective capacitance. A minimum of 2.2-µF capacitance for the input capacitor, CIN, and a 0.1-µF capacitance for a parallel high-frequency input capacitor are required for proper operation.

The CIN from the standard buck evaluation module acts as the bypass capacitor in the inverting buck boost configuration as shown in Figure 1-1.This included capacitor will have an inherent 2.2-µF from the evaluation board, but more bypass capacitance can be added to improve load transient performance.

Evaluating the Bode plot of the circuit under normal operation can also provide insight on the stability of the system. Having a stable phase margin provides the basis for the minimum recommended output capacitance for the inverting buck-boost at different output voltages. Refer to Table 3-1 for the minimum recommended output capacitance.

3.2 System Loop Stability

Stability is an important factor in the system when adding more output capacitance. The general rule of thumb for a stable design is a desired phase margin (PM) of at least 45° and under 70°. In some cases, a feed forward capacitor, C_{ff}, is necessary to maintain the stability of the system's open loop conditions. The TPSM365R6 EVM includes a 10-µF feed forward capacitor inherently. As a general rule of thumb, Equation 5 can be used to determine valid values for C_{ff}. C_{ff} is to be placed across the RFBT resistor shown in Figure 1-1.

$$C_{ff} = \frac{1}{2\pi \times R_{FBT} \times 2f_{c\_noC_{ff}}} \quad (5)$$

- $f_{c\_noC_{ff}}$ is the crossover frequency of the device without C_{ff}

Table 3-1 shows the theorized PM and capacitance with respect to VIN, –VOUT, and IOUT. With the 10-µF feed forward capacitor included on the TPSM365R6 EVM, these capacitor values and associated voltage ratings provide the desired phase margins.

Table 3-1. Phase Margin of IBB TPSM365R6

VIN	–VOUT	COUT	Voltage Rating (V)	PM (°)
24	–2.5	10	25	56.59
24	–3.3	10	25	63.47
24	–5	22	25	66.45
24	–12	44	25	60.40

4 Typical Performance

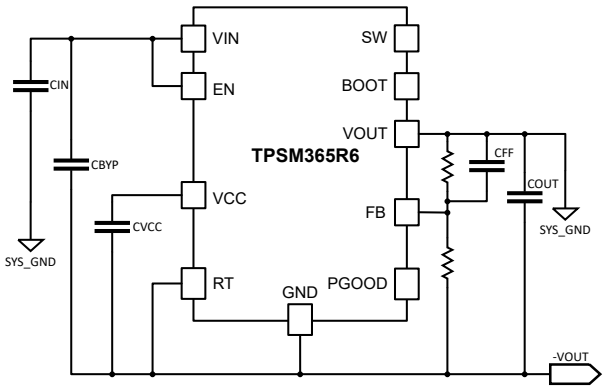

Figure 4-1. Basic Schematic Used

DSGNR	Part Number	Description	MFR	QTY
CIN	C3225X7R2A225K230AM	2.2 uF, 100 V, X7R, 1210	TDK	1
	GRM188R72A104KA35J	0.1 uF, 100 V, X7R, 0603	MuRata	1
CFF	CGA2B2C0G1H100D050BA	10 pF, 50 V, C0G/NP0, 0402	TDK	1
CBYP	C3225X7R2A225K230AB	2.2 uF, 100 V, X7R, 1210	TDK	1
CVCC	C1608X7R1C105K080AC	1 uF, 16 V, X7R, 0603	TDK	1
COUT	C3225X7R1E226M250AB	22 uF, 25 V, X7R, 1210	TDK	2

Figure 4-2. Capacitors Used

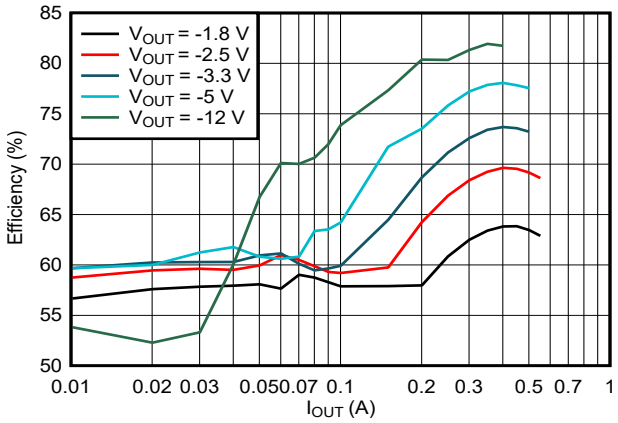

Figure 4-3. Efficiency vs. Load Current at V_{IN} = 24 V

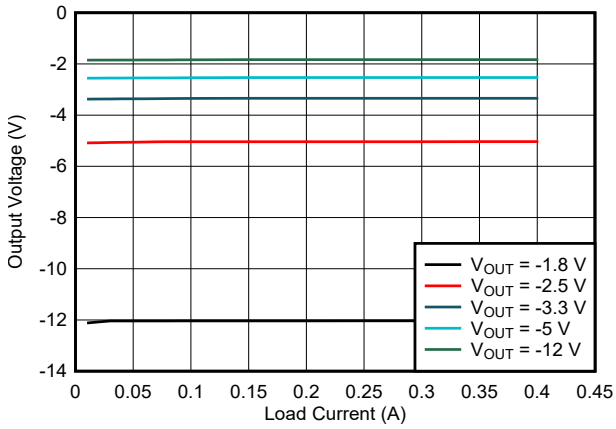

Figure 4-4. Load Regulation at V_{IN} = 24 V

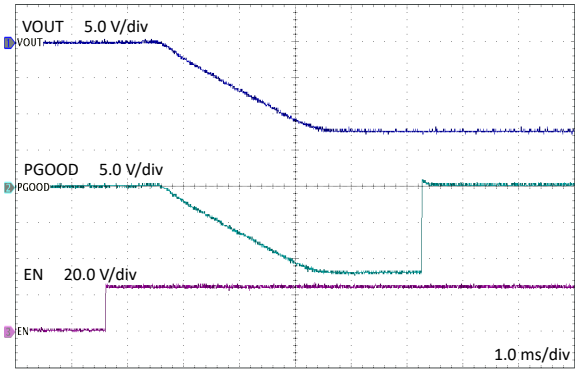

Figure 4-5. Start-up on V_{IN} = 24 V, V_{OUT} = –12 V, Expected Performance With no Level Shifters

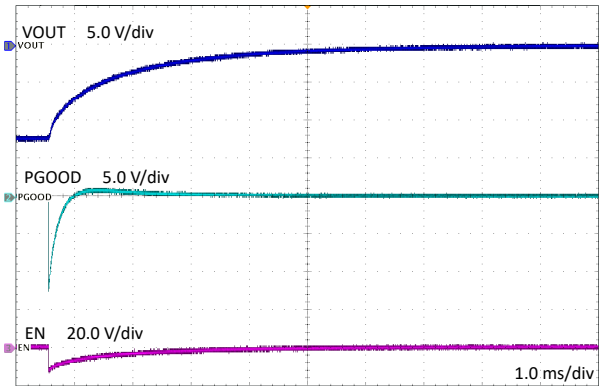

Figure 4-6. Shutdown on V_{IN} = 24 V, V_{OUT} = –12 V, Expected Performance With no Level Shifters

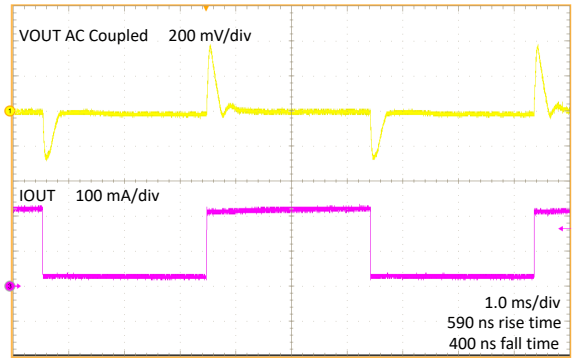

Figure 4-7. Load Transient Response, 100 mA to 410 mA With V_{IN} = 24 V, V_{OUT} = –12 V

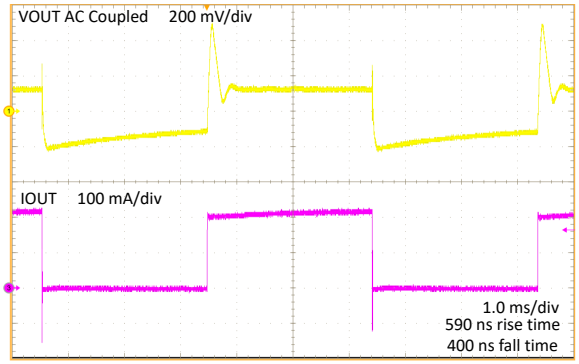

Figure 4-8. Load Transient Response, 0 mA to 410 mA With V_{IN} = 24 V, V_{OUT} = –12 V

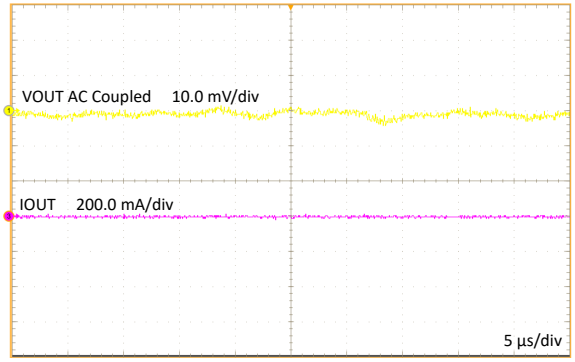

Figure 4-9. Output Voltage Ripple, V_{IN} = 24 V, V_{OUT} = –12 V, I_{OUT} = 0 mA

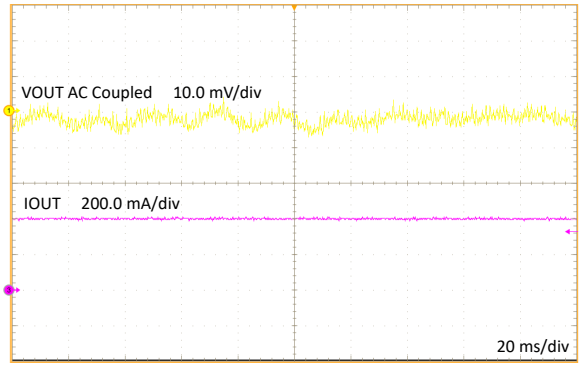

Figure 4-10. Output Voltage Ripple, V_{IN} = 24 V, V_{OUT} = –12 V, I_{OUT} = 410 mA

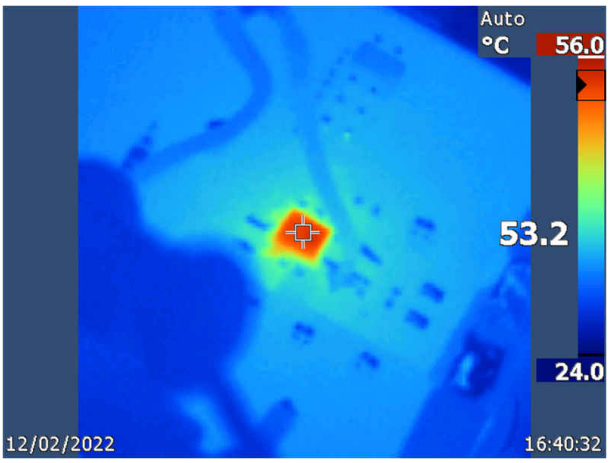

Figure 4-11. Temperature Response, V_{IN} = 24 V, V_{OUT} = –5 V, I_{OUT} = 450 mA

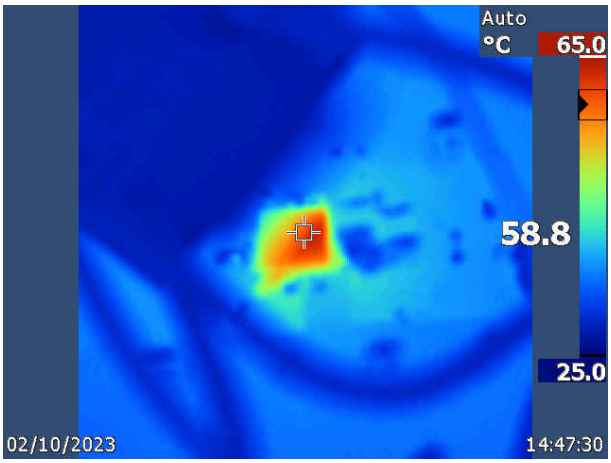

Figure 4-12. Temperature Response, V_{IN} = 24 V, V_{OUT} = –12 V, I_{OUT} = 410 mA

5 Digital Pin Configurations

5.1 Digital Input Pin

The TPSM365R6 has a digital input pin (EN) that can be used to turn the output of the device on and off. In the TPSM365R6 buck configuration, the specified typical threshold voltages for the EN pin with respect to TPSM365R6 IC GND is considered high above 1.36 V and low below 0.4 V. However, in the inverting buck-boost configuration, EN is now referenced to –VOUT voltage, not the TPSM365R6 IC GND; therefore, the threshold for the EN pin to be considered high is 1.36 V + –VOUT, and the threshold for the EN pin to be considered low is 0.4 V + -VOUT. For example, if –VOUT = –12 V, EN will be considered high for voltages above –10.64 V and low for voltages below –11.6 V. Thus, at startup a negative output voltage will cause EN to turn on, but will require a voltage of at least 0.4 V + –VOUT to shutdown the device. This behavior can cause difficulties disabling the part, because in many applications the voltage rail supplying the EN signal will not be able to produce the negative voltage required to turn EN low.

A relatively simple level shifter can alleviate any problems associated with the EN threshold voltages by eliminating the need for negative EN signals. Figure 5-1 shows the required connections to create the EN pin level shifter.

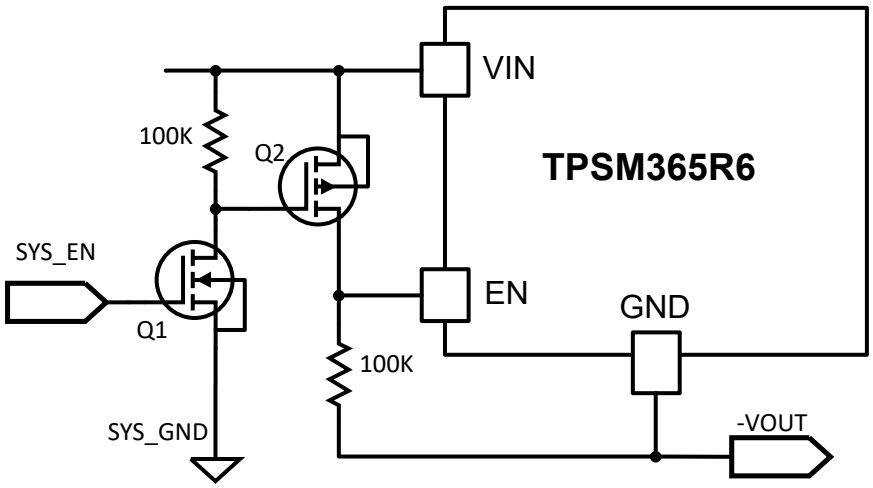

Figure 5-1. EN Pin Level Shifter

Table 5-1. Logic States with EN Level Shifter

SYS_EN	LOW	HIGH
Q1	OFF	ON
Q2	OFF	ON
EN Pin	LOW	HIGH

The positive signal (SYS_EN) that originally drove EN is now tied to the gate of Q1 in this level shifter. When SYS_EN is set to SYS_GND, Q1 turns off. Subsequently, Q2 detects no potential difference between its gate and source and also remains off. In this state, the EN pin detects -VOUT, which is below the low level threshold and disables the device.

When SYS_EN provides enough positive voltage to between Q1's gate and source to turn Q1 on, the gate of Q2 is pulled to SYS_GND through Q1. This drives a negative potential difference between Q2's gate and source, turning it on. Consequently, EN is tied to VIN through Q2, and the pin is above the high level threshold, causing the device to turn on.

It is important to select Q2 MOSFETs with the proper voltage ratings for the expected application conditions. Additional Zener diodes and/or a resistor divider can be used to lower the potential of Q2's gate. Ensure that the Q2 limits found in the MOSFET's data sheet are adhered to in both the on and off states of the IC.

The SYS_EN signal activates the EN pin level shifter circuit and swings the EN pin voltage to VIN and -VOUT, properly enabling and disabling the device. EN Pin Level Shifter on Start-Up and EN Pin Level Shifter on Shutdown show the behavior of the device with the EN pin level shifter installed.

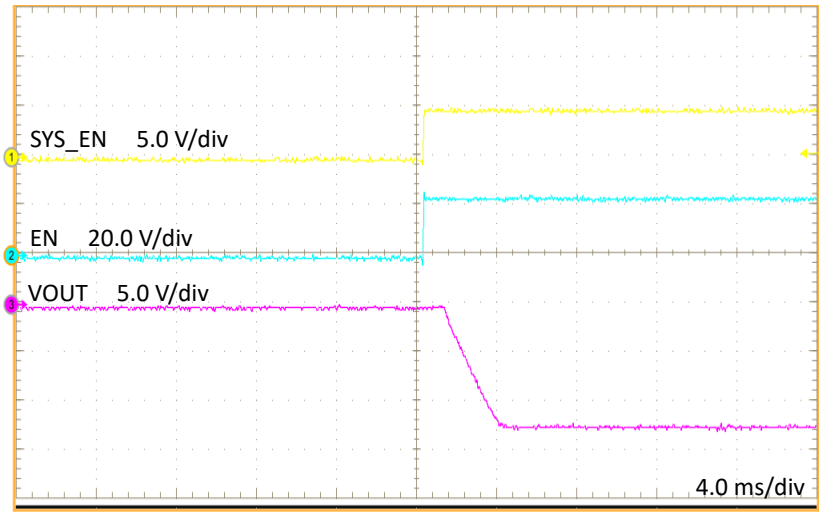

Figure 5-2. EN Pin Level Shifter on Start-Up

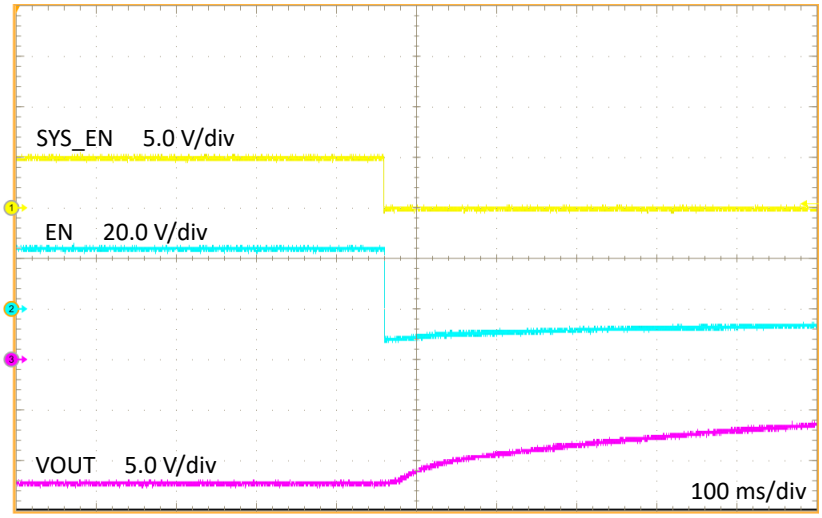

Figure 5-3. EN Pin Level Shifter on Shutdown

5.2 Power-Good Pin

The TPSM365R6 has a built-in power-good (PGOOD) function to indicate whether the output voltage has reached its target voltage or not. The PGOOD pin is an open-drain output that requires a pullup resistor. In the standard buck configuration, the PGOOD pin would be referenced to the TPSM365R6 IC GND pin, and output a high signal when the device reaches the proper output voltage. However, in the inverting buck boost configuration, as the TPSM365R6's IC GND pin turns into the -VOUT pin, the PGOOD pin will also be referenced to –VOUT. The device then pulls PGOOD to –VOUT when it is low.

This behavior can cause difficulties in reading the state of the PG pin, because in some applications the IC detecting the polarity of the PGOOD pin may not be able to withstand negative voltages. The level shifter circuit

alleviates any difficulties associated with the PGOOD pin voltages by eliminating the negative output signals of the PGOOD pin. If the PGOOD pin functionality is not needed, it can be left floating or connected to –VOUT. Note, to avoid violating the absolute maximum rating, the PGOOD pin must not be driven more than 20 V above the negative output voltage. Figure 5-4 shows the required connections to make the PGOOD pin level shifter.

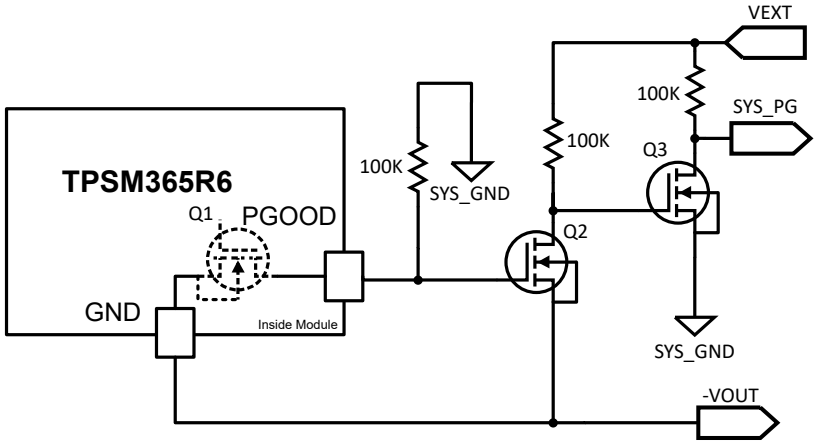

Figure 5-4. PGOOD Pin Level Shifter

Table 5-2. Transistor States During PGOOD Level Shifter Behavior

POWER	NOT GOOD	GOOD
Q1	ON	OFF
Q2	OFF	ON
Q3	ON	OFF
SYS_PG	LOW	HIGH

Internally, the PGOOD pin is connected to an N-channel MOSFET (Q1). By tying the PGOOD pin to the gate of Q2, Q2 will turn off when the PGOOD pin is pulled to -VOUT, as no potential difference will be detected across Q2's gate and source. As a result, Q3 will turn on, because the potential difference between it's gate and source will be VEXT. Note that the VEXT voltage must provide enough potential difference between Q3's gate and source to turn on Q3. The outgoing SYS_PG signal is then pulled to SYS_GND.

When –VOUT has reached its target value, Q1 turns on, which pulls the gate of Q2 to SYS_GND. Consequently, Q2 turns on as its gate voltage is higher than its source voltage. This pulls the gate of Q3 to -VOUT, turning Q3 off as its gate is now at a lower potential than its source, which is tied to SYS_GND. With Q3 off, the outgoing SYS_PG signal is pulled to VEXT.

The output voltage activates the PGOOD pin level shifter circuit and swings the output signal, SYS_PG from VEXT to SYS_GND, properly showing if the device's output is at its targeted output voltage or not. Figure 5-5 and Figure 5-6 show the behavior of the device with the PGOOD pin level shifter installed.

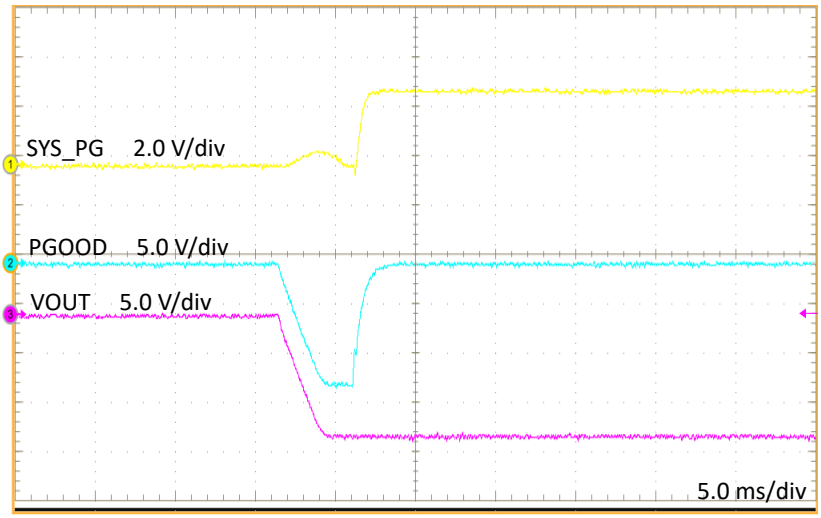

Figure 5-5. PG Pin Level Shifter on Start-Up

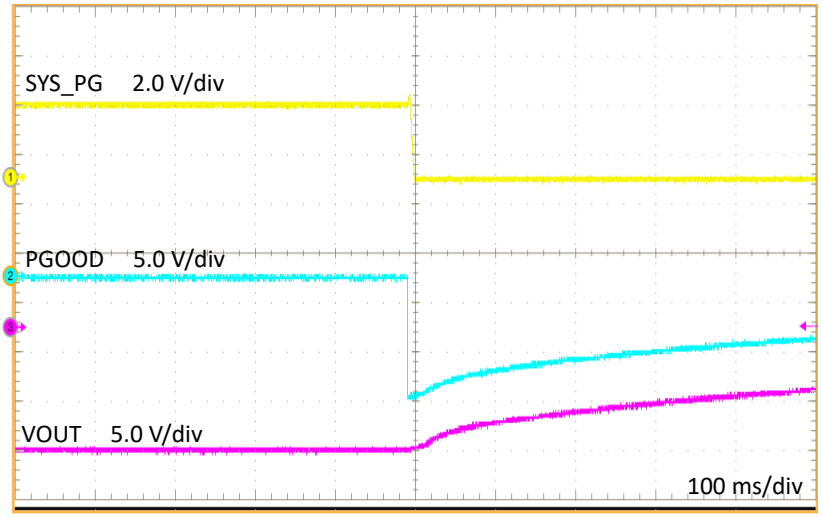

Figure 5-6. PG Pin Level Shifter on Shutdown

6 Conclusion

The TPSM365R6 buck power module can be configured into an IBB topology to generate a negative output voltage by switching the output and ground connections. The input voltage range is lowered because the device now has a reference point set to the negative output voltage rather than ground. Additionally, the inductor peak current is much higher, effectively lowering the recommended maximum output current operating range for all output voltages. Converting an original buck topology into an IBB topology will result in a lowered input voltage range and maximum output current. This application report explains the IBB topology and how to select the proper external components to keep the system stable. Data from the test circuits are measured and provided.

7 References

1. Texas Instruments, *Create an Inverting Power Supply From a Step-Down Regulator* application note.
2. Texas Instruments, *TPSM365R6 65-V, 0.6-A Synchronous Buck Converter Power Module* data sheet.
3. Texas Instruments, *Using a buck converter in an inverting buck-boost topology*, analog design journal.
4. Texas Instruments, *Using the TPS5430 as an Inverting Buck-Boost Converter*, application note.
5. Texas Instruments, *Inverting Application for the LMZM33602 and LMZM33603*, application note.

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