

Camera Module Shutdown Power Sequence Solution



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ABSTRACT

Most image sensors in the market have specific requirements for the power up sequence of supply rails, but not for the power down sequence. As a result, many manufacturers will ignore the power down sequence in their design of the power supply. However, it is increasingly common for image sensors to indicate power down timing requirements of each supply rail in the data sheet. For such image sensors, the designer will need to implement a robust shutdown sequence. This application note summarizes three common approaches to image sensor power supply design, and how they can meet precise power up and power down timing requirements of the sensor.



Table of Contents

1 Introduction	2
2 Power Solutions	3
2.1 Discrete Power.....	3
2.2 Discrete Power with Voltage Supervisor.....	3
2.3 Integrated Power with Camera Module PMIC.....	4

List of Figures

Figure 1-1. Power Up Sequence Requirement.....	2
Figure 1-2. Power Down Sequence Requirement.....	2
Figure 2-1. Typical Discrete Power Tree for Automotive Camera Modules.....	3
Figure 2-2. Discrete Power Tree with Supervisor.....	3
Figure 2-3. TPS65033x-Q1 Power Tree for Camera Modules.....	4
Figure 2-4. TPS650330-Q1 Programmable Power Up Sequence.....	5
Figure 2-5. TPS650330-Q1 Programmable Power Down Sequence.....	5

List of Tables

Table 2-1. Initiate a Controlled Power Down on the TPS650330-Q1 via I2C.....	4
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1 Introduction

This application note uses a typical image sensor to assess three feasible power solutions that need to support the sensor's power sequence requirements. These requirements can be found in the sensor data sheet. [Figure 1-1](#) demonstrates the power up sequence requirement of a typical image sensor. AVDD 2.8 V must power up first, followed by DOVDD 1.8 V, and then DVDD 1.2 V.

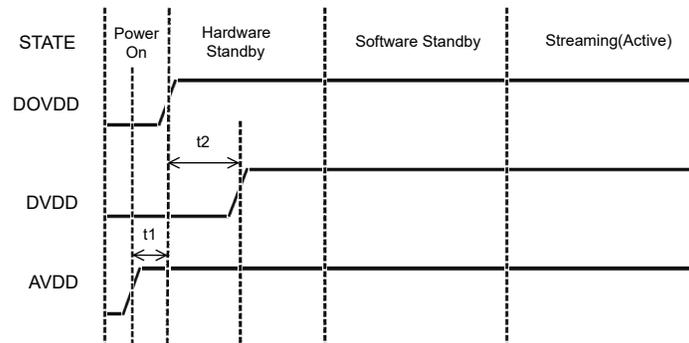


Figure 1-1. Power Up Sequence Requirement

[Figure 1-2](#) is the power down sequence requirement of the image sensor. The sequence is the reverse order of the power up sequence: DVDD 1.2 V, followed by DOVDD 1.8 V, and lastly AVDD 2.8 V.

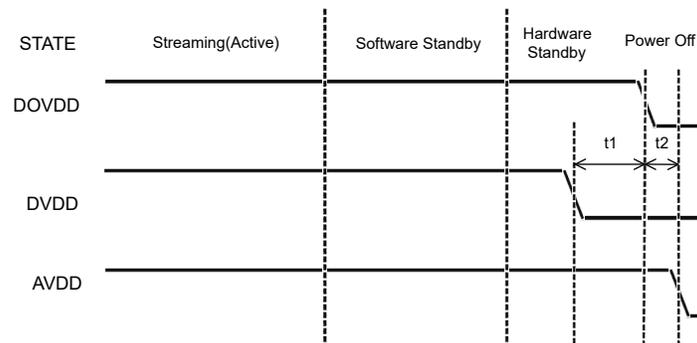


Figure 1-2. Power Down Sequence Requirement

Achieving the power up sequence is often a straightforward process. The bigger design challenge is reversing this sequence to meet the power down requirements. The following sections discuss this challenge in the context of three common power solutions for image sensors. These solutions consist of:

1. A discrete solution using regulator power good and enable pins.
2. A discrete solution using a voltage supervisor.
3. A Power Management Integrated Circuit (PMIC) using built-in, programmable power sequencing.

2 Power Solutions

2.1 Discrete Power

In a power solution using discrete regulators, the power good (PG) output of the previous regulator in the sequence can drive the enable (EN) pin of the next regulator. In this application note, the first regulator is a switching regulator that converts 12 V or 5 V into 3.3 V, for example TI hero products LMR33620 and TPS62160. A low-noise, high-PSRR LDO, such as the LP5907, converts 3.3 V into the AVDD 2.8 V rail for the image sensor. Secondary regulators are also used to convert 3.3 V into DOVDD 1.8 V and DVDD 1.2 V. DOVDD 1.8 V could be supplied by the TPS62260 or TPS62065, while a low cost LDO like the TLV702 or TPS793 supplies DVDD 1.2 V. In this solution, the power up sequence is achieved by routing PG outputs to EN inputs. However, this approach alone cannot satisfy the power down sequence requirement, which must be in the reverse order of the power up sequence.

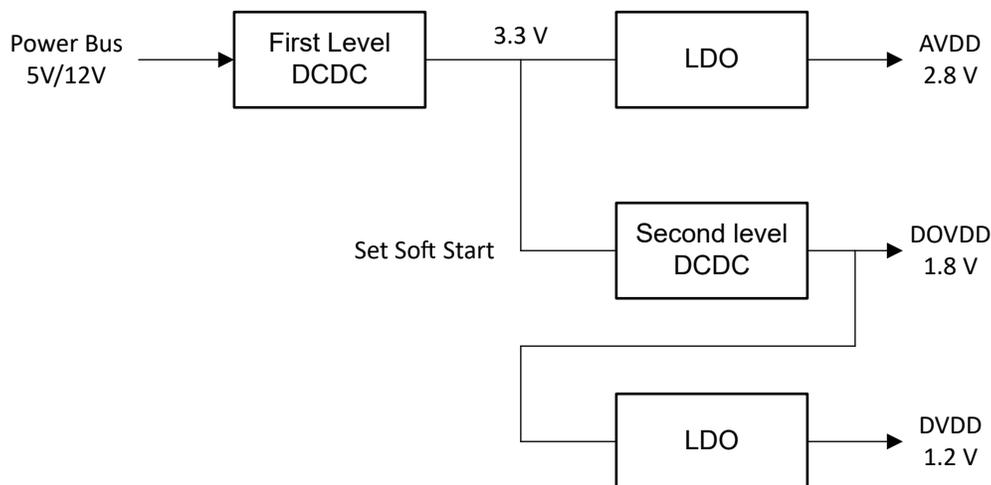


Figure 2-1. Typical Discrete Power Tree for Automotive Camera Modules

Capacitors would need to be added control the delay in this circuit to indirectly satisfy the shutdown sequence requirement. This adds cost and size to the solution, which are both critical factors in camera module design.

2.2 Discrete Power with Voltage Supervisor

An alternative to adding capacitance is implementing a voltage supervisor, for example TI's TPS3840 or TPS3808, as shown in [Figure 2-2](#). The supervisor RESET pin is used to enable and disable the LDO supplying DVDD 1.2 V. This process allows DVDD 1.2 V to power down first without the need for additional capacitors. The increase to the solution size is reduced, but not minimized, and the supervisor still results in a cost increase.

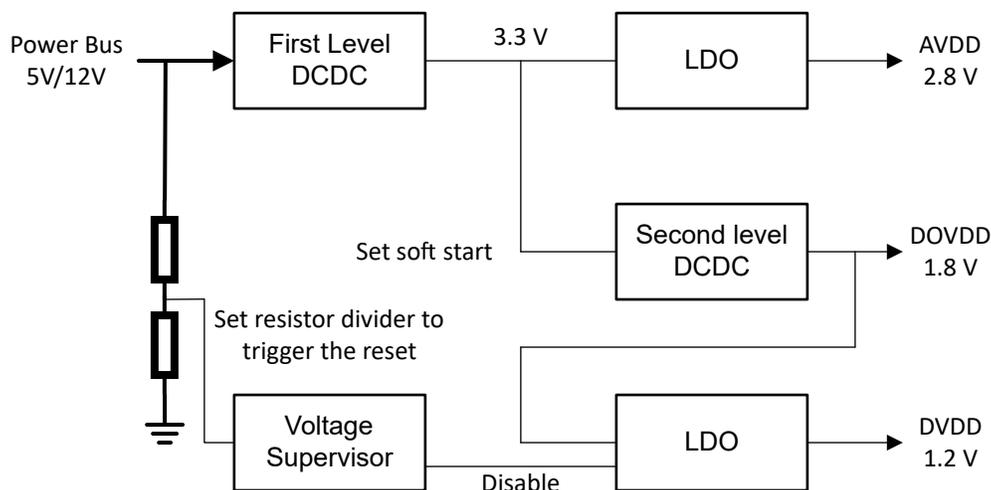


Figure 2-2. Discrete Power Tree with Supervisor

2.3 Integrated Power with Camera Module PMIC

TI offers PMICs intended for 3.3 V, 5 V and 12 V camera applications. The TPS65000 family covers 3.3 V and 5 V input applications, while the TPS650330 family covers 5 V and 12 V input applications. Both of these solutions have the capability to meet power up and power down sequencing requirements. The TPS65000x devices have EN pins for each regulator that can be sequenced similar to the discrete approach discussed in [Section 2.1](#) and [Section 2.2](#). The TPS65033x devices control the power sequence through internal register settings and Non-Volatile Memory (NVM). The engineer can program a custom power sequence or use an existing part number compatible with specific image sensors. Refer to the [Camera PMIC Spin Selection Guide](#) for current options.

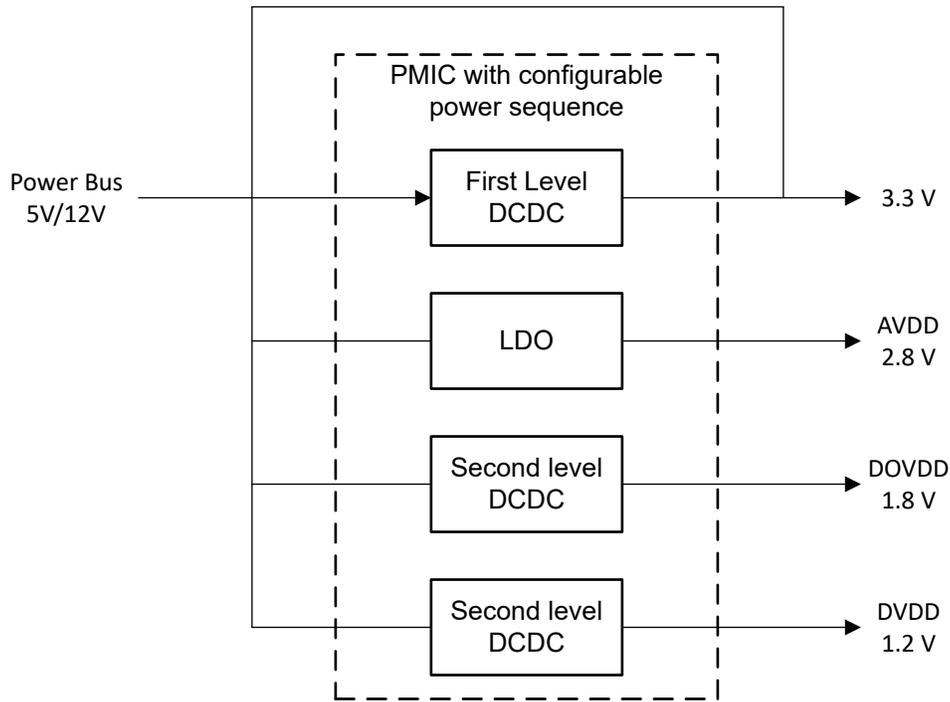


Figure 2-3. TPS65033x-Q1 Power Tree for Camera Modules

The TPS650330-Q1 device powers up according to the default power sequence register settings. The default power down sequence can be configured in the reverse order of the power up sequence, or it can be configured to meet the imager and/or serializer power down sequence requirements. To initiate a controlled power down sequence via I2C communication, unlock the device control registers and set the PWR_ON bit to 0. Input power must remain present throughout the shutdown to maintain the desired power down sequence.

Table 2-1. Initiate a Controlled Power Down on the TPS650330-Q1 via I2C

Write Transaction	Device Address (7-bit)	Register Address	Write Data
1	0x60	0x02	0xDD
2	0x60	0x05	PWR_ON = '0'

This is demonstrated using the PMIC-Serializer base-board in reference designs [TIDA-050035](#) and [TIDA-050036](#). The default power sequence settings are re-programmed to match the typical image requirements from [Figure 2-1](#) and [Figure 2-2](#). The power up sequence in [Figure 2-4](#) is achieved by ramping the Power Over Coax (POC) input voltage. The power down sequence in [Figure 2-5](#) is achieved by executing the I2C transactions described in [Table 2-1](#) via the FPD-Link III SERDES back-channel.

The fully integrated automotive camera PMIC, TPS650330-Q1, meets strict power up and power down sequence requirements through internal register settings, removing the need for external supervisors and PCB routing. This solution optimizes size, performance, and cost of the camera module.



Figure 2-4. TPS650330-Q1 Programmable Power Up Sequence



Figure 2-5. TPS650330-Q1 Programmable Power Down Sequence

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