

Application Report

LM25183, LM25184, LM25183-Q1, and LM25184-Q1

Functional Safety FIT Rate, FMD and Pin FMA



Table of Contents

1 Overview.....	2
2 Functional Safety Failure In Time (FIT) Rates.....	3
3 Failure Mode Distribution (FMD).....	4
4 Pin Failure Mode Analysis (Pin FMA).....	5

Trademarks

All other trademarks are the property of their respective owners.

1 Overview

This document contains information for LM25183, LM25184, LM25183-Q1, and LM25184-Q1 (WSON package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

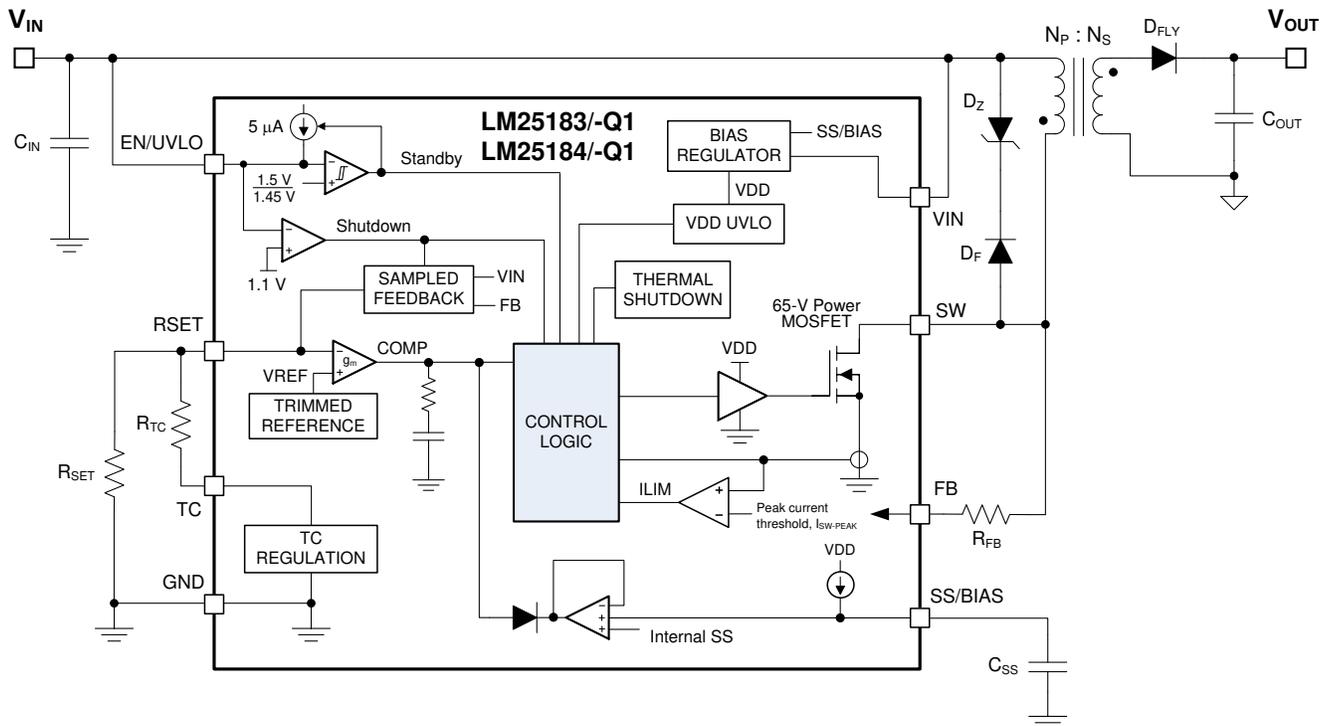


Figure 1-1. Functional Block Diagram

LM25183, LM25184, LM25183-Q1, and LM25184-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM25183, LM25184, LM25183-Q1, and LM25184-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total Component FIT Rate	13
Die FIT Rate	7
Package FIT Rate	6

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 300 mW
- Climate type: World-wide Table 8
- Package factor (λ_3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM25183, LM25184, LM25183-Q1, and LM25184-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No SW output	45%
SW output not in specification – voltage or timing	40%
SW power FET stuck on	5%
EN/UVLO false trip or fails to trip	5%
Short circuit to any two pins	5%

The FMD in [Table 3-1](#) excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM25183, LM25184, LM25183-Q1, and LM25184-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 4-1](#) shows the LM25183, LM25184, LM25183-Q1, and LM25184-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM25183, LM25184, LM25183-Q1, and LM25184-Q1 data sheets.

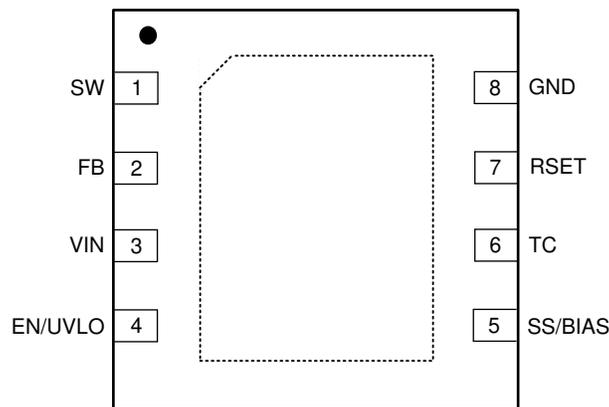


Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	VOUT = 0 V; Damage to transformer	A
FB	2	VOUT = 0 V; Damage VIN to FB	A
VIN	3	VOUT = 0 V	B
EN/UVLO	4	VOUT = 0 V; Shutdown operation	B
SS/BIAS	5	VOUT = 0 V if short during start-up. VOUT normal if short during steady-state	B
TC	6	Temperature compensation disabled; VOUT target will be slightly different due to $R_{tc} R_{set}$	C
RSET	7	$V_{OUT} = I_{SW-PEAK} \cdot t_{OFF} \cdot R_{load} \cdot N_{PS} / 240 \mu s$; 120 μs switching	B
GND	8	Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	VOUT = 0 V; No switching	B
FB	2	VOUT = 0 V; 120 μ s switching	B
VIN	3	VOUT = 0 V	B
EN/UVLO	4	Shutdown or Regulating since EN is high impedance	B
SS/BIAS	5	VOUT regulating; Internal SS only	C
TC	6	VOUT regulating; Temperature compensation disabled	C
RSET	7	VOUT = 0 V; VOUT cannot be sensed	B
GND	8	Floating GND	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	VOUT = 0 V; Damage VIN to FB diode	A
FB	2	VOUT = 0 V; VOUT cannot be sensed	B
VIN	3	VOUT regulating; Always in ACTIVE mode	C
EN/UVLO	4	--	--
SS/BIAS	5	Current limit threshold will be lower	B
TC	6	$V_{OUT} = I_{SW-PEAK} * t_{OFF} * R_{load} * N_{PS} / 240 \mu s$ depending on TC; VOUT cannot be sensed	B
RSET	7	$V_{OUT} = I_{SW-PEAK} * t_{OFF} * R_{load} * N_{PS} / 240 \mu s$ depending on TC; VOUT cannot be sensed	B
GND	8		--

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	VOUT = 0 V; Damage SW to GND	A
FB	2	VOUT = 0 V; VOUT cannot be sensed	B
VIN	3	Normal Operation	D
EN/UVLO	4	VOUT regulating; Always in ACTIVE mode	C
SS/BIAS	5	Damage to 15 V ESD on SS/BIAS	A
TC	6	Damage to 5 V ESD on TC	A
RSET	7	Damage to 5 V ESD on RSET	A
GND	8	VOUT = 0 V	B

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated