Application Note

How to Design a Boost Converter Using LM5157x, LM5158x

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ABSTRACT

The LM5157x/LM5158x device is a wide input range, non-synchronous converter with an integrated power switch. The common configurations include Boost, Flyback and SEPIC topologies. This report leads the reader through the configuration and design of a boost converter using LM5157x/LM5158x. The design example is used to create the LM5157EVM-BST evaluation module and the results are presented in *LM5157EVM-BST User's Guide*. This report only focuses on the design steps and considerations of implementing LM5157x/LM5158x as a boost converter. The basic concept and operation of a boost converter can be found in *Understanding Boost Power Stages in Switchmode Power Supplies*.

Table of Contents

List of Figures

List of Tables

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1 LM5157 Boost Design Example

This design example walks through the typical design procedures and calculations to implement a non-synchronous Boost converter with LM5157. The design with LM51571, LM5158, and LM51581 is very similar. The configuration is designed to provide a regulated 12 V of up to 1.6 A load current from an unregulated 6 V rail (3 V-9 V) (load derated by half at input below 6 V). A switching frequency of 2.1MHz is selected to avoid interference in the AM band (530kHz to 1.8MHz). The parameters are presented in Table 1-1 and the component selection is discussed in Section 2.

Table 1-1. Design Parameters

PARAMETER	SPECIFICATIONS
V_{SUPPLY}	3 V to 9 V
V_{LOAD}	12 V
I_{LOAD}	1.6 A (V_{SUPPLY}= 6 V to 9 V)
	0.8 A (V_{SUPPLY}= 3 V to 6 V)
f_{SW}	2.1MHz
η (estimated efficiency)	90%

2 Calculations and Component Selection

The calculation specific to the LM5157x and LM5158x is given to implement a boost converter that operates in the continuous conduction mode based on the design parameters in Table 1-1.

2.1 Switching Frequency

With the given design parameters, selecting the proper switching frequency is the first step in the design process. In general, a higher switching frequency yields a smaller solution size at the cost of a higher switching loss and lower efficiency. Therefore, the final selection of the switching frequency is a trade-off between the power density and efficiency based on the specific requirement of the application. Harmonics of the switching frequency should be considered in designs that have strict EMC requirements. Equation 1 is used to set the frequency of the oscillator in the LM5157x and LM5158x. The example application is selected to have a switching frequency of 2.1MHz.

$$R_T = \frac{2.21 \times 10^{10}}{f_{sw}} - 955 = \frac{2.21 \times 10^{10}}{2.1\text{MHz}} - 955 = 9.57\text{k}\Omega \quad (1)$$

A standard value of 9.53kΩ with 1% tolerance is chosen for R_T.

The internal oscillator of the LM5157x and LM5158x can be synchronized to an external clock as described in the data sheet. The LM5157x and LM5158x has a maximum duty cycle limit that is frequency dependent, which is also characterized in the data sheet.

2.2 Inductor Calculation

The inductance value of the boost converter can be calculated with the inductor current ripple ratio (RR, defined as the peak to peak ripple current over the average inductor current). There are three main considerations dominating the selection of the inductance value: the power loss, the falling slope of the inductor current and the right-half plane (RHP) zero frequency (ω_{Z_RHP}) of the control loop.

- As the inductance value increases, the inductor core loss and the RMS current becomes smaller but also note that the DCR of the inductor could be higher.
- The inductance value should be large enough so that the falling slope of the inductor current is small enough to prevent the sub-harmonic oscillation in the peak current mode control of the LM5157x/LM5158x.
- In a boost converter, the RHP zero usually sets the bandwidth limit of the design. Therefore, the RHP zero frequency should be high enough to allow a higher crossover frequency of the control loop. As the relative inductance value decreases the RHP zero frequency increases.

A maximum ripple ratio between 30% and 70% results in a good balance between the considerations above. In this example, the maximum ripple ratio of the inductor current is set to 60%. In the continuous conduction mode (CCM) operation, the maximum ripple ratio occurs at a duty cycle of 33% ($D_{maxΔIL}$=0.33) and Equation 2 is used to calculate the supply voltage at 33% duty cycle.

$$V_{SUPPLY\_maxΔIL} = V_{LOAD} \cdot (1 - D_{maxΔIL}) = 12 \cdot (1 - 0.33) = 8V \quad (2)$$

where

- $D_{maxΔIL}$ is the duty cycle where the maximum inductor ripple current occurs

Knowing $V_{SUPPLY\_maxΔIL}$, the desired ripple ratio, and the switching frequency, Equation 3 is used to calculate the inductance value at 1.6A load (V_{SUPPLY} = 6V to 9V).

$$L_{M\_calc\_1} = \frac{V_{SUPPLY}}{I_{SUPPLY} \cdot RR \cdot f_{sw}} \cdot D = \frac{8V}{2.4A \cdot 0.6 \cdot 2.1MHz} \cdot 0.33 = 0.88\mu H \quad (3)$$

where

- D is the duty cycle where the maximum inductor ripple current occurs
- RR is the inductor current ripple ratio

In the 0.8A load case (V_{SUPPLY} = 3V to 6V) where it does not result in a duty cycle of 33% the maximum supply voltage (6V, duty cycle = 0.5) is used to calculate the maximum ripple ratio. Equation 4 is used to calculate the inductor value.

$$L_{M\_calc\_2} = \frac{6V}{1.6A \cdot 0.6 \cdot 2.1MHz} \cdot 0.5 = 1.49\mu H \quad (4)$$

A standard inductance of 1.5µH is selected for the value of L_M to cover the requirement of both regions. The maximum peak inductor current occurs when the supply voltage is at the minimum value, V_{SUPPLY_min}, and the maximum load current I_{LOAD_max}. The peak inductor current is calculated using Equation 5 and Equation 6. Again, two regions are calculated separately and the maximum is the larger one.

$$IL_{peak\_MAX\_1} = \frac{V_{LOAD} \cdot I_{OUT}}{V_{SUPPLY} \cdot \eta} + \frac{1}{2} \cdot \frac{V_{SUPPLY} \cdot D}{L_M \cdot f_{sw}} = \frac{12V \cdot 1.6A}{6V \cdot 0.9} + \frac{1}{2} \cdot \frac{6V \cdot 0.5}{1.5\mu H \cdot 2.1MHz} = 4.03A \quad (5)$$

$$IL_{peak\_MAX\_2} = \frac{12V \cdot 0.8A}{3V \cdot 0.9} + \frac{1}{2} \cdot \frac{3V \cdot 0.75}{1.5\mu H \cdot 2.1MHz} = 3.91A \quad (6)$$

where

- η is the estimated efficiency

The peak inductor current is used to properly select the device among LM5158, LM51581, LM5157, and LM51571. Please refer to the data sheets for their current limits. Due to component tolerances and power loss of the regulator, the peak current limit should be selected with some margin above the calculated peak inductor current. In this example, a margin of 15% is used and the LM5157 device is selected.

2.3 Slope Compensation Check

According to the theory of the peak current mode control, the slope of the compensation ramp must be greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle. Therefore, the following inequality in Equation 7 will be satisfied.

$$0.5 \times \frac{(V_{LOAD} + V_F) - V_{SUPPLY}}{L_M} \times A_{CS} \times Margin < 500mV \times f_{sw} \quad (7)$$

where

- A_{CS} is the equivalent current sensing gain.
- 500mV is the slope compensation peak voltage.
- V_F is the forward voltage of the diode.

Typically 82% of the sensed inductor current falling slope is an optimal value of the slope compensation, which reflects to a margin of 1.6. If the inequality is failed, the inductance value of L_M must be increased so that the falling slope can be smaller. If the L_M inductance value is changed the peak current must be re-calculated and the device selection must be re-examined. In this example, the inequality is verified in Equation 8, Equation 9, and Equation 10.

$$0.5 \times \frac{(V_{\mathrm{LOAD}} + V_F) - V_{\mathrm{SUPPLY}}}{L_M} \times A_{\mathrm{CS}} \times \mathrm{Margin} = 0.5 \times \frac{(12V + 0.5V) - 3V}{1.5\mu\mathrm{H}} \times 0.095 \times 1.6 = 0.481 \times 10^6 \quad (8)$$

$$500\mathrm{mV} \times f_{\mathrm{sw}} = 500\mathrm{mV} \times 2.1\mathrm{MHz} = 1.05 \times 10^6 \quad (9)$$

$$0.481 \times 10^6 < 1.05 \times 10^6 \quad (10)$$

2.4 Inductor Selection

The inductor are selected according to three parameters: calculated inductance value (L_M), RMS inductor current and the maximum peak inductor current.

- The inductance is selected to be the standard 1.5µH, which is a common value that is commercially available.
- The saturation current of the inductor should be larger than the maximum current limit of the converter device selected. If the inductor becomes saturated, the components can be damaged and the converter cannot operate correctly .
- With the ripple ignored, the inductor RMS current can be approximated by the average inductor current, which is estimated to be 3.6 A. The inductor RMS current rating should be higher than the estimated RMS current and keep the inductor temperature within a reasonable level based on the application.

For this design example, the inductor is selected to have an inductance value of 1.5µH, a saturation current limit of 15 A, and a 20°C temperature rise at 10A RMS.

2.5 Diode Selection

The power diode must be rated for the average load current and the output voltage with some margin. It should also be able to handle the loss dissipation under the full load. The schottky diode is recommended due to the small reverse recovery time and charge. For this design a 45 V reverse voltage, 10 A average forward current schottky diode is selected. The conduction loss is calculated in Equation 11.

$$P_{D\_\mathrm{con}} = V_F \cdot (1 - D) \cdot I_{\mathrm{SUPPLY}} = 490\mathrm{mV} \cdot (1 - 0.5) \cdot \frac{12V \cdot 1.6A}{6V} = 0.78W \quad (11)$$

where

- V_F is the forward voltage drop of the diode

2.6 Output Capacitor Selection

The output capacitor determines the output voltage ripple and load transient performance. In this example, the output capacitor is appropriately sized based on the required output voltage ripple. With the required V_{LOAD} ripple of 100mV, Equation 12 is used to calculate the minimum output capacitance.

$$C_{\mathrm{OUT\_min}} = \frac{I_{\mathrm{LOAD}} \cdot D}{f_{\mathrm{sw}} \cdot \Delta V_{\mathrm{LOAD}}} = \frac{1.6A \cdot 0.5}{2.1\mathrm{MHz} \cdot 100\mathrm{mV}} = 3.8\mu\mathrm{F} \quad (12)$$

The output capacitor must be rated to handle the AC current. The maximum output ripple current is estimated using Equation 13.

$$I_{\mathrm{RMS\_COUT}} = \sqrt{(1 - D) \cdot \left[I_{\mathrm{LOAD}}{}^2 \cdot \frac{D}{(1 - D)^2} + \frac{\Delta i_L{}^2}{3} \right]} = \sqrt{(1 - 0.5) \cdot \left[1.6A^2 \cdot \frac{0.5}{(1 - 0.5)^2} + \frac{0.48A^2}{3} \right]} = 1.6A \quad (13)$$

Note that similar as in the inductor calculation, the above condition is selected to be the *worst-case scenario* with the highest capacitance requirement and highest RMS current between the full load case and the derated half load case. For this design, a total output capacitance of 28µF is selected, which becomes around 22µF

considering the capacitance drop under 12 V DC bias. The capacitor bank ESR (R_{ESR}) is estimated to be around 0.22mΩ.

2.7 Input Capacitor Selection

The input capacitor determines the supply ripple voltage. For this design an input capacitance of 60µF is selected using low ESR ceramic capacitors. Equation 14 is used to calculate the maximum supply voltage ripple.

$$\Delta V_{SUPPLY} = \frac{V_{LOAD}}{32 \cdot L_M \cdot C_{IN} \cdot f_{sw}^2} = \frac{12V}{32 \cdot 1.5\mu H \cdot 60\mu F \cdot 2.1MHz^2} = 1mV \quad (14)$$

2.8 UVLO Resistor Selection

The external under voltage lockout (UVLO) resistors set the minimum operating voltage of the regulator. Two levels must be specified: the desired start-up voltage of the converter ($V_{SUPPLY(ON)}$) and the desired turn-off voltage of the converter ($V_{SUPPLY(OFF)}$). In this example, $V_{SUPPLY(ON)}$ voltage is 2.8 V and the $V_{SUPPLY(OFF)}$ is 2.4 V. Using Equation 15, the top UVLO resistor (R_{UVLOT}) is calculated.

$$R_{UVLOT} = \frac{0.967 \cdot V_{SUPPLY(ON)} - V_{SUPPLY(OFF)}}{5\mu A} = \frac{0.967 \cdot 2.8V - 2.4V}{5\mu A} = 61.5k\Omega \quad (15)$$

A standard value of 61.9kΩ is selected for R_{UVLOT}. Using Equation 16, the bottom UVLO resistor (R_{UVLOB}) is calculated.

$$R_{UVLOB} = \frac{1.5V \cdot R_{UVLOT}}{V_{SUPPLY(ON)} - 1.5V} = \frac{1.5V \cdot 61.9k\Omega}{2.8V - 1.5V} = 71.4k\Omega \quad (16)$$

A standard value of 71.5kΩ is selected for R_{UVLOB}

2.9 Soft-Start Capacitor Selection

The soft-start capacitor is used to control the overshoot of the load voltage and inrush current during the start-up of the regulator. Equation 17 is used to calculate the minimum recommended soft-start capacitor value.

$$C_{SS} > \frac{10\mu A \cdot V_{LOAD} \cdot C_{OUT}}{I_{LOAD}} = \frac{10\mu A \cdot 12V \cdot 22\mu F}{0.8A} = 3.3nF \quad (17)$$

For this design a C_{SS} value of 22nF is selected to minimize any overshoot on the load voltage during the start-up.

2.10 Feedback Resistor Selection

The feedback resistors (R_{FBT}, R_{FBB}) determines the regulated output voltage. To help limit the bias current of the feedback resistor divider, R_{FBT} is selected to be 49.9kΩ. Equation 18 is used to calculate the value of R_{FBB}.

$$R_{FBB} = \frac{R_{FBT}}{\frac{V_{LOAD}}{V_{REF}} - 1} = \frac{49.9k\Omega}{\frac{12V}{1V} - 1} = 4.54k\Omega \quad (18)$$

R_{FBB} is selected to be 4.53kΩ

2.11 Control Loop Compensation

One benefit of the peak current mode control is the easier compensation design compared with that of the voltage mode control. A simple two-pole (one at origin), single zero network is adequate. A type II compensation network is implemented as shown in Figure 2-1, which provides a programmable zero and a pole. The following section introduces a general technique to set the crossover frequency and place the pole and zero of the error amplifier to achieve a stable system in the CCM boost. The detailed models of the control loop are presented in Section 4.

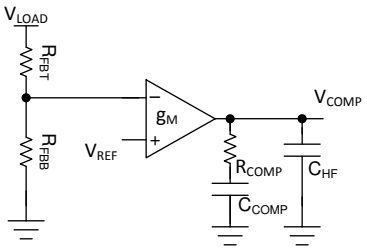

Figure 2-1. Type II Compensation Network

2.11.1 Crossover Frequency (f_{cross}) Selection

The crossover frequency of the loop can be either selected to be 1/10 the switching frequency or 1/5 the right-half plane zero frequency, whichever is lower. Equation 19 shows the calculation for 1/10 the switching frequency. Equation 20 and Equation 21 show how to calculate the 1/5 the right half plane zero frequency at full load and half load conditions.

$$f_{\text{cross}} = \frac{f_{\text{sw}}}{10} = \frac{2.1\text{MHz}}{10} = 210\text{kHz} \tag{19}$$

$$f_{CROSS\_1} = \frac{f_{Z\_RHP}}{5} = \frac{R_{LOAD} \cdot D'^2}{5 \cdot 2 \cdot \pi \cdot L_M} = \frac{7.5\Omega \cdot 0.5^2}{5 \cdot 2 \cdot \pi \cdot 1.5\mu H} = 39.8kHz \tag{20}$$

$$f_{CROSS\_2} = \frac{15\Omega \cdot 0.25^2}{5 \cdot 2 \cdot \pi \cdot 1.5\mu H} = 19.9kHz \tag{21}$$

where

- D' is (1 -D) a the minimum supply voltage
- R_{LOAD} is the load resistance equal to V_{LOAD} / I_{LOAD}

To give some margin, the crossover frequency is selected to be 16.6kHz, a little less than 1/5 the right half plane zero frequency at half load condition. In this design example, the performance under the full load condition is more important and needs to be optimized. Therefore, the full load condition with the input voltage from 6 V to 9 V is used for the following calculations. After the design and selection of the compensation loop, the stability of the half load condition can be checked with the equations in Section 4.

2.11.2 R_{COMP} Selection

The R_{COMP} value directly affects the crossover frequency of the control loop. The higher the crossover frequency, the faster the control loop reacts to transient conditions. Knowing the desired loop crossover frequency, 16.6kHz, R_{COMP} is calculated using Equation 22.

$$R_{COMP} = \frac{2\pi \cdot C_{OUT} \cdot A_{CS} \cdot V_{LOAD}^2 \cdot f_{CROSS}}{g_m \cdot V_{SUPPLY\_min}} = \frac{2\pi \cdot 22\mu F \cdot 0.095 \cdot 12V^2 \cdot 16.6kHz}{2mA/V \cdot 6V} = 2.62k\Omega \tag{22}$$

where

- g_m is the transconductance of the error amplifier, 2mA/V
- A_{CS} is the equivalent current sensing gain, 0.095

R_{COMP} is selected to be 2.63kΩ.

2.11.3 C_{COMP} Selection

The R_{COMP} resistor and C_{COMP} capacitor set the low frequency zero of the compensation network. For a desired settling time constant, the low frequency zero are placed as a phase boost. A good strategy used here is placing the zero directly at the geometric mean of the crossover frequency (f_{CROSS}) and the low frequency pole of the plant (ω_{P_LF}). Equation 23 produces the value of C_{COMP}.

$$C_{COMP} = \sqrt{\frac{C_{OUT} \cdot R_{LOAD}}{4\pi \cdot {R_{COMP}}^2 \cdot f_{CROSS}}} = \sqrt{\frac{22\mu F \cdot 7.5\Omega}{4\pi \cdot 2.63k\Omega^2 \cdot 16.6kHz}} = 10.7nF \quad (23)$$

C_{COMP} is chosen to be 10nF.

2.11.4 C_{HF} Selection

The C_{HF} capacitor sets the high frequency pole of the compensation network. The high frequency pole aids in attenuating high frequency noise due to the switching frequency and assuring enough gain margin. It is recommended to set the pole frequency at the RHP zero(ω_{Z_RHP}), which is usually smaller than the ESR zero, or between the RHP zero and half the switching frequency. In this design example, the high frequency pole is placed at the RHP zero. Equation 24 is used to calculate the value of C_{HF}.

$$C_{HF} = \frac{C_{COMP} \cdot L_M}{C_{COMP} \cdot {D'}^2 \cdot R_{LOAD} \cdot R_{COMP} - L_M} = \frac{10nF \cdot 1.5\mu H}{10nF \cdot 0.75^2 \cdot 7.5\Omega \cdot 2.62k\Omega - 1.5\mu H} = 138pF \quad (24)$$

C_{HF} is chosen to be 100pF.

2.12 Power Loss and Efficiency Estimation

The total loss of the boost converter (P_{TOTAL}) can be expressed as the sum of the losses in the device (P_{IC}, excludes the power MOSFET loss), MOSFET power losses (P_Q), diode power losses (P_D), inductor power losses (P_L), and the loss in the sense resistor (P_{RS}, see explanation below). The sum of (P_{IC}) and (P_Q) is the power dissipation in the converter device and should be designed within the reasonable range to prevent excessive temperature rise of the IC.

$$P_{TOTAL} = P_{IC} + P_Q + P_D + P_L + P_{RS}[W] \quad (25)$$

P_{IC} can be separated into gate driving loss (P_G) and the losses caused by quiescent current (P_{IQ}).

$$P_{IC} = P_G + P_{IQ}[W] \quad (26)$$

Each power loss is approximately calculated as follows:

$$P_G = Q_{G(@VCC)} \times V_{BIAS} \times F_{SW}[W] \quad (27)$$

$$P_{IQ} = V_{BIAS} \times I_{BIAS}[W] \quad (28)$$

I_{BIAS} values in each mode can be found in the LM5157x and LM5158x data sheet.

P_Q can be separated into switching loss ($P_{Q(SW)}$) and conduction loss ($P_{Q(COND)}$).

$$P_Q = P_{Q(SW)} + P_{Q(COND)}[W] \quad (29)$$

Each power loss is approximately calculated as follows:

$$P_{Q(SW)} = 0.5 \times (V_{LOAD} + V_F) \times I_{SUPPLY} \times (t_R + t_F) \times F_{SW} \quad (30)$$

t_R and t_F are the rise and fall times of the integrated power MOSFET. I_{SUPPLY} is the input supply current of the boost converter.

$$P_{Q(COND)} = D \times {I_{SUPPLY}}^2 \times R_{DS(ON)}[W] \quad (31)$$

$R_{DS(ON)}$ is the on-resistance of the MOSFET given in the LM5157x and LM5158x data sheet. Consider the $R_{DS(ON)}$ increase due to self-heating.

P_D can be separated into diode conduction loss (P_{VF}) and reverse recovery loss (P_{RR}).

$$P_D = P_{VF} + P_{RR}[W] \quad (32)$$

Each power loss is approximately calculated as follows:

$$P_{VF} = (1-D) \times V_F \times I_{SUPPLY}[W] \quad (33)$$

$$P_{RR} = V_{LOAD} \times Q_{RR} \times F_{SW}[W] \quad (34)$$

Q_{RR} is the reverse recovery charge of the diode and is specified in the diode data sheet. Reverse recovery characteristics of the diode strongly affect efficiency, especially when the load voltage is high.

P_L is the sum of DCR loss (P_{DCR}) and AC core loss (P_{AC}). DCR is the DC resistance of inductor which is mentioned in the inductor data sheet.

$$P_L = P_{DCR} + P_{AC}[W] \quad (35)$$

Each power loss is approximately calculated as follows:

$$P_{DCR} = I_{SUPPLY}^2 \times R_{DCR}[W] \quad (36)$$

$$P_{AC} = K \times \Delta I^{\beta} F_{SW}^{\alpha}[W] \quad (37)$$

$$\Delta I = \frac{V_{SUPPLY} \times D \times \frac{1}{F_{SYNC}}}{L_M} \quad (38)$$

ΔI is the peak-to-peak inductor current ripple. K, α, and β are core dependent factors which can be provided by the inductor manufacturer.

Due to the current sensing technique implemented in LM5157x and LM5158x, the sensing resistance and the power loss P_{RS} is negligible.

Efficiency of the power converter can be estimated as follows:

$$\text{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{P_{TOTAL} + V_{LOAD} \times I_{LOAD}} \times 100[\%] \quad (39)$$

3 Implementation Results

Please see the *LM5157EVM-BST User's Guide* for more testing results.

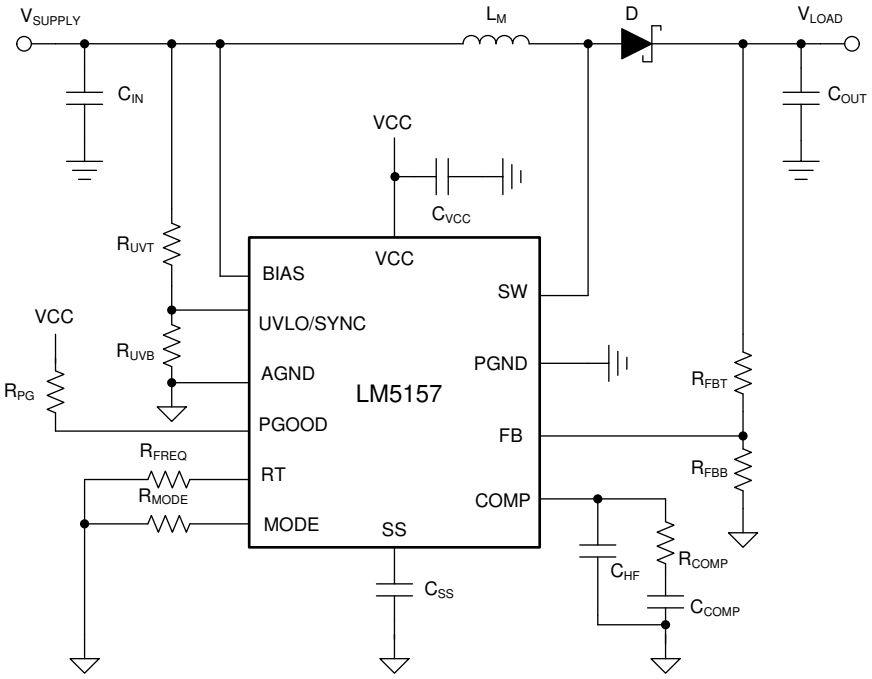

Figure 3-1. Application Circuit

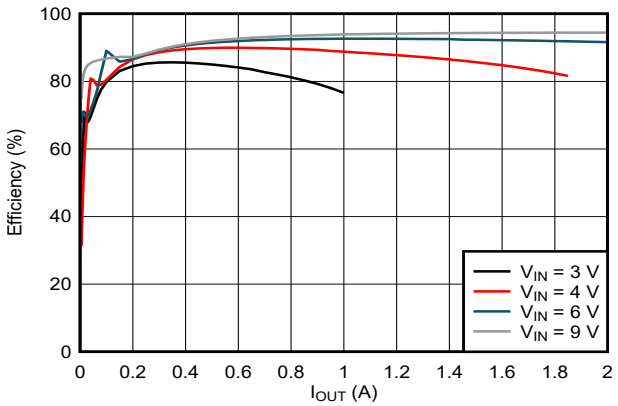

Figure 3-2. Efficiency vs. I_{OUT}

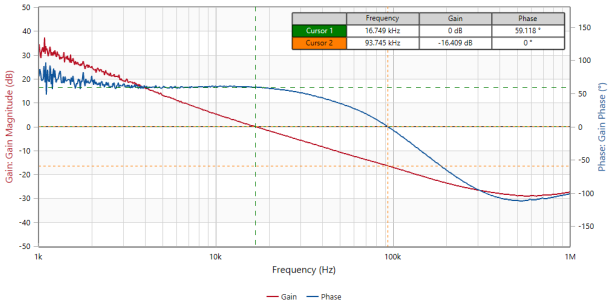

Figure 3-3. Control Loop Response V_{SUPPLY} = 6V I_{LOAD} = 1.6A

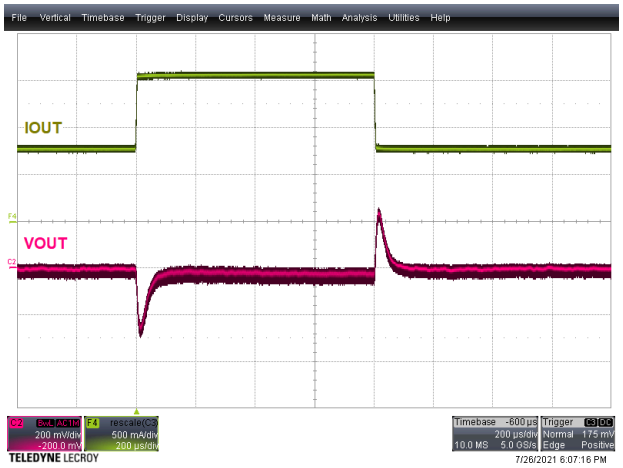

Figure 3-4. Load Step: I_{LOAD} 0.8A to 1.6A, V_{SUPPLY} =6V

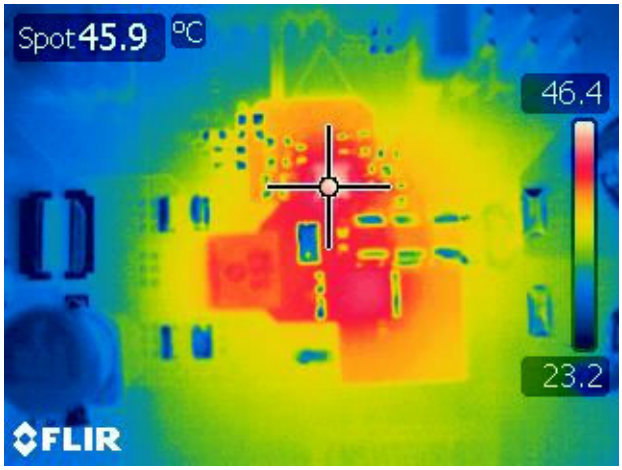

Figure 3-5. Thermal Image: V_{SUPPLY} = 6V, I_{LOAD} =1.6A

LM5157EVM-BST
1.6A/0.8A

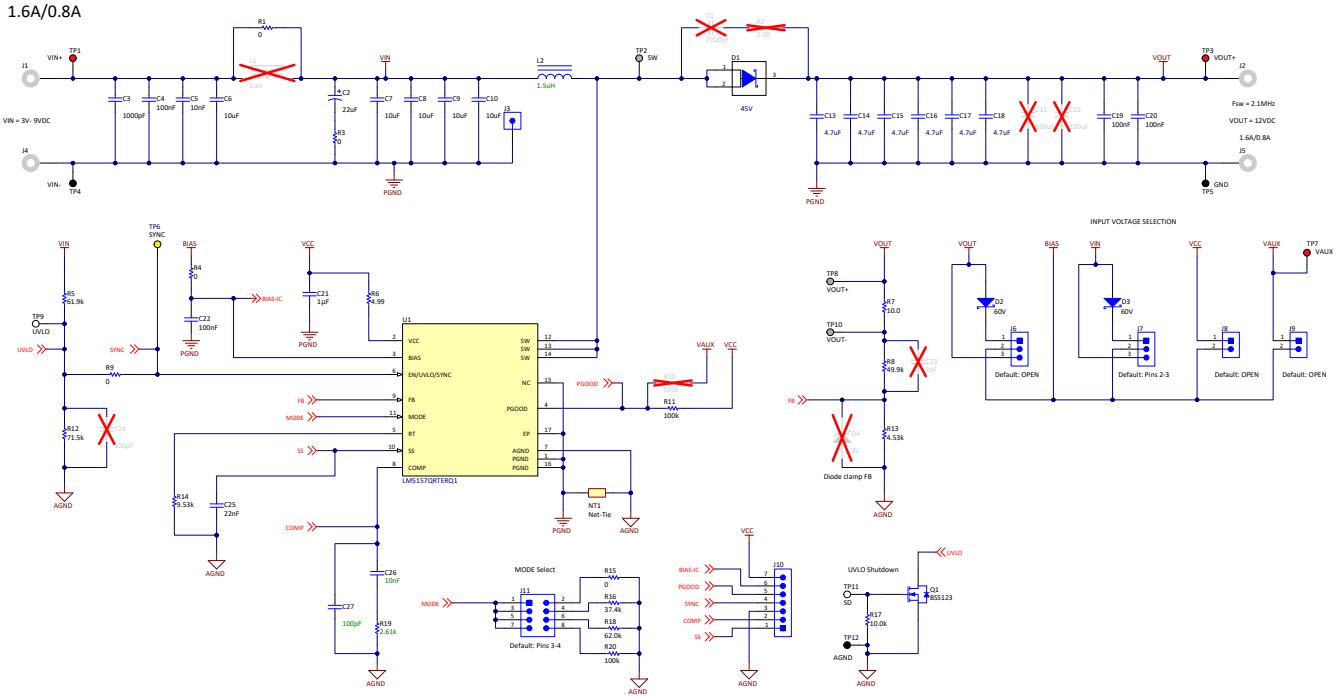

Figure 3-6. LM5157EVM-BST Schematic

Table 3-1. List of Materials

REFERENCE DESIGNATOR	QTY.	SPECIFICATION	MANUFACTURER	PART NUMBER
R_T	1	RES, 9.53 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06039K53FKEA
R_{FBT}	1	RES, 49.9 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0749K9L
R_{FBB}	1	RES, 4.53 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06034K53FKEA
L_M	1	Inductor, Shielded, Composite, 1.5 µH, 14 A, 0.01052 Ω, AEC-Q200 Grade 1, SMD	Coilcraft	XEL6030-152MEB
C_{OUT1}	6	CAP, CERM, 4.7 µF, 50 V, ±10%, X7R, 1210	TDK	C3225X7R1H475K250AB
C_{OUT2} (Bulk)	2	CAP, Aluminum Polymer, 100 µF, 50 V, ±20%, 0.025 Ω, AEC-Q200 Grade 2, D10xL10mm SMD	Chemi-Con	HHXB500ARA101MJA0G
C_{IN1}	4	CAP, CERM, 10 µF, 50 V, ±10%, X7R, 1210	MuRata	GRM32ER71H106KA12L
C_{IN2} (Bulk)	1	CAP, AL, 22 uF, 100 V, ±20%, 1.3 Ω, AEC-Q200 Grade 2, SMD	Panasonic	EEE-FK2A220P
D1	1	Diode, Schottky, 45 V, 10 A, AEC-Q101, CFP15	Nexperia	PMEG045V100EPDAZ
R_{COMP}	1	RES, 2.61 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-072K61L
C_{COMP}	1	CAP, CERM, 0.01 µF, 50 V, ±10%, X7R, 0603	Kemet	C0603X103K5RACTU
C_{HF}	1	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, AEC-Q200 Grade 0, 0603	TDK	CGA3E2NP01H101J080AA
R_{UVLOT}	1	RES, 61.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060361K9FKEA
R_{UVLOB}	1	RES, 71.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060371K5FKEA
R_{UVLOS}	1	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL
C_{SS}	1	CAP, CERM, 0.022 µF, 50 V, ±10%, X7R, 0603	Kemet	C0603X223K5RACTU
R_{BIAS}	1	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL
C_{BIAS}	1	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCJ188R72A104KA01D
C_{VCC}	1	CAP, CERM, 1 µF, 16 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E1X7R1C105K080AC
R_{VCC}	1	RES, 5.1, 5%, 0.1 W, 0603	Yageo America	RC0603JR-075R1L
R_{PG}	1	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100KFKEA
R_{MODE}	1	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL

4 Small Signal Frequency Analysis

This section provides all the equations for the control loop small signal model when the LM5157x/LM5158x is configured as a boost regulator in CCM operation. The simplified formulas allow for a quick evaluation of the control loop, but loose accuracy at high frequencies. The comprehensive formulas are more complex but provide better accuracy at high frequencies.

4.1 Boost Regulator Modulator Modeling

Table 4-1 includes equations model the plant (control-to-output) of a peak current mode boost regulator in continuous conduction mode.

Table 4-1. Power Plant Equations

	Simplified Formula	Comprehensive Formula
Modulator Equations		
Modulator Transfer Function	$\frac{\hat{v}_{LOAD}(s)}{\hat{v}_{COMP}(s)} = A_M \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)}$ (40)	$\frac{\hat{v}_{LOAD}(s)}{\hat{v}_{COMP}(s)} = A_M \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)\left(1+\frac{s}{Q\cdot\omega_n}+\frac{s^2}{\omega_n^2}\right)}$ (41)
Modulator DC Gain	$A_M = \frac{R_{LOAD}}{A_{CS}} \times \frac{D'}{2}$ (42)	
RHP Zero	$\omega_{Z\_RHP} = \frac{R_{LOAD}\left(D'\right)^2}{L_M}$ (43)	
ESR Zero	$\omega_{Z\_ESR} = \frac{1}{C_{OUT}\cdot R_{ESR}}$ (44)	
Low Frequency Pole	$\omega_{P\_LF} = \frac{2}{C_{OUT}\cdot R_{LOAD}}$ (45)	
Sub-Harmonic Double Pole	Not Considered	$\omega_n = \pi \cdot f_{sw}$ (46)
Quality Factor	Not Considered	$Q = \frac{1}{\pi\left[D'\cdot\left(1+\frac{s_e}{s_n}\right)-\frac{1}{2}\right]}$ (47)
Slope Compensation	Not Considered	$S_e = V_{SLOPE} \times f_{SW}$ (48)
Sensed Rising Inductor Slope	Not Considered	$S_n = \frac{V_{SUPPLY} \times A_{CS}}{L_M}$ (49)

4.2 Compensation Modeling

Table 4-2 includes equations model a type II compensation network implemented using a transconductance error amplifier.

Table 4-2. Compensation Modeling Equations

	Simplified Formula	Comprehensive Formula
Feedback Equations		
Feedback Transfer Function	$\frac{\hat{v}_{COMP}(s)}{\hat{v}_{LOAD}(s)} = -A_{FB}\frac{\left(1+\frac{s}{\omega_{Z\_EA}}\right)}{s\cdot\left(1+\frac{s}{\omega_{P\_EA}}\right)}$ (50)	
Feedback DC Gain	$A_{FB} = \frac{R_{FBB}\cdot g_m}{(R_{FBB}+R_{FBT})\cdot C_{COMP}}$ (51)	$A_{FB} = \frac{R_{FBB}\cdot g_m}{(R_{FBB}+R_{FBT})\cdot (C_{COMP}+C_{HF})}$ (52)
Low Frequency Zero	$\omega_{Z\_EA} = \frac{1}{R_{COMP}\cdot C_{COMP}}$ (53)	$\omega_{Z\_EA} = \frac{1}{R_{COMP}\cdot C_{COMP}}$ (54)
High Frequency Pole	$\omega_{P\_EA} = \frac{1}{R_{COMP}\cdot C_{HF}}$ (55)	$\omega_{P\_EA} = \frac{C_{COMP}+C_{HF}}{R_{COMP}\cdot C_{COMP}\cdot C_{HF}}$ (56)
Mid-band Gain	$G_{MID} = \frac{R_{COMP}\cdot R_{RFBB}\cdot g_m}{(R_{FBB}+R_{FBT})}$ (57)	$G_{MID} = \frac{C_{COMP}\cdot R_{COMP}\cdot R_{RFBB}\cdot g_m}{(C_{HF}+C_{COMP})\cdot (R_{FBB}+R_{FBT})}$ (58)

1. g_m is the transconductance of the error amplifier, 2mA/V

4.3 Open Loop Modeling

These equations model the open loop transfer function of the control loop.

Table 4-3. Open Loop Modeling Equations

	Simplified Formula	Comprehensive Formula
Open Loop Equations		
Open Loop Transfer Function	$T(s) = A_M\cdot A_{FB}\cdot\frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)}\cdot\frac{\left(1+\frac{s}{\omega_{Z\_EA}}\right)}{s\cdot\left(1+\frac{s}{\omega_{P\_EA}}\right)}$ (59)	$T(s) = A_M\cdot A_{FB}\cdot\frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)\left(1+\frac{s}{Q\cdot\omega_n}+\frac{s^2}{\omega_n{}^2}\right)}\cdot\frac{\left(1+\frac{s}{\omega_{Z\_EA}}\right)}{s\cdot\left(1+\frac{s}{\omega_{P\_EA}}\right)}$ (60)
Crossover Frequency	$f_{cross} = \frac{g_m\times V_{SUPPLY}\times R_{COMP}}{2\pi\times C_{OUT}\times A_{CS}\times V_{LOAD}{}^2}$ (61)	Use Bode Plot

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