Functional Safety Information

LM636xx-Q1
Functional Safety FIT Rate, FMD, and Pin FMA

Table of Contents

1 Overview

This document contains information for the LM636xx-Q1 (HTSSOP and WSON packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

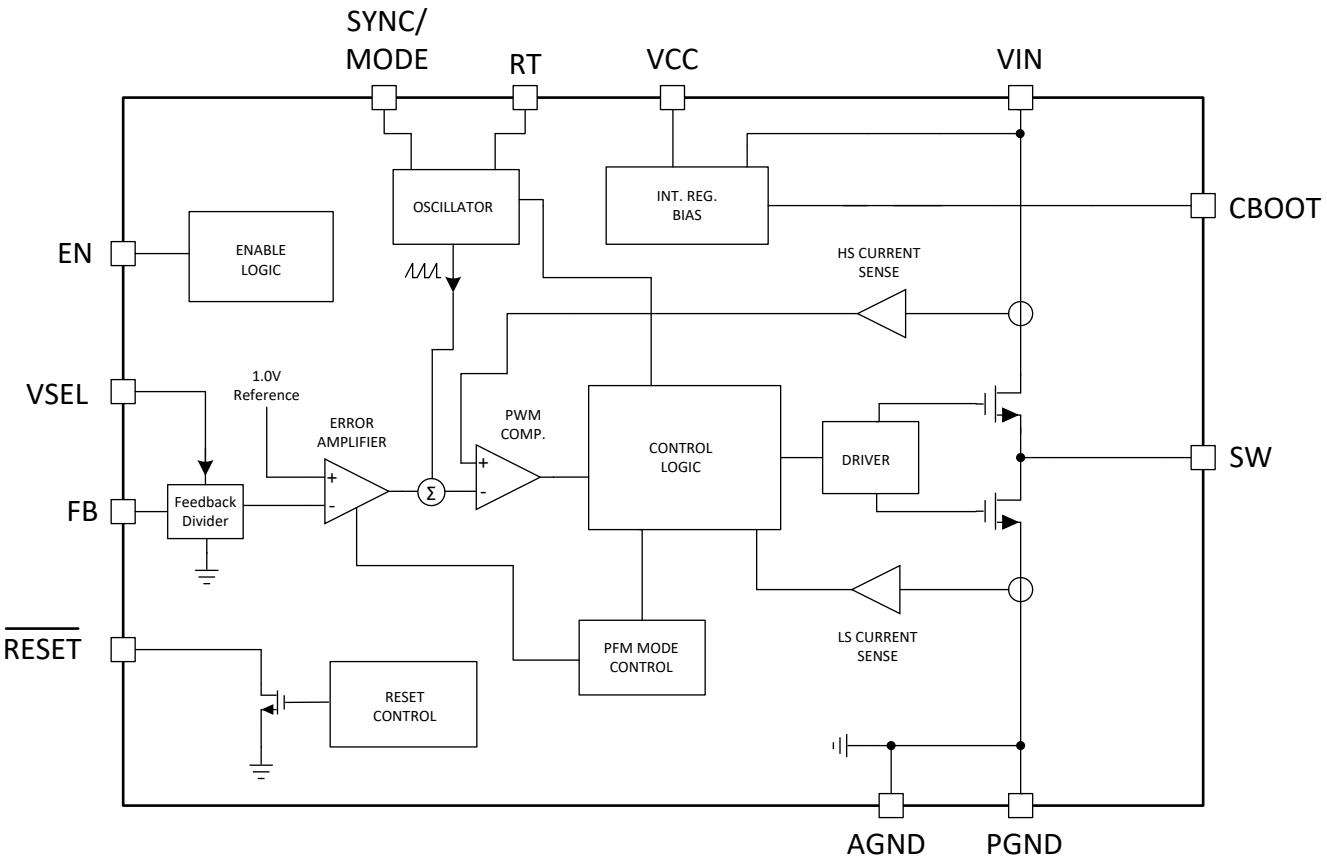

Figure 1-1. Functional Block Diagram

The LM636xx-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 HTSSOP Package

This section provides Functional Safety Failure In Time (FIT) rates for the HTSSOP package of the LM636xx-Q1 based on the following industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	17
Die FIT Rate	7
Package FIT Rate	10

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 600 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 WSON Package

This section provides Functional Safety Failure In Time (FIT) rates for the WSON package of the LM636xx-Q1 based on the following industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	12
Die FIT Rate	7
Package FIT Rate	5

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 600 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM636xx-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	35%
Output not in specification -- voltage or timing	45%
SW driver FET stuck on	10%
$\overline{\text{RESET}}$ false trip or fails to trip	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM636xx-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to VIN (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* found in the LM63625 data sheet.
- Configuration as shown in the *Example Application Circuit* found in the LM63625 data sheet.

4.1 HTSSOP-16 Package

Figure 4-1 shows the LM636xx-Q1 pin diagram for the HTSSOP-16 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM63625 data sheet.

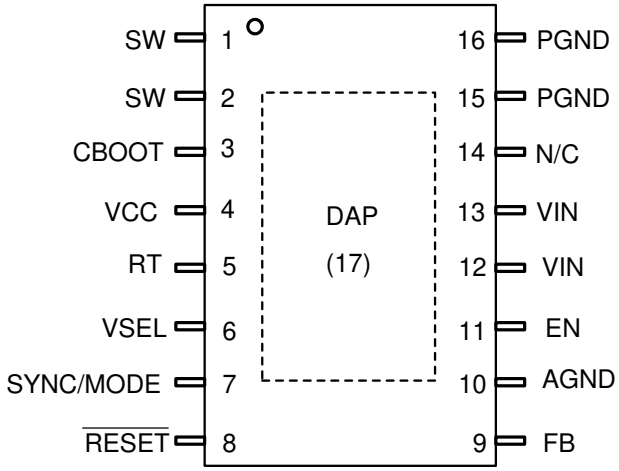

Figure 4-1. Pin Diagram for HTSSOP

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1, 2	Damage to internal power FET or FETs, other internal circuits, or both	A
BOOT	3	Damage to internal circuits	A
VCC	4	Fault mode shuts the device off.	B
RT	5	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, no effect is produced. If an RT resistor is used, the frequency is set to 2.1MHz. If a 0Ω jumper is used to connect the RT input to VCC, then the VCC output is pulled to ground; see *short to ground on pin 4*.	B
VSEL	6	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, VCC is shorted to ground; see *short to ground on pin 4*. If a VSEL resistor is used or if the VSEL input is pulled to ground with a 0Ω jumper, then the output voltage is set to 3.3V before power up. No effect after power up.	B
SYNC/MODE	7	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, no effect is produced. If a 0Ω jumper is used to connect the SYNC/MODE input to VCC, then the VCC output is pulled to ground; see *short to ground on pin 4*	B
$\overline{\text{RESET}}$	8	$\overline{\text{RESET}}$ functionality is lost.	B
FB	9	The regulator operates at maximum duty cycle. Output voltage rises to nearly the input voltage (V_{IN}) level. Possible damage to customer load, output stage components, or both, can occur. No effect on device	B
AGND	10	No effect	D
EN	11	Loss of ENABLE functionality. The device remains in shutdown mode.	B
VIN	12, 13	The device does not operate. No output voltage is generated. Output capacitors discharge through input short. Large reverse current can damage the device.	A
N/C	14	No effect	D
PGND	15, 16	No effect	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1, 2	With both pins open – loss of output voltage. With one pin open – some loss of device performance	B
BOOT	3	Loss of output voltage regulation; low or no output voltage. Possible damage to the device	A
VCC	4	VCC LDO is unstable. Loss of output voltage regulation and possible damage to internal circuits.	A
RT	5	Device switching frequency drops to zero or become erratic. Loss of output voltage	B
VSEL	6	The device enters ADJ mode when EN or VIN is cycled. Incorrect output voltage if fixed VOUT mode is intended. No effect after power up	C
SYNC/MODE	7	Internal pulldown places the device in auto mode.	B
$\overline{\text{RESET}}$	8	$\overline{\text{RESET}}$ functionality is lost.	B
FB	9	Loss of output voltage regulation. Output voltage can rise or fall outside of the intended regulation window.	B
AGND	10	Loss of output voltage regulation. Possible damage to internal circuits	A
EN	11	Loss of ENABLE functionality. Erratic operation; probable loss of regulation	B
VIN	12, 13	With both pins open – loss of output voltage. With one pin open – possible device damage	A
N/C	14	No effect	D
PGND	15, 16	With either one or both pins open, there is possible device damage	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	SW	No effect	D
SW	2	BOOT	Loss of output regulation, possible damage to internal circuits	A
BOOT	3	VCC	Loss of output regulation, possible damage to internal circuits	A
VCC	4	RT	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, VCC is shorted to ground; see *short to ground on pin 4*. For all other configurations, the effect is either no change or erratic switching frequency with possible damage to device internal circuits.	A
RT	5	VSEL	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, VCC is shorted to ground; see *short to ground on pin 4*. For all other configurations, the effect is either no change or erratic output voltage, switching frequency, or both with possible damage to device internal circuits.	A
VSEL	6	SYNC/MODE	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, VCC is shorted to ground; see *short to ground on pin 4*. For all other configurations, the effect is either no change or erratic operation, switching frequency, or both with possible damage to device internal circuits.	A
SYNC/MODE	7	$\overline{\text{RESET}}$	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, $\overline{\text{RESET}}$ is shorted to ground; see *short to ground on pin 8*. For all other configurations, the effect is either no change or erratic operation, loss of $\overline{\text{RESET}}$, SYNC/MODE functionality, or all of the above, with possible damage to device internal circuits.	A
FB	9	AGND	See *short to ground on pin 9*	B
AGND	10	EN	See *short to ground on pin 11*	B
EN	11	VIN	See *short to VIN on pin 11*	B
VIN	12, 13	N/C	No effect	D
N/C	14	PGND	No effect	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1,2	Damage to internal power FET or FETs, other internal circuits, or both	A
BOOT	3	Damage to internal circuits	A
VCC	4	Damage to internal circuits for V_{IN} > 5.5V	A
RT	5	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, no damage occurs. For all other configurations, damage to internal circuits occurs for V_{IN} > 5.5V.	A
VSEL	6	Damage to internal circuits for V_{IN} > 5.5V	A
SYNC/MODE	7	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, no damage occurs. For all other configurations, damage to internal circuits occurs for V_{IN} > 5.5V.	A
$\overline{\text{RESET}}$	8	Damage to internal circuits	A
FB	9	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, damage to internal circuits occurs for V_{IN} > 16V. For operation in ADJ mode, damage to internal circuits occur for V_{IN} > 5.5V.	A
AGND	10	Possible damage to internal circuits or package	A
EN	11	No damage to device. Loss of ENABLE functionality	B
VIN	12, 13	No effect	D
N/C	14	No effect	D
PGND	15, 16	Possible damage to internal circuits or package	A

4.2 WSON Package

Figure 4-2 shows the LM636xx-Q1 pin diagram for the WSON package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM63625 data sheet.

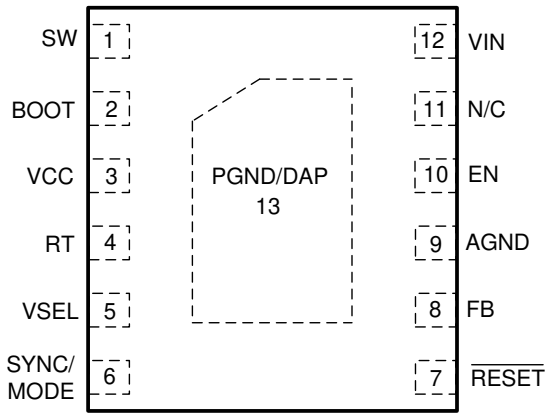

Figure 4-2. Pin Diagram for DRR0012E (WSON-12)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	Damage to internal power FET or FETs, other internal circuits, or both	A
BOOT	2	Damage to internal circuits	A
VCC	3	Fault mode shuts the device off.	B
RT	4	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, no effect is produced. If an RT resistor is used, the frequency is set to 2.1MHz. If a 0Ω jumper is used to connect the RT input to VCC, then the VCC output is pulled to ground; see "short to ground on pin 3."	B
VSEL	5	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, VCC is shorted to ground; see *short to ground on pin 3*. If a VSEL resistor is used or if the VSEL input is pulled to ground with a 0Ω jumper, then the output voltage is set to 3.3V before power up. No effect after power up.	B
SYNC/MODE	6	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, no effect is produced. If a 0Ω jumper is used to connect the SYNC/MODE input to VCC, then the VCC output is pulled to ground; see *short to ground on pin 3*	B
$\overline{\text{RESET}}$	7	$\overline{\text{RESET}}$ functionality is lost.	B
FB	8	The regulator operates at maximum duty cycle. Output voltage rises to nearly the input voltage (V_{IN}) level. Possible damage to customer load, output stage components, or both, can occur. No effect on device.	B
AGND	9	No effect	D
EN	10	Loss of ENABLE functionality The device remains in shutdown mode.	B
VIN	12	The device does not operate. No output voltage is generated. Output capacitors discharge through input short. Large reverse current can damage device.	A
N/C	11	No effect	D
PGND	13	No effect	D

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	With both pins open – loss of output voltage. With one pin open – some loss of device performance	B
BOOT	2	Loss of output voltage regulation; low or no output voltage. Possible device damage	A
VCC	3	VCC LDO is unstable. Loss of output voltage regulation and possible damage to internal circuits	A
RT	4	Device switching frequency drops to zero or becomes erratic. Loss of output voltage	B
VSEL	5	The device enters ADJ mode when EN or VIN is cycled. Incorrect output voltage if fixed VOUT mode was intended. No effect after power up	C
SYNC/MODE	6	Internal pulldown places the device in auto mode.	B
$\overline{\text{RESET}}$	7	$\overline{\text{RESET}}$ functionality is lost	B
FB	8	Loss of output voltage regulation. Output voltage can rise or fall outside of intended regulation window.	B
AGND	9	Loss of output voltage regulation. Possible damage to internal circuits	A
EN	10	Loss of ENABLE functionality. Erratic operation; probable loss of regulation	B
VIN	12	With both pins open – loss of output voltage. With one pin open – possible device damage	A
N/C	11	No effect	D
PGND	13	With either one or both pins open, there is possible device damage.	A

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	BOOT	Loss of output regulation, possible damage to internal circuits	A
BOOT	2	VCC	Loss of output regulation, possible damage to internal circuits	A
VCC	3	RT	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, VCC is shorted to ground; see *short to ground on pin 3*. For all other configurations, the effect is either be no change or erratic switching frequency with possible damage to device internal circuits.	A
RT	4	VSEL	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, VCC is shorted to ground; see *short to ground on pin 3*. For all other configurations, the effect is either be no change or erratic output voltage, switching frequency, or both; with possible damage to device internal circuits.	A
VSEL	5	SYNC/MODE	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, VCC is shorted to ground; see *short to ground on pin 3*. For all other configurations, the effect is either be no change or erratic operation, switching frequency, or both; with possible damage to device internal circuits.	A
$\overline{\text{RESET}}$	7	FB	Loss of regulation. Output voltage is unstable. Possible damage to device	A
FB	8	AGND	See *short to ground on pin 8*	B
AGND	9	EN	See *short to ground on pin 10*	B
EN	10	N/C	No effect	D
N/C	11	VIN	No effect	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	Damage to internal power FET or FETs, other internal circuits, or both	A
BOOT	2	Damage to internal circuits	A
VCC	3	Damage to internal circuits for V_{IN} > 5.5V	A
RT	4	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, no damage occurs. For all other configurations, damage to internal circuits occurs for V_{IN} > 5.5V.	A
VSEL	5	Damage to internal circuits for V_{IN} > 5.5V	A
SYNC/MODE	6	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, no damage occurs. For all other configurations, damage to internal circuits occurs for V_{IN} > 5.5V.	A
$\overline{\text{RESET}}$	7	Damage to internal circuits	A
FB	8	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, damage to internal circuits occur for V_{IN} > 16V. For operation in ADJ mode, damage to internal circuits occur for V_{IN} > 5.5V.	A
AGND	9	Possible damage to internal circuits or package	A
EN	10	No damage to device. Loss of ENABLE functionality	B
VIN	12	No effect	D
N/C	11	No effect	D
PGND	13	Possible damage to internal circuits or package	A

5 Revision History

Changes from Revision D (June 2022) to Revision E (March 2024) **Page**

- Corrected formatting throughout document....2
- Changed *SW Output to no output voltage* 5
- Changed *SW Output not in specification* to *Output not in specification* 5
- Corrected typo in document.... 5

Changes from Revision C (June 2021) to Revision D (June 2022) **Page**

- Changed BOOT description and failure class.... 7

Changes from Revision B (November 2020) to Revision C (June 2021) **Page**

- Added LM63610-Q1 to document.... 2

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