

# Reduce Conducted EMI in Automotive Buck Converter Applications

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#### **ABSTRACT**

Compliance to Electromagnetic Interference (EMI) standards often presents a significant challenge for many automotive design engineers. Adherence to EMI standards is a requirement for automotive electronic control units (ECUs), and automotive EMI standards are more stringent than those in the industrial and communication market segments. The buck converter is continuously switching during operation, making it one of the primary sources of noise in the system. Usually, it becomes easy to pass radiated EMI after conducted EMI passes. This article introduces how to reduce the conducted EMI of the buck converter in automotive applications through schematics, layout-optimization, and shielding.

Section 1 introduces automotive conducted EMI test standards. Section 2 provides the conducted emission model of a buck converter. Section 3 provides several methods to reduce EMI based on the noise model, along with test results to validate the effectiveness of each method. Section 4 summarizes tips to reduce automotive conducted EMI.

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#### **Trademarks**

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#### 1 Automotive Conducted EMI Test

Side view

Among the various automotive standards for conducted EMI, CISPR 25 is the essential international test standard. This chapter introduces the test setup and limit.

#### 1.1 Test Setup

Figure 1 is the test setup specified by CISPR 25, and Figure 2 is the test configuration photo for buck converter TPS560430-Q1. The power supply is a 12-V battery. The EUT is a TPS560430-Q1 board with an input filter. The board is placed 50 mm above the metal ground plane. The Artificial Network (AN), also known as a line impedance stabilization network (LISN), is inserted in the power supply to measure the noise emission from the buck converter.

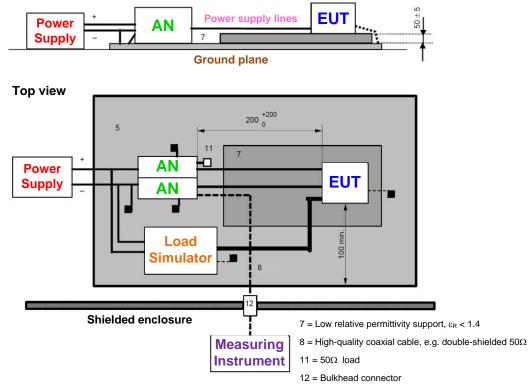


Figure 1. Conducted Emission Test Setup in CISPR 25



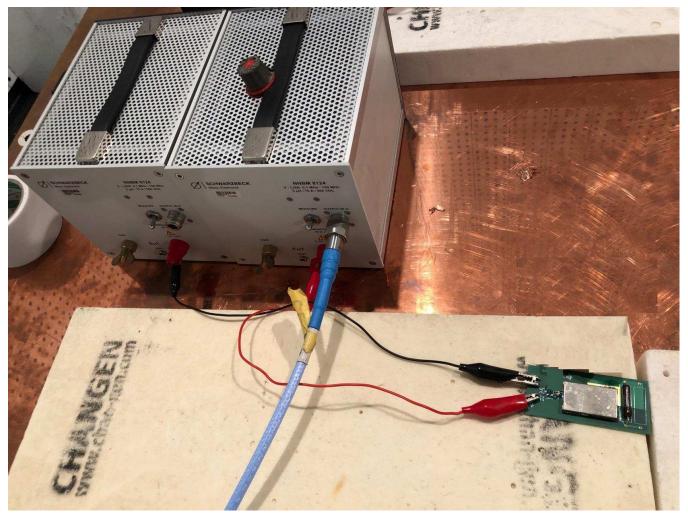


Figure 2. Test Setup Photo for Buck Converter TPS560430-Q1

## 1.2 Equivalent Circuit

Figure 3 is the equivalent circuit of the test setup with the internal schematic of the LISN. The LISN allows DC power into the harness of the EUT. The LISN also strips out RF noise coming from the EUT, and directs it to the RF-measurement equipment. The measurement equipment is configured for 50  $\Omega$  input.



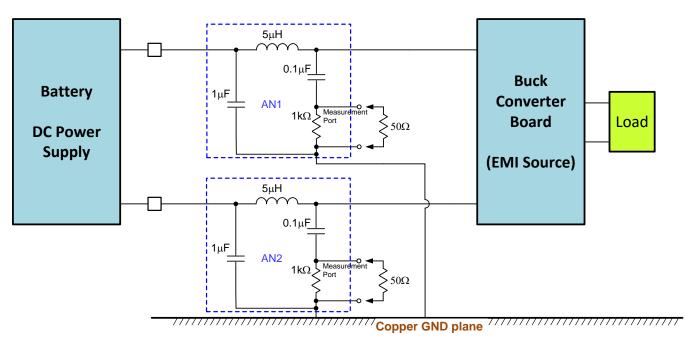


Figure 3. Equivalent Circuit of a Conducted Emission Test in CISPR 25

#### 1.3 Test Standard Limit

Table 1 lists the peak and average limits for conducted EMI according to CISPR 25. Class 5 is the most stringent. This test covers 150 kHz to 108 MHz in specific frequency bands (AM and FM radio, and mobile service bands). For CISPR 25, higher noise spikes are allowed in the gaps between the concerned frequency bands. However, some customers limit the noise in the frequency band gaps to the adjacent band limit due to special requirements.

The measurement frequency is up to 108 MHz, and the limit is quite tight. Parasitic capacitance and inductance, as well as near-field radiation, greatly influences the test results. These constraints make it much harder to pass conducted EMI standards for automotive applications than standards for industrial and communication applications.

	Levels in dB (μV)									
Frequen cy (MHz)	Class 1		Class 2		Class 3		Class 4		Class 5	
	Peak	Average	Peak	Average	Peak	Average	Peak	Average	Peak	Average
dcast										
0.15 - 0.3	110	90	100	80	90	70	80	60	70	50
0.53 - 1.8	86	66	78	58	70	50	62	42	54	34
5.9 - 6.2	77	57	71	51	65	45	59	39	53	33
76 - 108	62	42	56	36	50	30	44	24	38	18
41 - 88	58	48	52	42	46	36	40	30	34	24
Services										
26 - 28	68	48	62	42	56	36	50	30	44	24
30 - 54	68	48	62	42	56	36	50	30	44	24
68 - 87	62	42	56	36	50	30	44	24	38	18
	cy (MHz) dcast 0.15 - 0.3 0.53 - 1.8 5.9 - 6.2 76 - 108 41 - 88 Services 26 - 28 30 - 54	Cy (MHz) Peak    Coast	Peak   Average	Peak   Average   Peak   Average   Peak	Peak   Average   Peak   Average	Frequen cy (MHz)         Class 1         Class 2         Class 2         Class 3         Class 3         Class 4         Average         Peak         Averag	Frequen cy (MHz)         Class 1         Class 2         Class 3           Peak         Average         Peak         Average         Peak         Average           O.15 - 0.3         110         90         100         80         90         70           0.53 - 1.8         86         66         78         58         70         50           5.9 - 6.2         77         57         71         51         65         45           76 - 108         62         42         56         36         50         30           41 - 88         58         48         52         42         46         36           Services         26 - 28         68         48         62         42         56         36           30 - 54         68         48         62         42         56         36	Frequen cy (MHz)         Class 1         Class 2         Class 3         Class 3           Peak deast         Peak deast         Average         Peak deast         Average         Peak deast         Average deast         Peak deast         <	Frequen cy (MHz)         Class 1         Class 2         Class 3         Class 4           Peak         Average         Peak         Average         Peak         Average           0.15 - 0.3         110         90         100         80         90         70         80         60           0.53 - 1.8         86         66         78         58         70         50         62         42           5.9 - 6.2         77         57         71         51         65         45         59         39           76 - 108         62         42         56         36         50         30         44         24           41 - 88         58         48         52         42         46         36         40         30           Services         26 - 28         68         48         62         42         56         36         50         30           30 - 54         68         48         62         42         56         36         50         30	Frequen cy (MHz)         Class 1         Class 2         Class 3         Class 4         Class 4           Peak deast         Average         Peak Average

Table 1. Conducted Emissions Peak and Average Limits in CISPR 25



#### 2 Conducted Emission Model of Buck Converter

## 2.1 Ideal Conducted Emission Model

The Ideal Conducted EMI Model does not consider parasitic parameters or coupling effects. Instead, the noise level is calculated directly from the schematic. The result is only accurate at low frequency, and when the noise level is high. However, it is still useful, as it provides a starting point to calculate the EMI filter

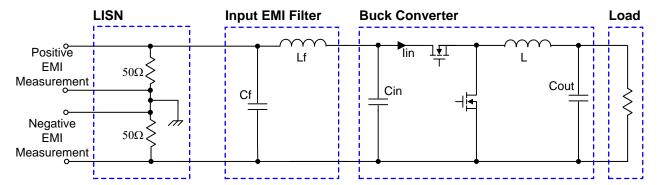


Figure 4. Ideal Conducted Emission Model of a Buck Converter

Figure 4 displays the ideal conducted emission model of a buck converter. The input current of a buck converter is the noise source. It conducts to the 50  $\Omega$  resistor of the LISN. The voltage on the two 50  $\Omega$  resistors is measured by a spectrum analyzer. This makes positive and negative EMI measurements obtainable.

In order to prevent the noise from conducting to the 50  $\Omega$  resistor of the LISN, an inductor and capacitor must be added at the input side of the buck converter as an EMI filter.

## 2.2 Conducted Emission Model Considering Parasitic Parameter

Inductors and capacitors are used in the EMI filter. Real inductors and capacitors are not ideal, as they have parasitic parameters. This makes them less effective at high frequency.

Figure 5 is the equivalent circuit model of a capacitor. Impedance is at its minimum value at resonant frequency. Ceramic capacitors are used in the EMI filter due to their low ESR. Figure 6 displays the impedance of ceramic capacitors with different capacitance. Capacitors with larger capacitance have lower resonant frequency, so using small and large capacitances in parallel filters the noise at both low and high frequencies.

Figure 5. Capacitor Equivalent Circuit



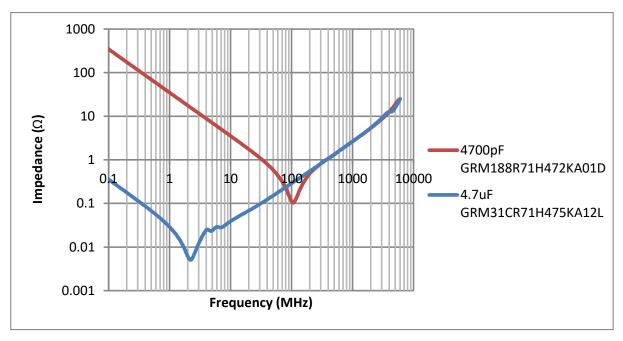


Figure 6. Variation of Impedance with Capacitance

Figure 7 is the equivalent circuit model of the inductor. It has self-resonant frequency (SRF) due to the parasitic parameters. In Figure 8, both Inductor1 (LQM21PN2R2MCA) and Inductor2 (LQM18PN2R2MGH) are 2.2 uH, but the impedance at high frequency is different. The impedance of the inductor decreases at the FM frequency band (76 MHz – 108 MHz). As such, it is recommended to add another filter stage with a ferrite bead, as it has a higher resonant frequency.

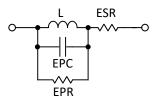


Figure 7. Inductor Equivalent Circuit



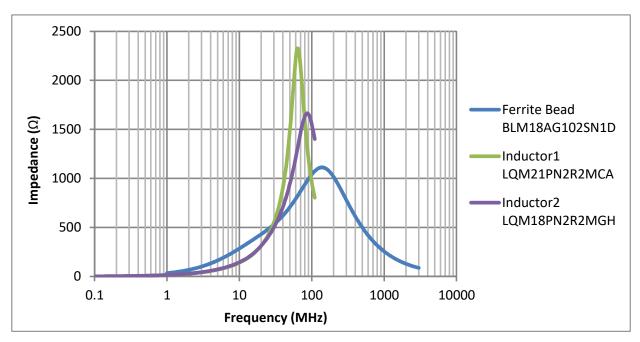


Figure 8. Impedance Comparison of Inductors and Bead

#### 2.3 Conducted Emission Model Considering Near Field Coupling

It is quite difficult to pass the FM band limit in CISPR 25 Class 5. One reason, explained in Chapter 2.2, is that the performance of the EMI filter becomes worse at high frequencies. Another reason is near-field coupling. High-frequency noise will generate stronger electric and magnetic fields, which will couple to the front of EMI filter and make measurement results worse.

Figure 9 is an example of electrical coupling. Electrical field coupling is modeled as a parasitic capacitor Csw(par). The SW pin of the buck converter has high dv/dt, and big harmonics at high frequency. This causes high-frequency noise flow, as displayed in Figure 9. The differential filter has almost no effect on this noise from the model.

There are several ways to reduce the near-field electrical coupling effect:

- Reduce the noise source. Adding a boot resistor, a snubber, or decreasing the switching frequency will
  decrease the high-frequency harmonics of the noise source.
- Reduce the Csw(par). Place as little PCB SW copper as possible, but consider the thermal dissipation. Adding a shielding case also reduces electrical field coupling.
- Add filter components. A common-mode choke can be added, but the system cost will increase.



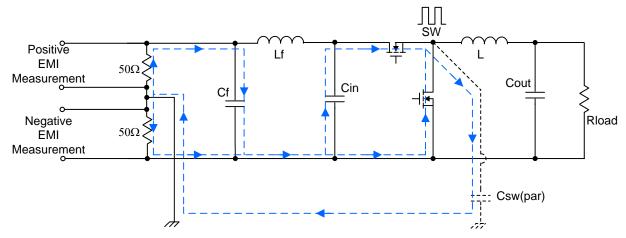


Figure 9. Electrical Coupling Example

As shown in Figure 10, near-field magnetic coupling is another path. Magnetic field coupling is modeled as mutual inductance Lm. The high-frequency harmonics in the input current generate a magnetic field, which jumps over the input EMI filters and couples to the LISN. Another magnetic noise source is the power inductor.

There are also several ways to reduce the near-field magnetic coupling effect:

- Reduce the noise source. Adding the boot resistor, snubber, or decreasing the switching frequency will
  decrease high-frequency harmonics of the input current.
- Reduce the magnetic field of the noise. Keep the input-critical loop area as small as possible.
   Figure 10 displays the critical loop of the buck converter. A shielded power inductor is recommended, since it has less magnetic field leakage.
- Reduce the magnetic field coupled to the LISN. Place the front of input filter far from the noise source. The near-field coupling strength is approximately inversely proportional to cube of distance, so a small distance change can greatly influence the test result.

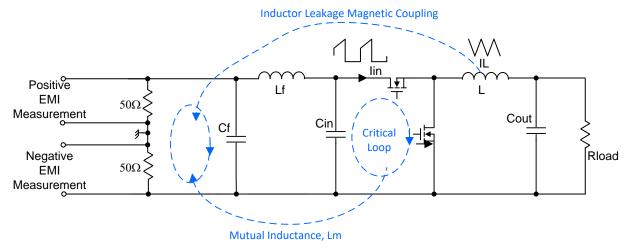


Figure 10. Magnetic Coupling Example



#### 3 Reduce Conducted EMI of Buck Converter

The conducted emission model of a buck converter is introduced in Section 2. Based on the model, the EMI filter is designed as shown in Figure 11. Input voltage is 12-V, while the output is 3.3-V / 330-mA. A low-frequency EMI filter with inductor is placed as the second stage. A high-frequency filter with a ferrite bead is placed close to the buck converter. This filter serves as the first stage. The placement of the ferrite bead is discussed, in detail, in Chapter 3.2. The high-frequency, common-mode noise can be filtered by a common-mode choke. This choke serves as the third stage, far from the noise source. It is optional if using other techniques described in this section. The buck converter PCB, with first and second filter stages, is displayed in Figure 12.

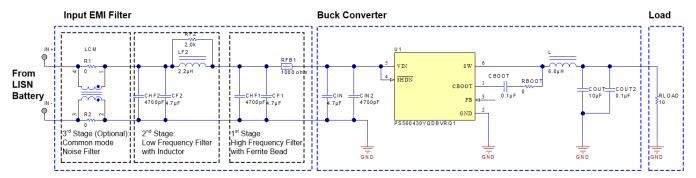


Figure 11. Buck Converter Schematic with 3-Stage EMI Filter

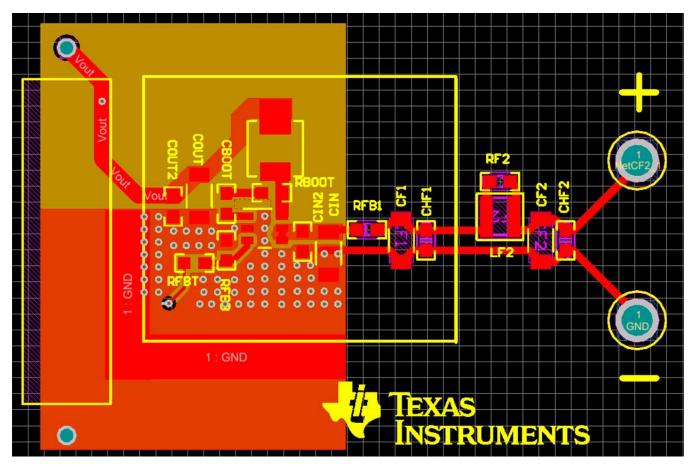


Figure 12. Buck Converter PCB with 2-Stage EMI Filter



Figure 13 shows the circuit testing results. A third-stage, common-mode filter was not used. The circuit passed the CISPR 25 Class 3, but failed the CISPR 25 Class 4 at the FM band. Several solutions are discussed in this section.

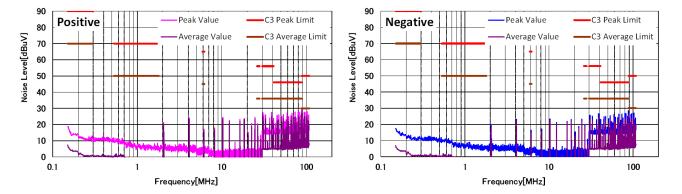


Figure 13. Noise with 2-Stage EMI Filter Against the CISPR 25 Class 3 Standard

#### 3.1 Reduce Noise Source

To reduce the noise source, the first step is to identify the critical noise source. As shown in Figure 13, the high-frequency EMI is usually difficult to pass. This makes noise sources with large, high-frequency harmonics critical. SW voltage, input current, and inductor current are signals with relatively large amplitude. Figure 14 and Figure 15 display the waveforms and FFT analysis results. The FM band noise generated by the input current, and the SW voltage, are high, but the inductor current has lower high-frequency noise. This means the SW voltage and input current are critical noise sources. The waveforms with sharply rising and falling edges have high-frequency noise.



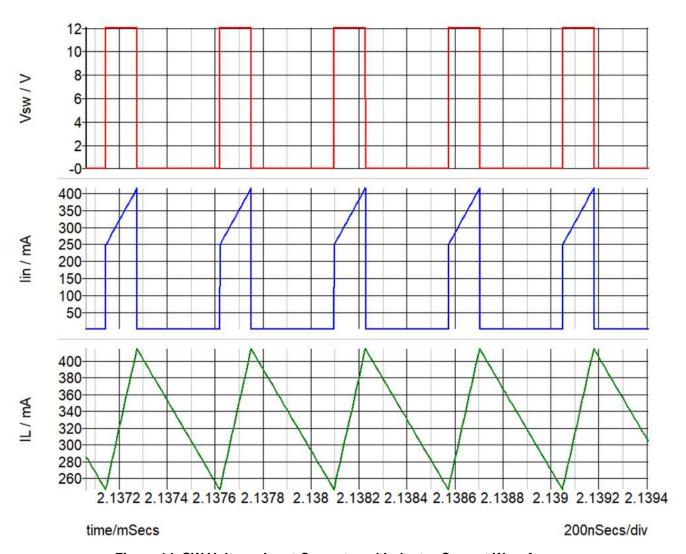


Figure 14. SW Voltage, Input Current, and Inductor Current Waveforms



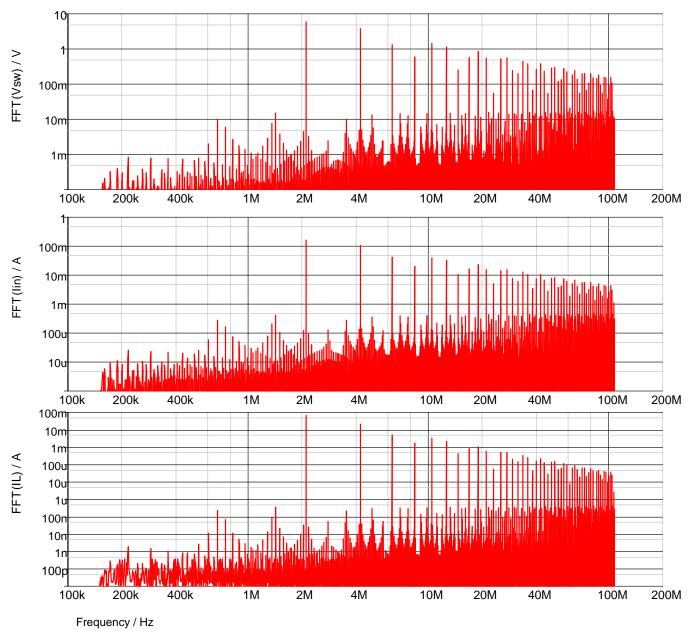


Figure 15. FFT Analysis of SW Voltage, Input Current, and Inductor Current

Reducing the high-frequency noise of the input current and SW voltage involves decreasing the switching frequency and output current, as well as adding a boot resistor and snubber to the low-side FET.

Figure 16 shows the SW waveform with 0  $\Omega$ , and 75  $\Omega$  boot resistor. After adding the 75  $\Omega$  boot resistor, the SW rising edge is slowed down, and the SW overshoot is much smaller. Figure 17 is the EMI Testing Result with a 75  $\Omega$  boot resistor. Compared to Figure 13, the RF band performance is better.



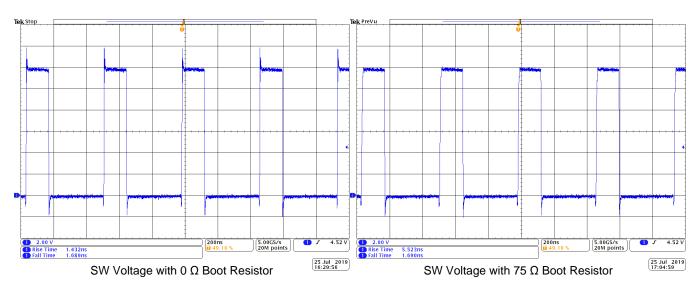


Figure 16. Impact of a Boot Resistor to SW Voltage

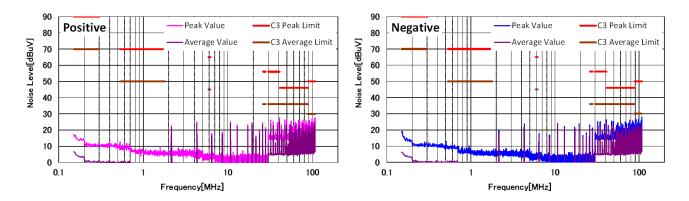


Figure 17. EMI Testing Result with a 75  $\Omega$  Boot Resistor

#### 3.2 Filter Components

Figure 11 displays the 3-stage EMI filter of a buck converter. The cost of the third-stage, common-mode choke is high, and is optional if using other techniques. The second stage is the main input-noise filter. It is composed of a 2.2 uH inductor, and 4.7 uF ceramic capacitor. The resistor, in parallel with the inductor, prevents filter stability issues. The ferrite bead used in the first stage must have a high resonant frequency, and high impedance, at the RF band. The BLM18AG102SN1D was chosen in this stage. The impedance characteristics of the device are displayed in Figure 18.

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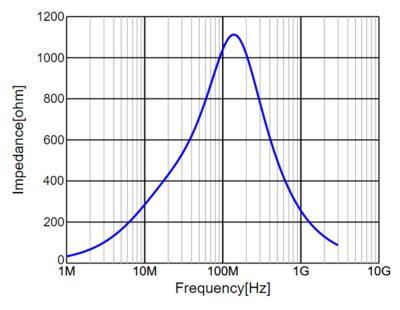


Figure 18. Impedance Characteristics of the First-Stage Bead

The ferrite bead must be placed very close to the IC. This ensures the bead can filter high-frequency noise immediately, and prevent coupling to other places. If the ferrite bead is not placed close to the IC, like in Figure 19, the EMI test results are worse. This is displayed in Figure 20.

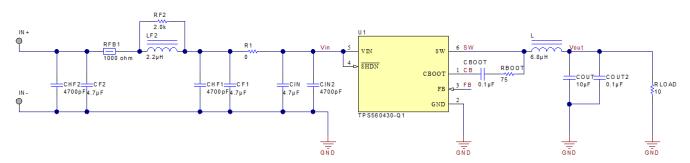


Figure 19. Improper Input Filter with Ferrite Bead Not Placed Near the IC

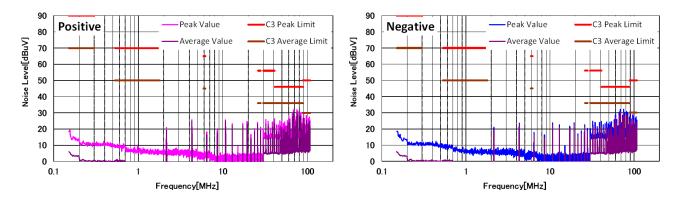


Figure 20. EMI Testing Result with the Ferrite Bead not Placed Near the IC



#### 3.3 Layout Consideration

Layout is critical in reducing high-frequency noise coupling, as explained in Chapter 2.3. Figure 12 is the recommended layout for synchronous buck converter TPS560430-Q1. The most important points are:

- 1. As shown in Figure 10, keep the input-critical loop area as small as possible. For a synchronous buck converter with high and low side MOS integrated in the IC, the input capacitor should be placed close to the IC VIN pin and the GND pin. A small-package input capacitor can lead to smaller input-loop area. For a non-synchronous buck converter, the critical loop is composed of the input capacitor, the low-side diode, the IC SW pin, and the VIN pin. The IC GND pin is not in this critical loop. A small-package input capacitor and diode can shrink this loop as well.
- 2. The GND layer underneath the critical loop must be complete. Mirror current flows in this GND layer and helps reduce the equivalent critical loop area.
- 3. The IC internal bootstrap circuit drives the high-side FET of the buck converter. It is also a noise source. A boot capacitor and resistor must be placed close to the IC CB pin and SW pin.
- 4. The SW copper area must be kept as small as possible, but consider heat dissipation. Do not use vias to connect the SW to more than one layer. Power inductors with small package size also reduce the SW area.
- 5. The snubber circuit helps reduce SW overshoot. Place it close to low-side FET of the buck converter to maximize the effect and improve EMI.
- 6. To filter high-frequency noise immediately, place the input filter bead close to the IC.
- 7. Placing the front of the input filter far from the IC and power inductor will prevent noise from skipping the input filter, and from coupling to the input power line directly.
- 8. Do not place copper underneath, or surrounding, the input EMI filter. Noise may flow in the copper, and couple to the input power line directly.
- 9. Do not use a wide trace to connect the filter capacitor (including the input capacitor, output capacitor of the buck converter, and the EMI filtering capacitor). As shown in Figure 21, the wide copper allows some noise flow to bypass the filter capacitor. Figure 22 displays the recommended method: forcing noise to pass the filter capacitor.
- 10. Do not place the first-layer GND copper under the power inductor or surrounding SW. Noise may couple to the GND copper, and then radiate outside.
- 11. The back-side GND layer works like a shielding case for the noise source. Keep it complete, and use multi vias to ensure a low-impedance connection. This is further discussed in Chapter 3.4.

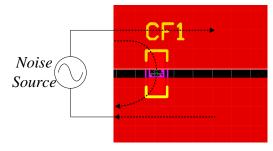


Figure 21. Wide Copper Allows Noise to Bypass the Filter Capacitor

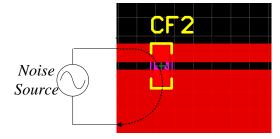


Figure 22. Force Noise to Pass the Filter Capacitor



Every tip listed previously has some effect in reducing high frequency noise. For example, to verify tip 4, another PCB is made. It has the same schematic with Figure 11, but different a layout from Figure 23. Compared to Figure 12, the power inductor is rotated to form a smaller output-inductor loop, but generates a bigger SW area. As stated in Chapter 3.1, inductor current has a lower FM-band noise level than SW voltage. Therefore, the EMI performance tested in Figure 24 is worse than the result in Figure 13.

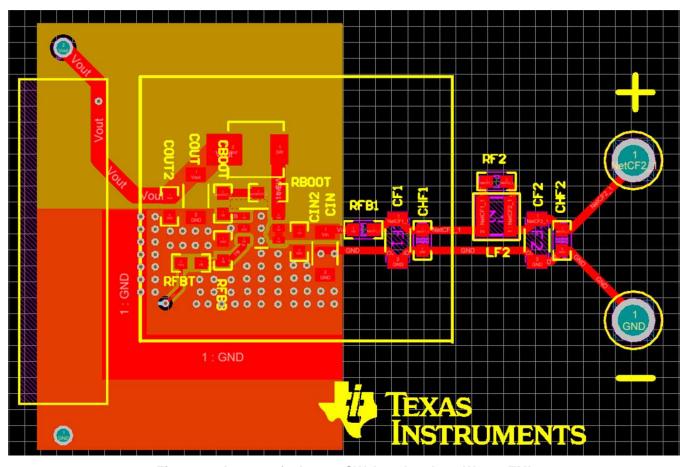


Figure 23. Layout of a Larger SW Area Leads to Worse EMI

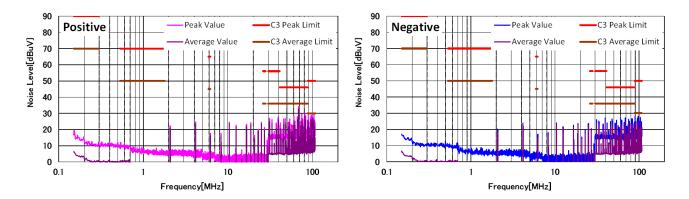


Figure 24. EMI Testing Result with the Layout of Larger SW Area



#### 3.4 Shielding

Shielding is effective in reducing near-field coupling. As displayed in Figure 9, electrical field coupling is modeled as a parasitic capacitor Csw(par) from the switch node of a buck converter to the GND plane, which is connected to the LISN. As shown in Figure 25, adding a metal box over the noise source means that SW noise can only couple to the shielding box, rather than the LISN GND. It is important to ensure a good connection between the shielding box and the power GND of the buck converter. This ensures the electrical field is shorted to the ground immediately.

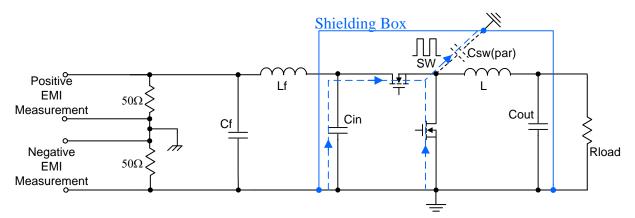


Figure 25. Shielding Box Reduces Electrical Feld Coupling

If noisy components and traces are placed on the top layer, the bottom layer works as part of the shielding box. It is recommended to pour a complete copper on the bottom layer, and use multi vias to connect it to the buck converter GND.

Sometimes, rotating the direction of the power inductor changes EMI performance. This is even true with a shielded inductor. The reason is similar to the shielding box effect. As seen in Figure 26, for a multi-wound inductor, pin one is connected to the inner side of the wires, while pin two is connected to the outside of the wires. The multi-wound wire acts like shielding box. Aligning pin one of the inductor to the switch node, rather than to the output voltage, reduces electrical field coupling.

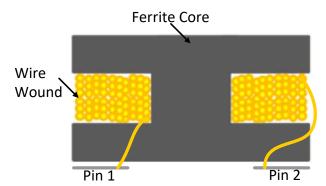


Figure 26. Multi-Wound Inductor Cross-Section Image

As seen in Figure 10, magnetic fields can also be reduced by adding an iron shielding box. The permeability of iron is much higher than air, so magnetic flux will flow in the iron box, rather than couple to the front of the EMI filter. Using a shielded inductor also helps to reduce magnetic field coupling.

Figure 27 shows the position of the shielding box on the PCB. The switch node, input current loop, and power inductor are inside the shielding box, while the front of EMI filter is outside of the box. The shielding box is soldered to the buck converter GND at the bottom-left corner for good electrical connection.



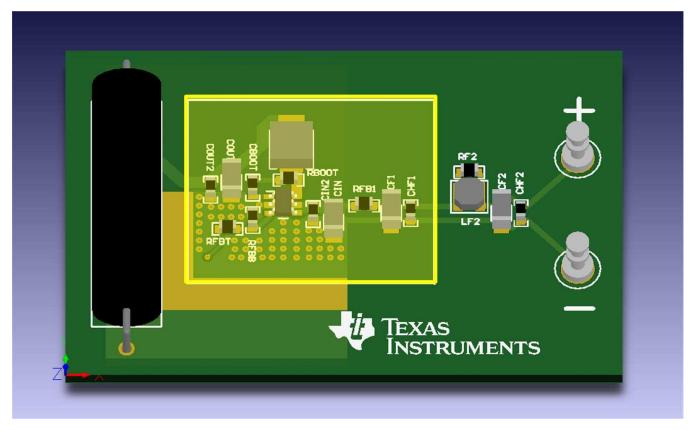


Figure 27. Position of the Shielding Box on PCB

Figure 28 shows the EMI test result with an iron shielding box. CISPR 25 Class 5 passed successfully. Compared to Figure 17, EMI performance is greatly improved by the shielding box.

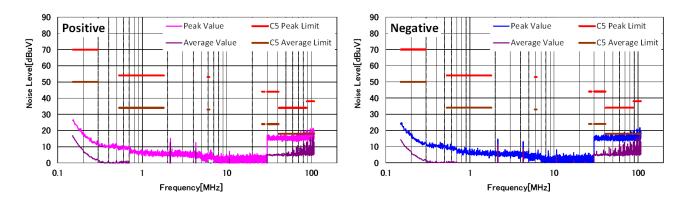


Figure 28. Noise with Shielding Box Against the CISPR 25 Class 5 Standard

## 4 Summary of Tips to Reduce Buck Converter Conducted EMI

Tips to reduce buck converter conducted EMI are summarized in this section.

From the schematic and components side:

1. Use the 3-stage input EMI filter shown in Figure 11. The high-frequency filter with a ferrite bead is placed close to the buck converter, and serves as the first stage. The low-frequency EMI filter with an inductor is placed as the second stage. The third-stage, common-mode choke is optional. It serves as the last step if high-frequency noise can not be eliminated.



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- 2. Use small capacitance, in parallel with the big capacitance, in the input EMI filter.
- 3. Place a small-package input capacitor close to the IC. Choose a low-side diode with a small package for a non-synchronous buck converter.
- 4. Choose a ferrite bead with high impedance at the FM band.
- Add a boot resistor.
- 6. Add a snubber circuit.
- 7. Decrease the switching frequency
- 8. Choose a shielded power inductor.
- 9. Add an iron shielding box.

#### From PCB layout side:

- Keep the input-critical loop area as small as possible. For a synchronous buck converter, the input capacitor should be placed close to the IC VIN pin and GND pin. For a non-synchronous buck converter, the critical loop is composed of
  - · an input capacitor
  - low-side diode
  - IC SW pin
  - VIN pin
- 2. Keep the GND layer underneath the critical loop complete.
- 3. Place the boot capacitor and resistor close to IC.
- 4. Place the snubber circuit close to the low-side FET of the buck converter.
- 5. Keep the SW copper area as small as possible while considering heat dissipation. Do not use vias to connect the SW to more than one layer.
- 6. Place the input ferrite bead close to the IC.
- 7. Place the front of input filter far from the IC and power inductor.
- 8. Do not place copper underneath, or surrounding, the input EMI filter.
- 9. Do not use wide trace to connect the filter capacitor.
- 10. Do not place the first-layer GND copper under the power inductor, or surrounding SW.
- 11. Keep the back-side GND layer complete, and use multi vias to connect it to the buck converter GND.
- 12. Place the shielding box so that the switch node, input current loop, and power inductor are inside the shielding box, and the front of EMI filter is outside of the box.
- 13. Solder the shielding box to the buck converter GND for a good electrical connection.
- 14. Align pin one of the power inductor to the switch node, rather than to the output voltage.

#### 5 References

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