# Mitigating the Indeterminate Output of a Voltage Supervisor (Reset IC) During Power Up/Down

### What is the indeterminate output voltage issue on the output of a voltage supervisor?

Voltage Supervisors (Reset ICs) require a minimum voltage called the Power-on-Reset Voltage ($V_{POR}$) on the supply pin before the internal circuitry that creates the voltage reference for comparing the sensed voltage is operational. Specifically, $V_{POR}$ defines the minimum required voltage threshold to turn on the internal output MOSFET (circled in RED in Figure 1) that defines the output logic state. When the supply voltage is below $V_{POR}$, the output logic state is undefined and the output voltage is indeterminate. The indeterminate output voltage only appears at the output ($\overline{RESET}$) of an active-low Voltage Supervisor when VDD is below $V_{POR}$.

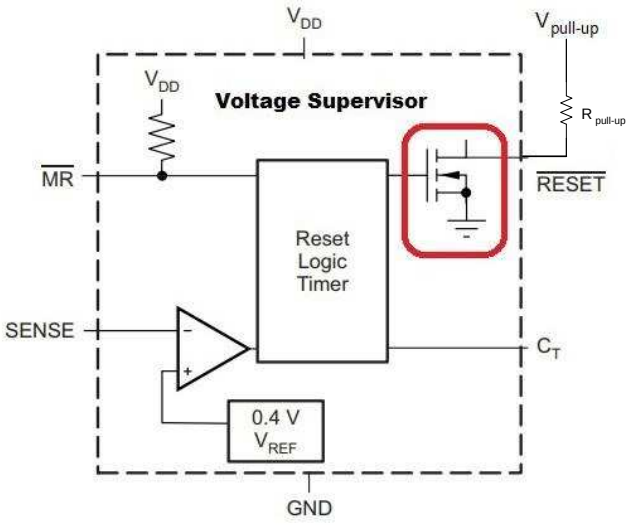


**Figure 1. Voltage Supervisor Latch Circuit**

When $V_{DD}$ is below $V_{POR}$, there isn't enough voltage for the internal circuitry driving the output MOSFET to operate so the output MOSFET is off and the supervisor has no way to control the output $\overline{RESET}$ voltage. As shown in Figure 2, $\overline{RESET}$ will rise up in proportion to the pull-up voltage, $V_{PULL-UP}$, until the voltage at $V_{DD}$ is above $V_{POR}$ to provide enough voltage to turn on the internal MOSFET to pull $\overline{RESET}$ to GND. Since $\overline{RESET}$ may have a voltage potential when $V_{DD}$ is not above the undervoltage threshold ($V_{IT}$) of the supervisor, an error could result in the system.

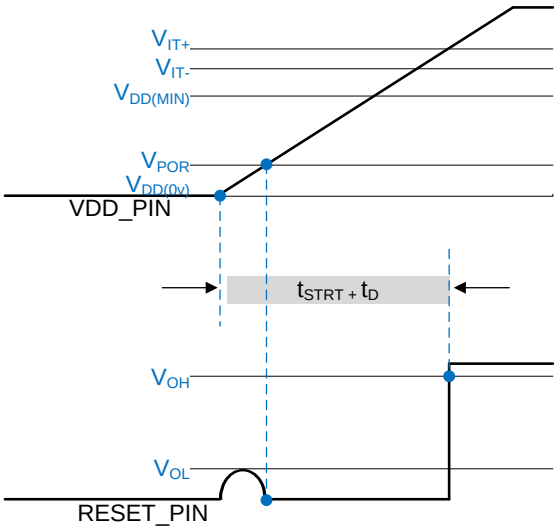




**Figure 2. Timing Diagram of Device Startup**

Once $V_{DD}$ is above $V_{POR}$, the internal MOSFET turns on, connects $\overline{RESET}$ to GND, and causes $\overline{RESET}$ to output the correct low logic level.

For active-high output devices, the same indeterminate voltage occurs when $V_{DD}$ is below $V_{POR}$, but when $V_{DD}$ is below $V_{IT}$, the device is supposed to pull-up to logic high anyway, so seeing a voltage potential at $\overline{RESET}$ in this case is not considered an issue.

### How to prevent the indeterminate output voltage when $V_{DD}$ is below $V_{DD\ (min)}$?

In the case the system cannot accept the output voltage being undefined when $V_{DD}$ is below $V_{POR}$, adding a P-channel junction field effect transistor (JFET), to $\overline{RESET}$ as shown in Figure 3 ensures that the output remains low even during power up and power down.

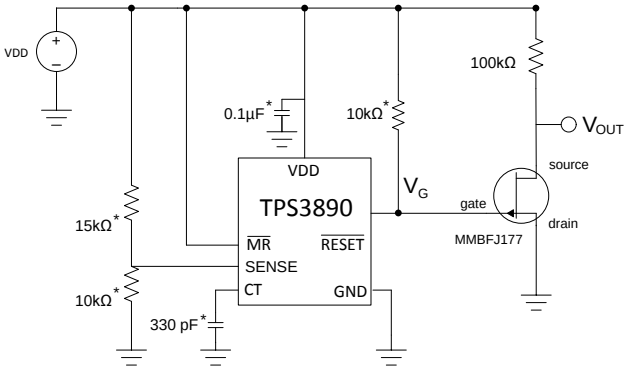


**Figure 3. Adding a P-type JFET to Mitigate the Indeterminate Output Voltage**

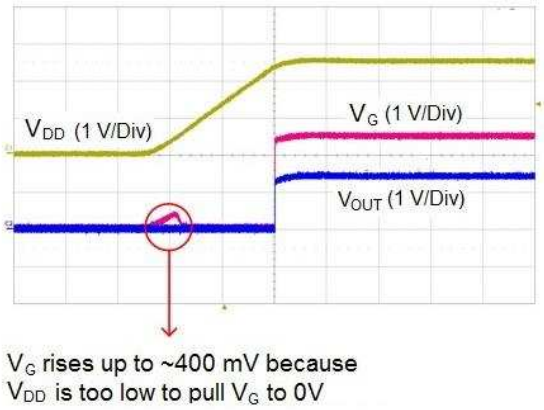


**Figure 4. TPS3890 Start-up with JFET (Blue Trace) and without JFET (Pink Trace)**

In Figure 3, the normal output of the TPS3890 voltage supervisor is represented as $V_G$. When $V_{DD}$ rises, the voltage at $V_G$ also rises because the internal circuitry driving the MOSFET is not operational yet. By adding a standard JFET configured in a source-follower configuration, the voltage at the source (labeled as $V_{OUT}$) will follow the voltage at $V_G$ minus the threshold voltage of the JFET. The threshold of the JFET causes approximately a 1V drop between $V_G$ and $V_{OUT}$ and eliminates the voltage potential rise on the output until the internal circuitry becomes operational. Note: when connecting the $V_{OUT}$ of the JFET to the next device, the user must account for the drop in output voltage caused by the JFET threshold.

Figure 4 shows the effect of using a JFET on the output of a TPS3890. The Yellow trace shows the power supply at $V_{DD}$, the Pink trace shows the rising indeterminate system output as $V_{DD}$ rises using just the voltage supervisor, and the Blue trace shows the system output remaining low as $V_{DD}$ rises using the voltage supervisor with the additional JEFT.

This solution can be used for all active-low supervisors with proper choice of the JFET and pull-up resistor. The selected JFET should have a voltage threshold higher than $V_{POR}$ so the JFET remains turned on connecting the system output to GND until after $V_{POR}$ in which the voltage supervisor internal circuitry is operational and causes system output to be in the correct defined logic state. The selected pull-up resistor should be low enough for the required system output response time and high enough to minimize the voltage drop across the JFET when conducting.

**Table 1. Alternative Device Recommendations**

| Device | Description |
|---|---|
| TPS3808 | SOT package type |
| TPS389x | Additional output topologies, higher $V_{DD\ (max)}$ |

## IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265