Analog Engineer's Circuit

Window Comparator with Integrated Reference Circuit

Design Goals

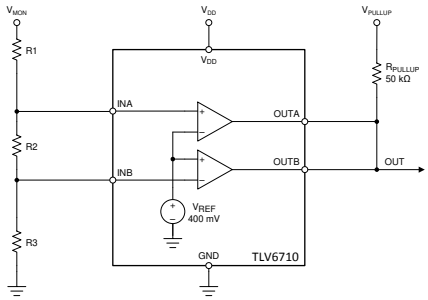
Input		Output		Supply	
$V_{MON\ Min}$	$V_{MON\ Max}$	$V_{OUT\ Min}$	$V_{OUT\ Max}$	V_{DD}	V_{REF}
0 V	6 V	0 V	3.3 V	3.3 V	400 mV

Lower Threshold (V_L)	Upper Threshold (V_H)	Divider Load Current (I_{MAX}) at V_H
3.2 V	4.1 V	10 µA

Design Description

This circuit utilizes the TLV6710, which contains two comparators and a precision internal reference of 400mV. The monitored voltage (V_{MON}) is divided down by R_1, R_2, and R_3. The voltage across R_2 and R_3 is compared to the 400 mV internal reference voltage (V_{REF}). If the input signal (V_{MON}) is within the window, the output is high. If the signal level is outside of the window, the output is low.

The TLV6710 will be utilized for this example, which conveniently contains two comparators and a common precision internal reference trimmed to a 400 mV threshold. Two discrete comparators and an external reference may also be used.



Design Notes

1. Make sure the comparator input voltage range is not violated at the highest expected V_{MON} voltage.
2. If the outputs are to be combined together (ORed), open collector or open drain output devices *must* be used.
3. It is also recommended to repeat the following calculations using the minimum and maximum resistor tolerance values and comparator positive and negative offset voltages.
4. The TLV6710 has built-in asymmetrical hysteresis, resulting in the rising edge V_L and falling edge V_H being slightly shifted. Comparators without hysteresis will meet the calculated thresholds.

Design Steps

The resistor divider will be calculated in separate V_H and V_L segments to create 400 mV at the appropriate comparator input at the desired threshold voltage.

1. The total divider resistance R_{TOTAL} is calculated from the upper threshold voltage and divider current:

$$R_{TOTAL} = R_1 + R_2 + R_3 = \frac{V_H}{I_{MAX}} = \frac{4.1V}{10\mu A} = 410k\Omega$$

2. The upper threshold voltage is set by the *bottom* divider resistor R_3 going into the INB pin. From the reference voltage and the divider current, the value of R_3 is calculated from:

$$R_3 = \frac{V_{REF}}{I_{MAX}} = \frac{400mV}{10\mu A} = 40k\Omega$$

3. The *middle* resistor R_2 is found by looking at R_2 and R_1 as one resistor, and calculating the value for that total resistance for V_{REF} at V_L, then subtracting out the known R_3:

$$R_2 = \left(\left(\frac{R_{TOTAL}}{V_L} \times V_{REF}\right) - R_3\right) = \left(\left(\frac{410k\Omega}{3.2V} \times 400mV\right) - 40k\Omega\right) = 11.25k\Omega$$

4. R_1 is found by taking the total resistance and subtracting the sum of R_2 and R_3:

$$R_1 = R_{TOTAL} - (R_2 + R_3) = 410k\Omega - (11.25k\Omega + 40k\Omega) = 358.75k\Omega$$

Because these are calculated ideal resistor values, the next closest 0.1% standard resistor values will be used. The following table summarizes the changes due to the resistor value changes and the resulting trip point voltage change.

Nearest 0.1% Resistor Values

Resistor	Calculated Ideal Value	Nearest Standard 0.1% (E192) Value
R_1	358.750 kΩ	361 kΩ
R_2	11.25 kΩ	11.3 kΩ
R_3	40 kΩ	40.2 kΩ

Because the values of the divider string resistors were changed, the resulting new threshold voltages must be calculated. The thresholds are found by multiplying the divider ratio by the reference voltage:

$$V_H = \left(\frac{R1 + R2 + R3}{R3}\right) \times V_{REF} = \left(\frac{361k\Omega + 11.3k\Omega + 40.2k\Omega}{40.2k\Omega}\right) \times 0.4V = 10.26119 \times 0.4V = 4.1045 \quad V$$

$$V_L = \left(\frac{R1 + R2 + R3}{R2 + R3}\right) \times V_{REF} = \left(\frac{361k\Omega + 11.3k\Omega + 40.2k\Omega}{11.3k\Omega + 40.2k\Omega}\right) \times 0.4V = 8.0097 \times 0.4V = 3.2039 \quad V$$

Ideal and Standard Resistor Thresholds

Threshold	Using Ideal Resistors	Using Standard Resistors	Percent Change
V_H	4.1 V	4.1045 V	+0.109%
V_L	3.2 V	3.2039 V	+0.121%

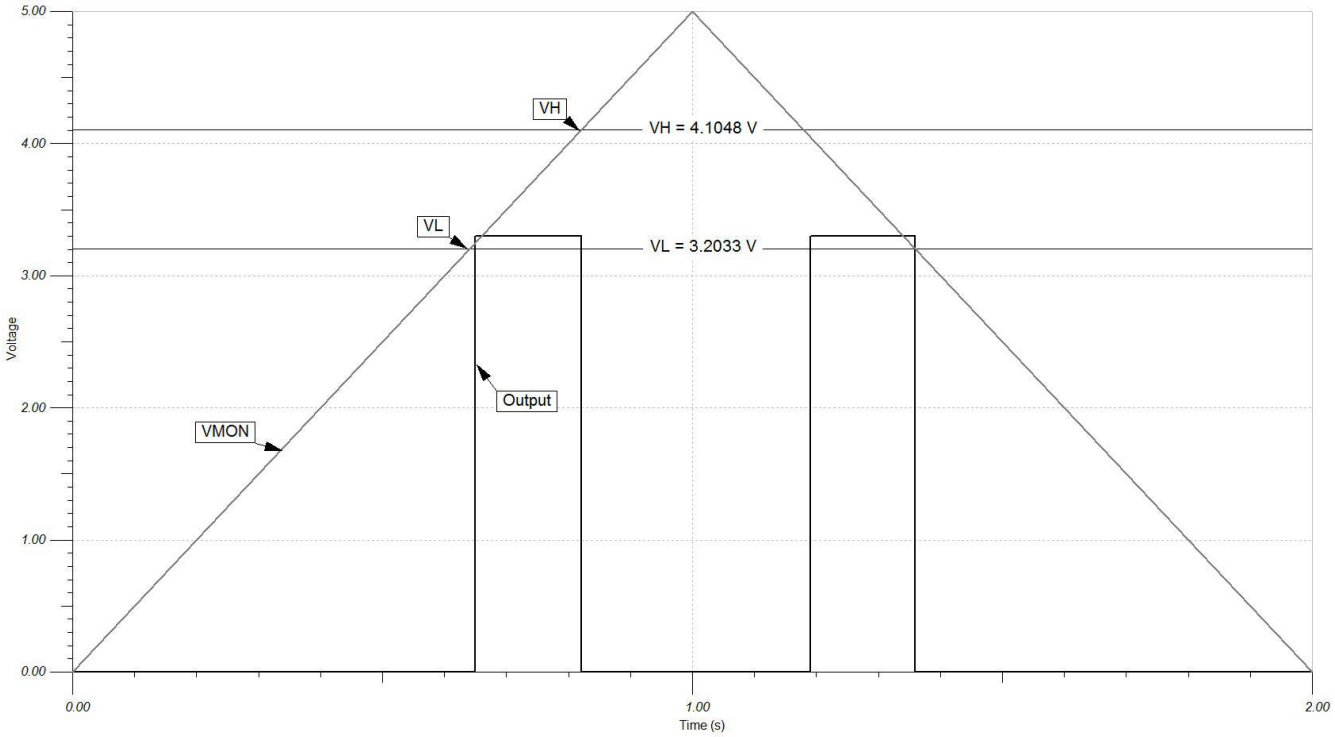
To ensure that the maximum 6V V_{MON} voltage does not violate the TLV6710 1.7 V maximum input voltage rating, the V_{MON_MAX} and the V_L division ratio found in step 4 above are used to calculate the maximum voltage at the TLV6710 input:

$$V_{INPUT\_MAX} = \frac{V_{MON\_MAX}}{V_{L\_RATIO}} = \frac{6\ V}{8.0097} = 749.1 \quad mV$$

The value 749 mV is less than 1.7 V, so the input voltage is well below the input maximum. If using discrete comparators, make sure the voltage is within the specified input common mode range (V_{ICR}) of the device used.

Design Simulations

Transient Simulation Results



Note: The Rising edge V_L and falling edge V_H thresholds are slightly shifted due to the built-in asymmetrical hysteresis of the TLV6710. Comparators without hysteresis will meet the calculated thresholds.

Design References

For more information on many comparator topics including input voltage range, output types and propagation delay, please visit TI Precision Labs - Comparator Applications.

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See TINA-TI™ TLV6710 Reference Design circuit simulation file, Literature Number SNVMB09.

Design Featured Comparator

TLV6710	
V_{ss}	2 V to 36 V
V_{inCM}	0 V to 1.7 V
V_{out}	0 V to 25 V
Vref	400 mV ±0.25%
I_q	11 µA
I_b	1 nA
Prop Delay	10 µs
#Channels	2
TLV6710	

Design Alternate Comparator

TLV6700	
V_{ss}	1.8 V to 18 V
V_{inCM}	0 V to 6.5 V
V_{out}	0 V to 18 V
Vref	400 mV ±0.5%
I_q	5.5 µA
I_b	1 nA
Prop Delay	29 µs
#Channels	2
TLV6700	

Design Alternate Comparator

TLV1702	
V_{ss}	2.7 V to 36 V
V_{inCM}	Rail to Rail
V_{out}	Open Drain to 36 V
V_{os}	±3.5 mV
I_q	75 µA
I_b	15 nA
Prop Delay	0.4 µs
#Channels	2
TLV1702	

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