Application Report
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Optimizing Efficiency Through Dead Time Control With the LMG1210 GaN Driver

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ABSTRACT

Dead time is an extremely important design parameter in some high-frequency converters using GaN. Dead time becomes ever more important as the frequency of operation increases. This report demonstrates the need for dead time optimization by measuring efficiency of a converter with varying dead times. This report also discusses the various sources of propagation delay mismatch which cause dead time variations and presents measurements to quantify these variations on the LMG1205 and the LMG1210 drivers.

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Trademarks

1 Third Quadrant Losses

The third quadrant loss in a FET occurs when the current flows from the source to drain while the FET gate is low (FET is off). In silicon FETs, there is a parasitic body diode in the structure which typically turns on at about 0.7 V. GaN HEMTs do not have a P-type material, hence the body diode is absent.

The conduction from drain to source happens when the drain drops below the gate by more than the threshold voltage of the device (V_T). When this happens, the FET turns on *backwards* with the gate to drain voltage turning on the device. To turn on the FET, the drain must fall below the gate by more than the V_T of the device, and then drop further to support the channel current. This effectively appears as a 2-V drop plus a drop proportional to 1/gm.

In a power converter, there is typically a short time in each cycle—the dead time—where neither switch is on and the inductor current is forced to flow through one of the FETs in third-quadrant mode.

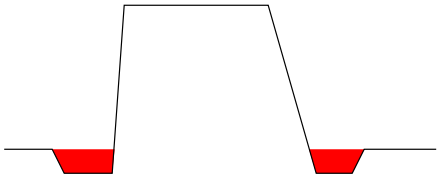


Figure 1. Idealized Buck Switch Node Waveform. The Red Area is the Dead Time Loss.

Figure 1 shows an idealized waveform of the switching node in a buck converter with dead time losses highlighted graphically in red.

The energy lost in the dead time is proportional to the current, voltage, and the amount of time spent in this mode, which corresponds directly to the dead time for the half-bridge. The energy lost in each dead time is shown in Equation 1:

$$E_{Dead} = T_{Dead} \times V_{Dead} \times I_L \quad (1)$$

where

- I_L is the inductor current during the dead time,
- V_{Dead} is the source-drain voltage during the dead time,
- and T_{Dead} is the dead time.

The power loss is shown in Equation 2:

$$P_{Dead} = \left(E_{Dead1} + E_{Dead2}\right) \times F_{SW} \quad (2)$$

where

- E_{Dead1} and E_{Dead2} are the energy lost during each dead time,
- and F_{SW} is the switching frequency.

Assuming the two dead times are equal and the user can substitute 1 into 2 and use Equation 3:

$$P_{Dead} = 2 \times T_{Dead} \times V_{Dead} \times I_L \times F_{SW} \quad (3)$$

The dead time is directly proportional to this loss and must be minimized to achieve high efficiency.

As an example of a system where this is particularly impactful, consider a 12-V to 1.8-V buck converter using an integrated half-bridge EPC2100 device operating at 5 MHz. In this example, both dead times were set to the same value. The effective dead times were measured by observing the switch node as shown in Figure 2.

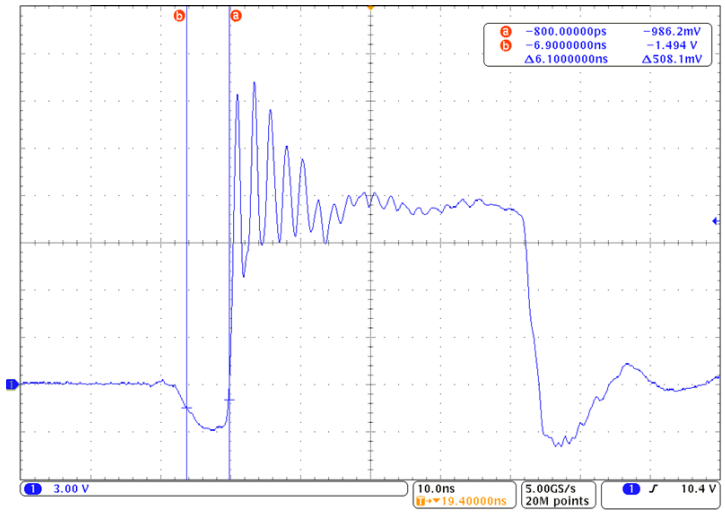
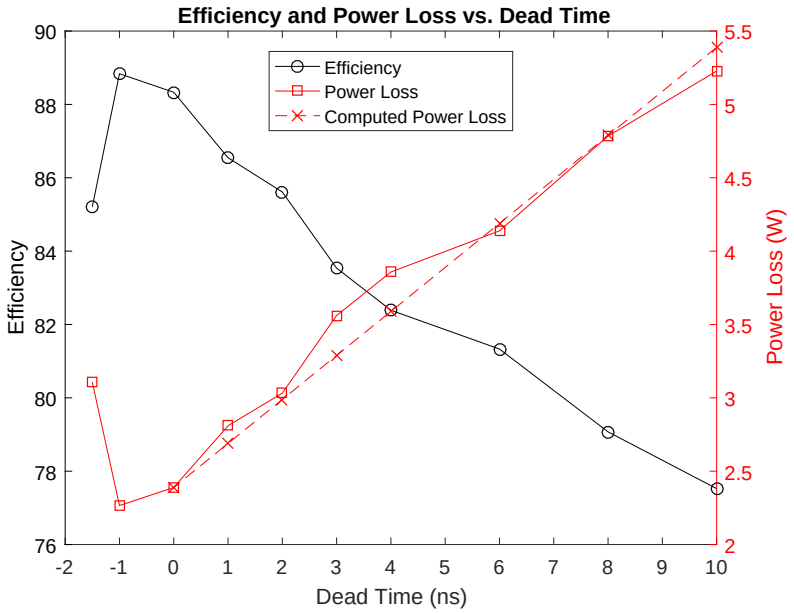


Figure 2. Switch Node Voltage Waveform Showing Measured Effective Dead Time of 6 ns



V_{IN} = 12 V, V_{OUT} = 1.8 V, I_L = 10 A, L_{IND} = 250 n

Figure 3. Effective Dead Time and Power Loss Versus Dead Time for a 12-V to 1.8-V Buck Converter

Figure 3 shows the measured efficiency and power loss versus the dead time. It also shows the modeled power loss according to Equation 3 with V_{dead}= 3 V, I_L= 10 A, and F_{SW}= 5 MHz with an additional factor added to equalize the losses at the dead time of 0 ns. The measured power loss matches the calculated loss very well. Data was also collected with small negative dead times. A small negative dead time has a beneficial effect on efficiency, but a shoot-through occurs very quickly soon after and efficiency degrades rapidly.

It is apparent that for many applications, minimizing the dead time is critical to achieve low power loss. If the dead time goes negative, however, cross conduction will occur with the associated loss in efficiency. Therefore, the dead time must be held to a small band without straying outside it.

2 Minimizing Dead Time

Achieving very low dead time on the bench with a single board is easy. For any given board and set of operating conditions, it is easy to adjust the dead time and achieve very low dead time losses. It is another matter entirely to maintain that low dead time across a wide range of operating conditions and across part-to-part variations in a production environment. Therefore whenever promotional materials claim very good dead time losses, users should question if those losses can be implemented in production.

Further complicating matters, one edge is soft-switched in most converters. To avoid hard switching and maintain a small effective dead time on this soft-switched edge, the dead time must be varied depending on load current. This must be done by the power supply controller and is out of the realm of this driver-centric discussion. Failing to do this could cause degraded efficiency, but will generally not cause shoot-through.

There are many different sources for dead-time variation in and around the driver which must be explored. Any factor which affects the propagation delay of the high and low side differently can cause dead time shifts. Some questions to consider when determining what dead time is sufficient for a production product include:

- What is the intrinsic dead-time variation performance of the driver itself?
- Does the high-side propagation delay vary with the high-side ground voltage?
- Does the high-side propagation delay vary with the bootstrap voltage?
- Does the propagation delay vary if it propagates at the same time as a common-mode transient?

Many of these questions cannot be answered in the driver data sheets, so these questions are addressed in the following sections.

2.1 Mismatch of the Driver Itself

The driver has an intrinsic propagation delay variation between the high and low side that manifests itself as a dead-time variation across parts, and this is usually specified on the data sheet. For drivers with separate high and low side inputs, it is important to look for the difference in propagation delays of the falling low-side to the rising high-side outputs or the falling high-side to rising low-side output. For drivers with a single input where the dead time is generated internally, the data sheet should specify what the variation of the output dead time will be when the commanded dead time is minimal (or zero). The two methods are roughly equivalent at measuring the performance of the driver; however the latter also includes the variation of the dead-time generation circuit in addition to the driver itself.

A non-zero constant value for the above parameters can be corrected; the user should be more concerned with part-to-part variation of the above parameters. Many drivers, however, are designed so the average of these parameters is zero. Therefore, unless the data sheet states otherwise, the data sheet values can be considered the part-to-part variation values.

The LMG1210 was carefully designed to minimize the part-to-part intrinsic variation of the propagation delay. Table 1 shows a comparison between the LMG1210 and LMG1205.

Table 1. Mismatch Parameters of Various Drivers From the Data Sheet

PART	(IID MODE) PROP. DELAY MISMATCH. (ns)	(PWM MODE) DEAD-TIME VARIATION (ns)
LMG1210	±3.4	–0.55/3.1
LMG1205	±8	N/A

The LMG1210 can work in both PWM mode and independent input mode (IID), so it specifies both numbers in the data sheet. It is optimized to work in PWM input mode with noticeably better specs than in IID mode.

2.2 Propagation Delay Variation With High-Side Ground

In the LMG1205 the delay through the level shifter varies with the HS pin voltage. This means that the dead time may shift depending on HS voltage at the moment the HI signal is propagating through the driver if this varies in an application. This effect is generally not measured in the data sheet. The intrinsic driver mismatch in the data sheet is usually specified when HS = 0 V, but in an application, this will not be the case. Because of the architecture of the level shifter, most of the variation occurs when the HS pin is within a few volts of the low-side ground.

Figure 4 shows the measured high-side propagation delay versus the HS pin voltage for the two parts. The LMG1210 is capacitively isolated so it has no variation, but the LMG1205 can vary up to ±3 ns. In many applications, however, this error will be a fixed error and may be corrected for.

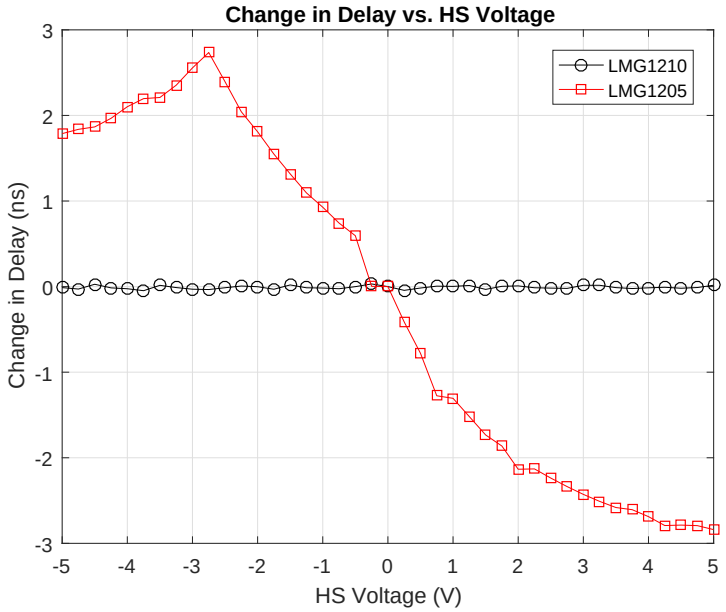


Figure 4. Change in Delay vs HS for the Two Parts

2.3 Propagation Delay Variation With Bootstrap Voltage

In an actual application, the bootstrap voltage may vary depending on the temperature, low-side pulse width, and low-side supply voltage which all affect the bootstrap charging path. Only the high-side propagation delay is affected by bootstrap voltage variations which cause a mismatch with the low side. The size of this effect depends on how much the bootstrap voltage varies over different operating conditions in the application and the effect this has on the driver. Figure 5 shows the measured high-side propagation delay versus the bootstrap voltage for the two parts. The LMG1210 was designed to minimize this delay variation, but it is nonetheless not immune from variation.

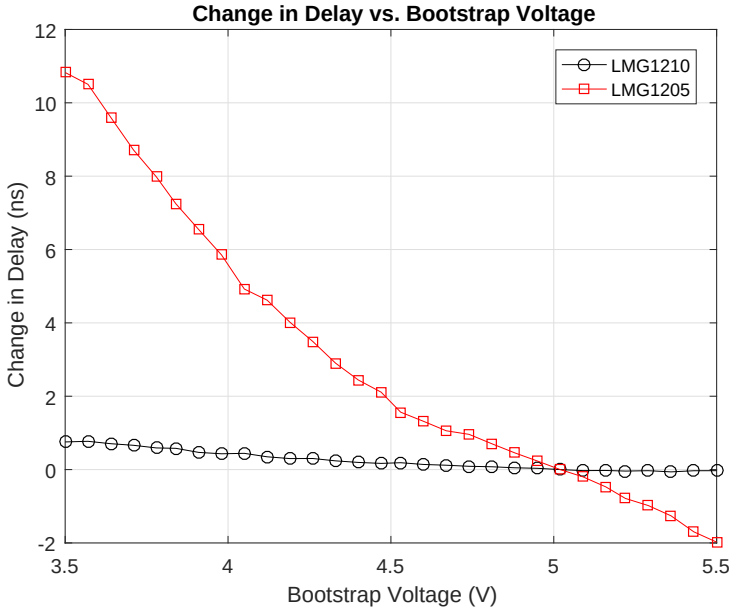


Figure 5. Change in Propagation Delay vs Bootstrap Voltage for the Two Devices

In most converters there will be some variation of the bootstrap voltage over temp and operating conditions, so this is a parameter which should be included when determining the necessary dead time in most applications.

2.4 Propagation Delay Variation During CMTI

The propagation delay of the high-side can be affected if the signal is propagating through the level shifter simultaneously with a switching transition of the HS node.

This effect is most commonly encountered in a boost-type converter where the current is flowing into the half-bridge. In this case, the high-side FET is soft-switched. The signal to turn on the high-side FET will be propagating through the level shifter at the same time that the HS voltage is driven high by the current through the inductor. If the current is reversed such as in a buck, this condition will only be encountered if the high-side on-time is less than the propagation delay of the part so that the signal to turn off the high-side FET is propagating through the level shifter at the same time the high-side FET is being turned on.

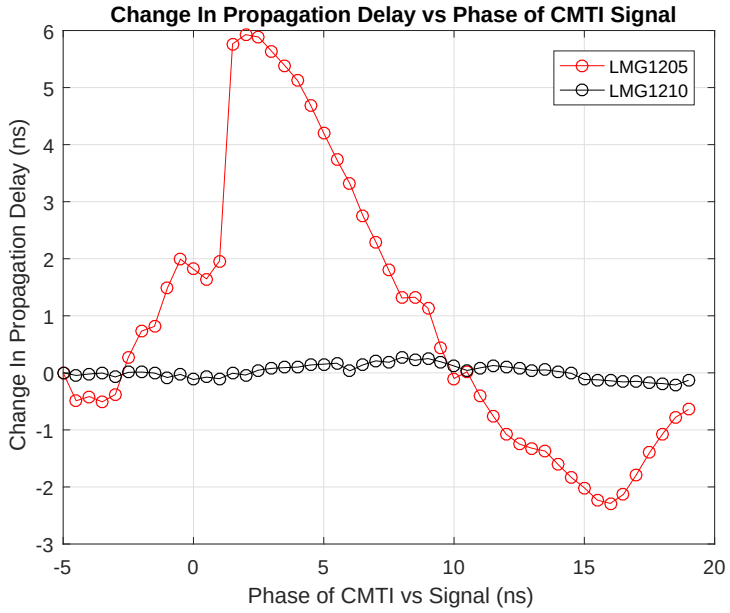


Figure 6. Change in Propagation Delay vs Phase of CMTI. CMTI = 30 V/ns, HS Rising

Figure 6 shows the propagation delay of the two parts versus the relative phase of the 30-V/ns CMTI pulse. The LMG1210 level shifter was carefully designed to minimize any variation during a common-mode transient so its delay stays almost completely constant and therefore does not add to the required dead time. The LMG1210 data sheet also shows graphs which show it does not vary even with faster CMTI levels.

The LMG1205 level shifter is affected by the CMTI by effectively *blanking* during sufficiently fast CMTI. Effectively, the level shifter will not propagate signals during a CMTI event, so if a signal edge happens during a CMTI transition, it must wait until after the CMTI slows enough to propagate the new signal. For this case, the duration of the CMTI event is about 3.5 ns, and that is the cause of the jump in propagation time around the 2-ns phase condition in Figure 6. At 1.5 ns, the signal propagated before the main CMTI edge, but at 3 ns, the signal waited to propagate until after the CMTI edge was complete. Paradoxically, this means that a faster CMTI edge would result in less propagation time distortion because the CMTI edge would complete faster, and slower CMTI produces more distortion until you get below a threshold where the signal can propagate during the CMTI.

3 Dead Time Example

To determine the usable dead time for an application, one first must determine which effects will be present on which edges. As an example, consider a boost converter. Table 2 gives a summary of the expected variation for each of the parameters listed above and how much that amount of variation is expected to cause the dead time to shift. A number of assumptions were made in the table: the bootstrap voltage was assumed to vary from 4 to 4.5 V, though that would depend on the diode chosen and the range of low-side on time durations expected, and the CMTI during the low-off to high-on transition would depend on the load current, but was assumed to vary from 10 to 100 V/ns. As can be seen for applications requiring tight dead time control, the LMG1210 is desired. For the low-off to high-on case—that is the soft-switching edge—it is acceptable to use a smaller dead time than stated because the cost of using a negative dead time results in limited hard-switching will have very minimal effects on efficiency, while negative dead time is much more catastrophic for the hard-switched edge.

Table 2. Breakdown of Effects for Each Edge of a Boost Converter

EFFECT	EDGE					
	HIGH-OFF TO LOW-ON (HARD-SWITCHING EDGE)			LOW-OFF TO HIGH-ON (SOFT-SWITCHING EDGE)		
	PARAMETER VARIATION	LMG1210 VAR. (ns)	LMG1205 VAR. (ns)	PARAMETER VARIATION	LMG1210 VAR. (ns)	LMG1205 VAR. (ns)
Variation of HS	None (Vin)	0	0	Minimal	0	0
Variation of Vbst	4 V to 4.5V	0.3	3.6	4V to 4.5V	0.3	3.6
Variation of CMTI	None	0	0	10-100V/ns	0.2	5
Intrinsic Driver Variation		3	8		3	8
Total variation in Dead time		**3.3**	**11.6**		**3.5**	**16.6**

4 Conclusion

This report demonstrates that, for some power converters, minimizing dead time is crucial to maximizing efficiency. Furthermore, there are a number of parameters in drivers which are rarely specified in the data sheet but are nonetheless important when minimizing dead time. Measurements of these parameters presented in this paper show the LMG1210 is designed for applications requiring tight dead time control.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2018) to A Revision	Page
• Changed the LMG1210 specs in the *Mismatch Parameters of Various Drivers From the Data Sheet* table	4
• Changed the LMG1210 intrinsic driver variation and total variation in dead time specs in the *Breakdown of Effects for Each Edge of a Boost Converter* table	8

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