Application Report
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Analysis and Design of Input Filter for DC-DC Circuit

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ABSTRACT

When designing DC-DC circuits, it is common to add the input filter circuit before the power stage. An LC filter is one of most frequently used input filter circuit. However, if a design is not optimal, input filter circuit may cause large output noise instead of suppressing the noise, and may even cause loop stability problems. This application report analyzes the influence of the input filter on the DC-DC control loop transfer function, and the influence of a closed loop on the input filter, explains why input filter causes unexpected problem, and suggests how to eliminate the side effect of the input filter.

Contents

Trademarks

1 Function of Input Filter Circuit

Input filters are widely used in power design. They have two main purposes: one is to suppress the noise and surge from the front stage power supply, another is to decrease the interference signal at switching frequency and its harmonic frequency to go back to the power supply and interfere other devices which uses the power supply. The input filter design is very important to pass the electromagnetic compatibility (EMC) test.

Simple LC passive filters are among the common filters for DC-DC converters. They can attenuate the high frequency noise from the power supply and can also suppress the switching noise to go back to the power supply.

If LC filter is not well damped, the frequency response will peak near resonant frequency, which means the LC actually is amplifying the noise signal. Apart from the amplification, sometimes, LC filter design also has effect on the control loop of the DC-DC converter, some poor LC filter will decrease the phase margin and degrade the transient response performance, some even cause stability problem. This is discussed in Section 2 based on a buck converter.

2 Loop Gain of Buck With Input LC Filter

2.1 Open Loop Small Signal Model

Figure 1 is a traditional synchronous buck converter. During the on and off status of one switching cycle, FET shows non-linear characteristic. According to the average model, the small signal of input current and switching node voltage can be calculated as Equation 1, and the open loop small signal model of the buck can be expressed as Figure 2.

$$\hat{i}_{in} = I_L \hat{d} + D\hat{i}_L$$
$$\hat{u}_{CP} = U_{in}\hat{d} + D\hat{u}_{in} \quad (1)$$

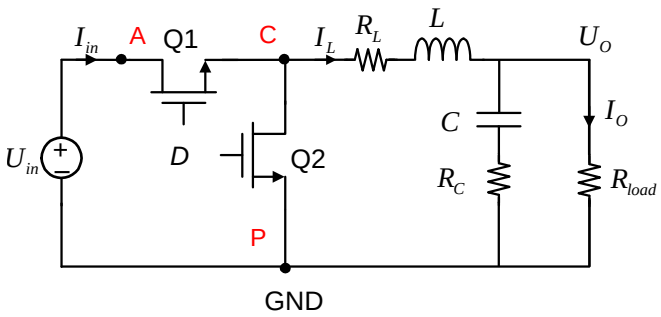

Figure 1. Buck Circuit Topology

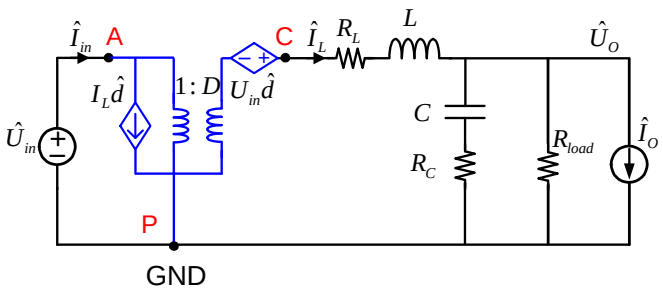

Figure 2. Buck Circuit Small Signal Model

It is normal that input voltage and output current may change, which influences the output voltage and inductor current. When adopting closed loop control, duty cycle may change to maintain the output voltage, at the same time, the inductor current will change. So we can build the open loop control block diagram as Figure 3.

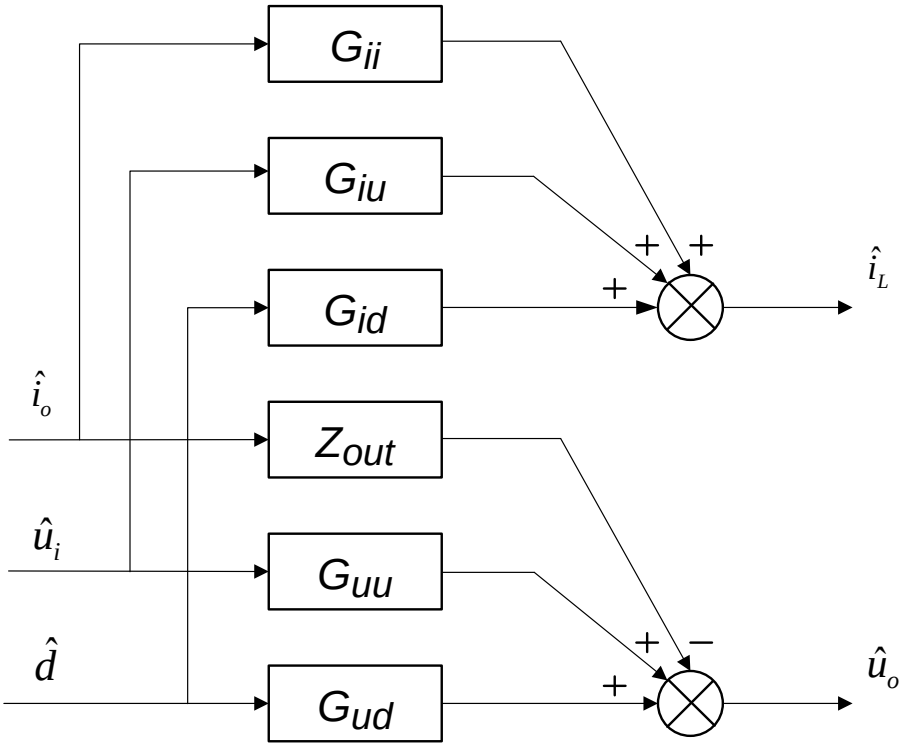

Figure 3. Open-Loop Buck Controller Block Diagram

For simplicity, ignore the inductor DCR and output capacitor ESR when calculated the transfer function. Then the six transfer functions in Figure 3 are calculated as Equation 2 to Equation 7. All the six transfer functions will be used in following sections, especially at *Section 3.1*.

$$G_{ud}(s)=\frac{\hat{u}_o(s)}{\hat{d}(s)}\Big|_{\hat{u}_i(s),\hat{i}_o(s)}=\frac{U_i}{LCs^2+\frac{L}{R}s+1} \tag{2}$$

$$G_{uu}(s)=\frac{\hat{u}_o(s)}{\hat{u}_i(s)}\Big|_{\hat{d}(s),\hat{i}_o(s)}=\frac{D}{LCs^2+\frac{L}{R}s+1} \tag{3}$$

$$Z_{out}(s)=\frac{\hat{u}_o(s)}{\hat{i}_o(s)}\Big|_{\hat{d}(s),\hat{u}_i(s)}=\frac{Ls}{LCs^2+\frac{L}{R}s+1} \tag{4}$$

$$G_{id}(s)=\frac{\hat{i}_L(s)}{\hat{d}(s)}\Big|_{\hat{u}_i(s),\hat{i}_o(s)}=\frac{\frac{U_{in}}{R}(1+RCs)}{LCs^2+\frac{L}{R}s+1} \tag{5}$$

$$G_{iu}(s)=\frac{\hat{i}_L(s)}{\hat{u}_i(s)}\Big|_{\hat{d}(s),\hat{i}_o(s)}=\frac{\frac{D}{R}(1+RCs)}{LCs^2+\frac{L}{R}s+1} \tag{6}$$

$$G_{ii}(s)=\frac{\hat{i}_L(s)}{\hat{i}_o(s)}\Big|_{\hat{d}(s),\hat{u}_i(s)}=\frac{1}{LCs^2+\frac{L}{R}s+1} \tag{7}$$

Input impedance is a key parameter in this paper, which is not obvious to drawn in Figure 3; nevertheless, open loop input impedance can be defined and calculated as Equation 8 using a similar method.

$$Z_{in}(s)=\frac{\hat{u}_i(s)}{\hat{i}_{in}(s)}\Big|_{\hat{d}(s),\hat{i}_o(s)}=\frac{\hat{u}_i(s)}{\hat{i}_L(s)\big/D}\Big|_{\hat{d}(s),\hat{i}_o(s)}=\frac{R}{D^2}\frac{LCs^2+\frac{L}{R}s+1}{(1+RCs)} \tag{8}$$

2.2 Closed Loop of the Buck Converter

For a buck converter, it is normally desired that the output voltage is constant. Feedback topology is used to close the control loop, it automatically changes the duty cycle to decrease or even eliminate the influence from the input voltage or output current. A typical closed loop of VMC buck converter is as Figure 4. *H* is the feedback resistor network, G_c represents the error amplifier, and G_m is for the modulator gain.

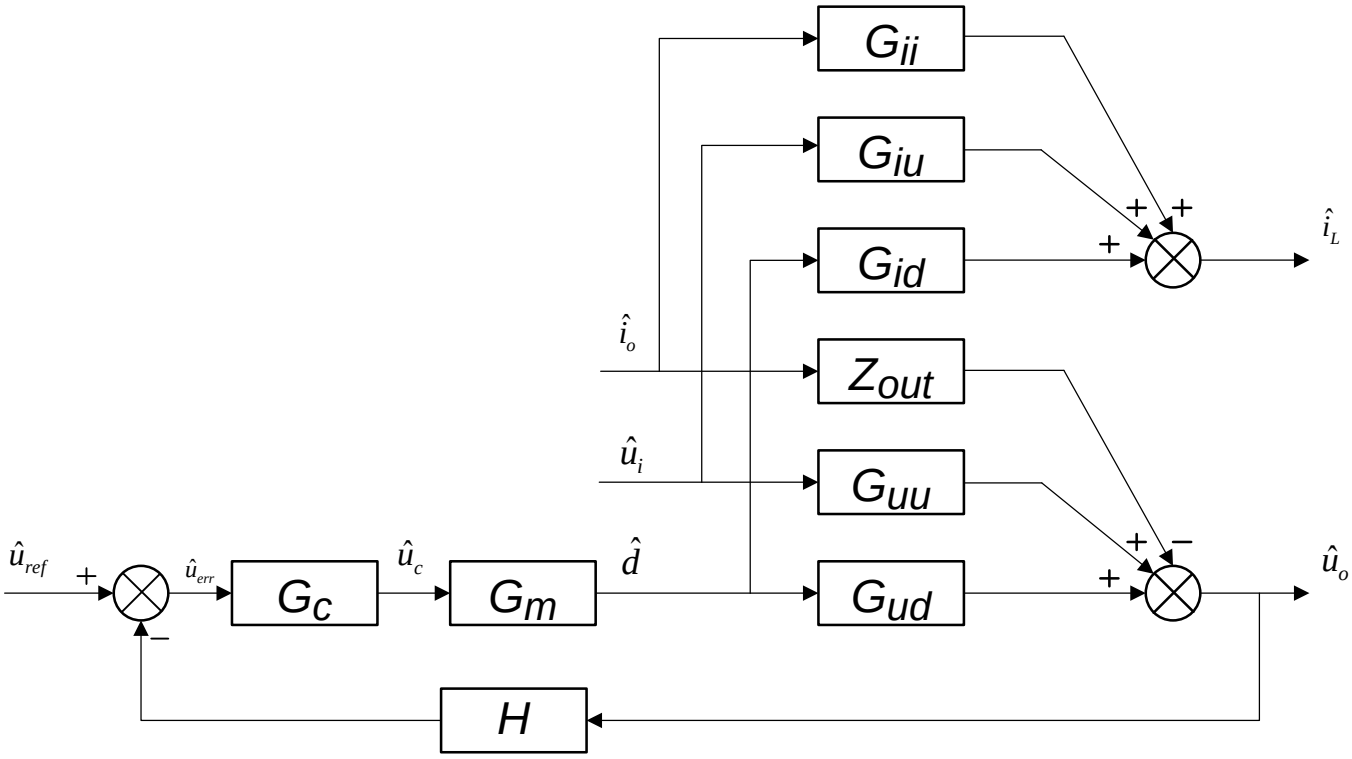

Figure 4. VMC Closed Loop Buck Controller Block Diagram

By adopting closed loop topology, loop gain is defined as the product of the gains in feedforward path and feedback path in the closed loop as Equation 9. Take the VMC plus type III compensator as example, the frequency response of T_{loop} can be plotted as Figure 5.

$$T_{loop}(s) = HG_cG_mG_{ud} \tag{9}$$

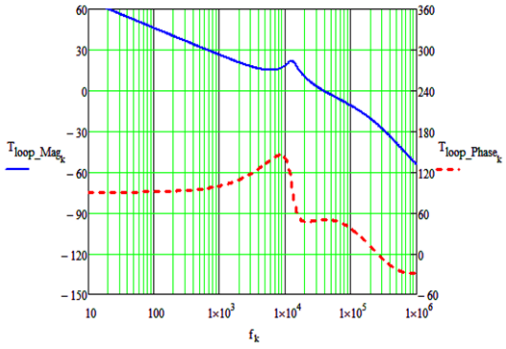

Figure 5. Loop Gain Frequency Response

Under the effect of the closed loop, the transfer function from the perturbation to the output voltage is multiplied by a factor *1 /(1 + T(s))*. The closed loop audio susceptibility and output impedance can be expressed as Equation 10 and Equation 11. And the open loop and closed loop frequency response can be drawn as Figure 6 and Figure 7, it can be seen from the picture, low frequency perturbation can be well suppressed by closing the control loop.

$$G_{uu\_CL}(s) = \frac{G_{uu}(s)}{1+T_{loop}(s)} = \frac{D}{(1+T_{loop}(s))\cdot(LCs^2+\frac{L}{R}s+1)} \tag{10}$$

$$Z_{out\_CL}(s) = \frac{Z_{out}(s)}{1+T_{loop}(s)} = \frac{Ls}{(1+T_{loop}(s))\cdot(LCs^2+\frac{L}{R}s+1)} \tag{11}$$

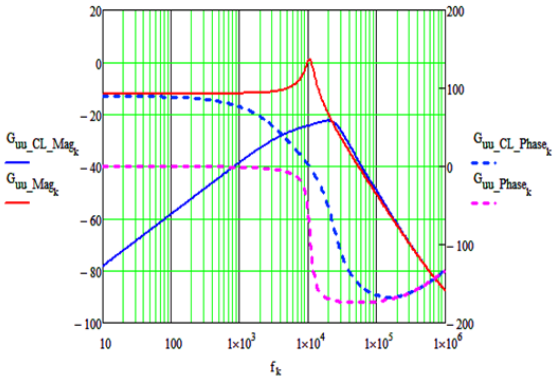

Figure 6. Closed Loop Audio Susceptibility

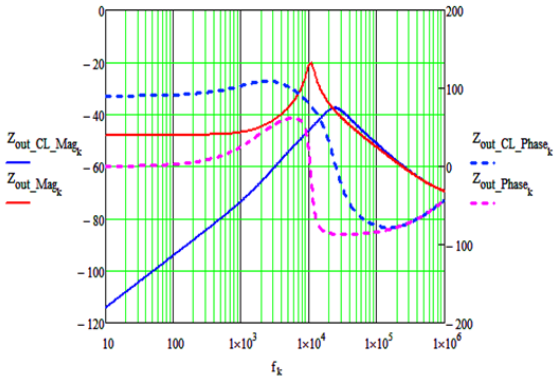

Figure 7. Closed Loop Output Impedance

2.3 Loop Gain With Input LC Filter

Even though closed loop suppresses the audio susceptibility a lot at low frequency, but it doesn't change too much for the middle and high frequency. The designer should also consider the interference from the DC-DC back to the power bus. Thus, a LC filter is often used for DC-DC circuit to pass EMI test.

When adopting LC filter to solve an EMI problem, another problem may arise, when the load transient performance changes, audio stability becomes worse at some frequency, some even cause the stability problem. These problems can be explained as that input filter circuit modifies the transfer function of the buck converter, including the control to output transfer function G_{ud}, which then changes the loop gain, phase margin, etc.

According to Middlebrook's extra element theorem, adding the filter circuit to the buck converter adds a correction factor to the original transfer function.

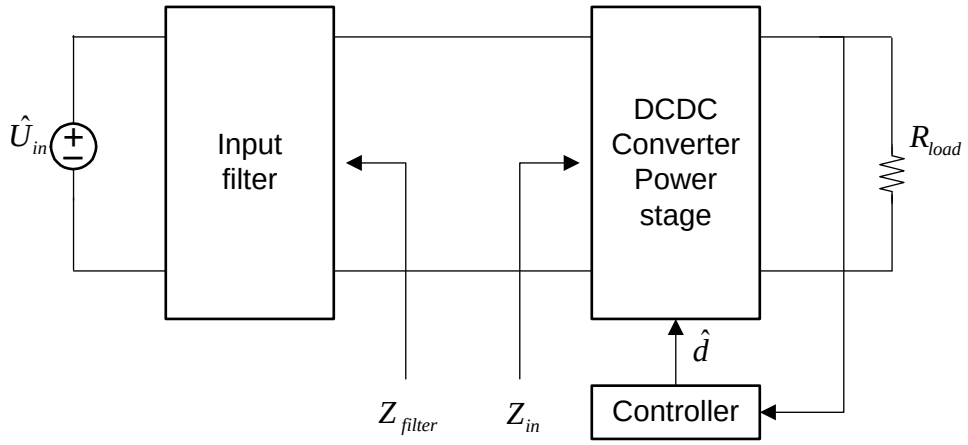

Figure 8. Buck Control Block Diagram With LC Filter

$$G_{ud\_f}(s) = \left(G_{ud}(s)\big|_{Z_{filter}(s)=0}\right)\frac{\left(1+Z_{filter}(s)/Z_N(s)\right)}{\left(1+Z_{filter}(s)/Z_D(s)\right)}$$

where

- $G_{ud}(s)\big|_{Z_{filter}(s)=0}$ is the original transfer function before addition of input filter. (12)

$Z_{filter}(s) = \left(sL_f + R_{DCR}\right) \| \left(\frac{1}{sC_f} + R_{ESR}\right)$ is the output impedance of the LC filter, looking from DC-DC side.

$Z_D(s) = Z_{in}(s)\big|_{\hat{d}(s)=0} = \frac{R}{D^2}\frac{LCs^2 + \frac{L}{R}s + 1}{1 + RCs}$ is the converter input impedance, with $\hat{d}(s)$ set to zero.

$Z_N(s) = Z_{in}(s)\big|_{\hat{u}_o(s)\to 0} = -\frac{R}{D^2}$ is the converter input impedance, with the output nulled to zero.

Using a poorly designed LC filter as an example, after addition of correct factor, the new loop gain transfer function can be calculated from Equation 13. The frequency response can be calculated as Figure 9, simulated as Figure 10 using Simplis, the two waveforms show good consistency of the LC resonant frequency.

$$T_{loop}(s) = HG_cG_mG_{ud\_f} \quad (13)$$

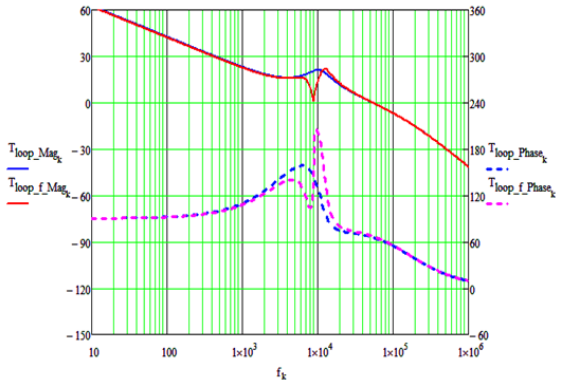

Figure 9. Mathcad Calculation Loop Gain

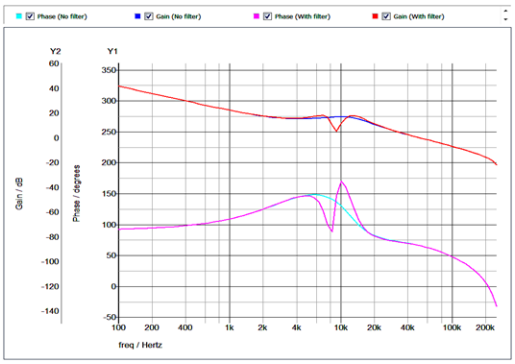

Figure 10. Simplis Simulation Loop Gain

Comparing the new frequency response waveform with original one, it can be easily found that the LC filter brings a dip to the original frequency response, the magnitude-frequency curve drops to close to 0 db in this case, and the phase-frequency curve also drops near that point, which makes the loop gain performance worse.

3 Closed-Loop Input Impedance

3.1 Closed-Loop Input Impedance Calculation

The open loop input impedance is defined as Equation 8, after applying the closed loop, the closed loop changes the input impedance, because when input voltage change, duty cycle changes to maintain the output voltage, which also brings additional change to the input current.

To calculate the closed loop input impedance, combined with Equation 1, the block diagram can be draw as Figure 11. By changing the feedback and feed-forward position, a simplified block diagram can be drawn as in Figure 12. By comparing Equation 2 through Equation 8, it can be calculated that

$$\frac{G_{uu}}{G_{ud}} = \frac{D}{U_I}, DG_{iu} = \frac{1}{Z_{in}}, G_{uu}G_{id} = \frac{G_{ud}}{DZ_{in}} \tag{14}$$

combined with Figure 12, a single block from input voltage to input current can be expressed as Figure 13.

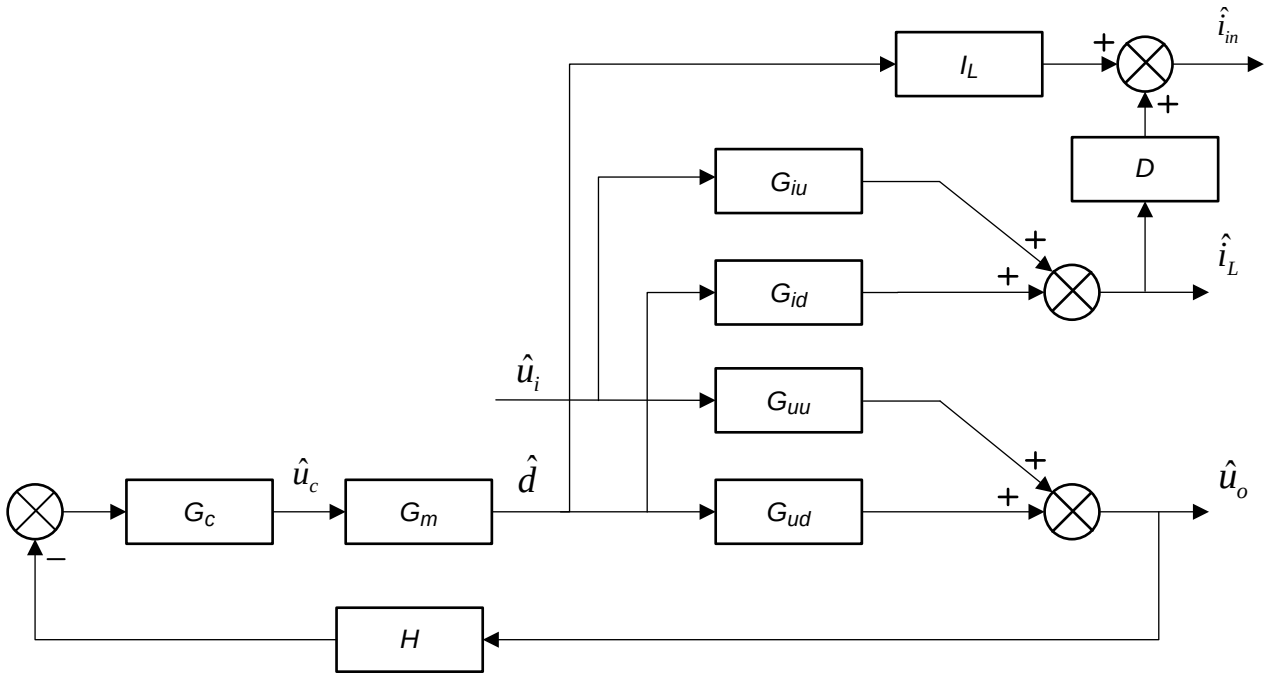

Figure 11. Closed Loop Input Impedance Calculation Block Diagram

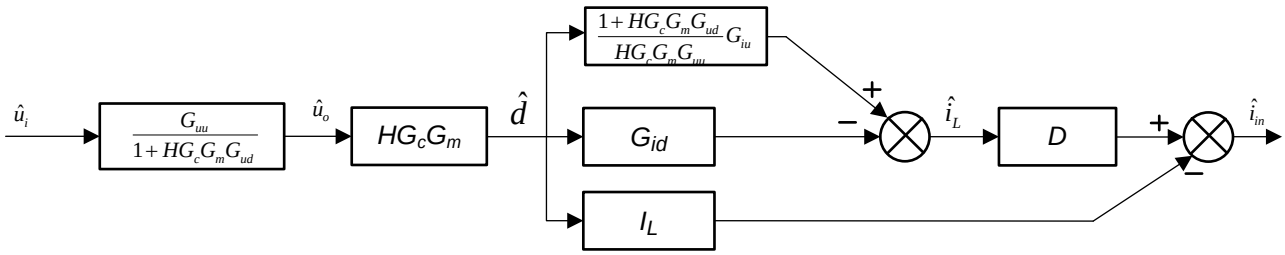

Figure 12. Simplified Closed Loop Input Impedance Calculation Block Diagram

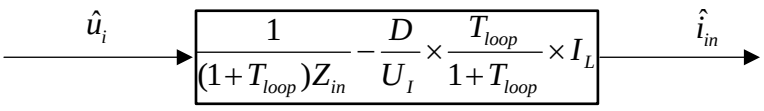

Figure 13. Single Block From Input Voltage to Input Current

So the closed loop input impedance can be calculated as Equation 15:

$$Z_{in\_CL}(s) = \frac{\hat{u}_{i\_CL}(s)}{\hat{i}_{in\_CL}(s)} = Z_{in} \frac{(1+T_{loop})}{1-\frac{DI_L T_{loop} Z_{in}}{U_I}} \quad (15)$$

The frequency response of closed loop input impedance is plotted as Figure 14 in comparison with open loop input impedance. It can be seen that closed loop impedance and open loop impedance shows similar characteristic when frequency goes high; during middle frequency, the closed loop makes the impedance amplitude larger, which means that same input voltage change will brings smaller input current variation. At low frequency, they show same amplitude characteristic, but closed loop makes the phase characteristic changes, the phase at low frequency is close to –180°, it functions as negative incremental input impedance. For example, the output voltage and current are fixed, if input voltage increases, the input current decreases, it looks like negative resistor.

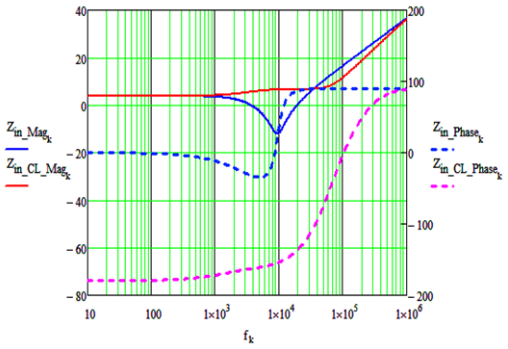

Figure 14. Open-Loop and Closed-Loop Input Impedance

3.2 Influence of the Input Impedance on Input Filter

For a DC-DC circuit, if the input filter is utilized, this negative incremental input impedance also has some influence on the input filter circuit. From Figure 14 it can also be seen, when loop is open, the input impedance is very low at middle frequency, and the low impedance brings more damping to the LC filter circuit, but when adopting closed loop, the impedance become negative, this is decreasing the damping to the LC filter. Define the transfer function from input voltage to the output of the LC filter as $G_{fv}(s)$. Use Mathcad to draw the frequency response of $G_{fv}(s)$ as Figure 15. It can be seen, when loop is open, the peak value of the amplitude is very small, much less than 20 dB. But when adopting the closed loop, the peak value is close to 20 dB, which means very small damping of the LC circuit.

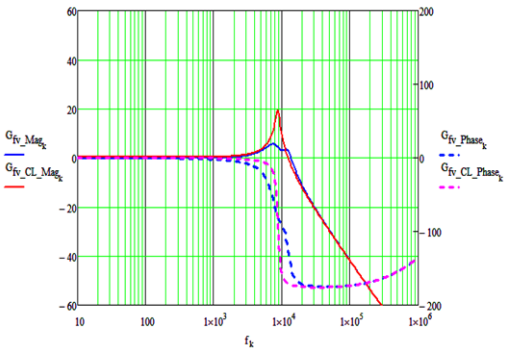

Figure 15. Input Filter Frequency Response With Closed Loop

When the damping ratio is too small, normally there will be large amplitude oscillation in time-domain waveform. Figure 16 is the test result based on the TPS40040EVM by adding a 3.5-µH inductor as filter circuit. Taking the de-rating of the inductor and MLCC into consideration, a Simplis simulation result is plotted as Figure 17, which shows good consistence with the EVM test result.

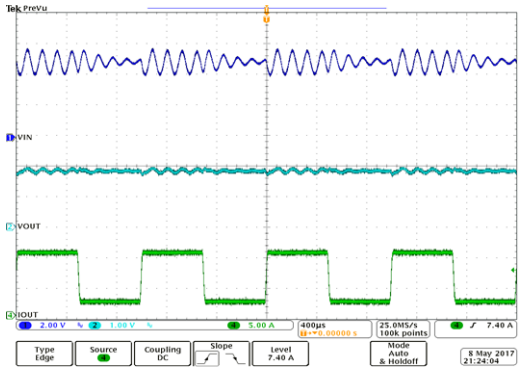

Figure 16. Load Transient Test on EVM

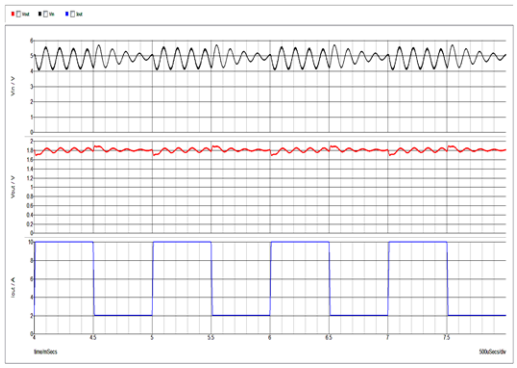

Figure 17. Load Transient Test of Simplis Simulation

4 Designing the Input Filter Circuit

4.1 Stability Criteria With Input Filter

From above load transient test, it can be seen that when the load is heavy, the oscillation is much larger than light load, because larger load current brings smaller negative incremental input impedance, which means much smaller damping ratio, or even brings stability problem. Capacitor ESR, Inductor DCR and power source output impedance R_O are also very critical for stability, because they also bring damping to the LC filter. To analyze the stability of a buck circuit with an LC filter, use a pure resistor $-R_{in} = Z_{in}(s)\|_{s=0}$ as input impedance, then equivalent circuit is Figure 18.

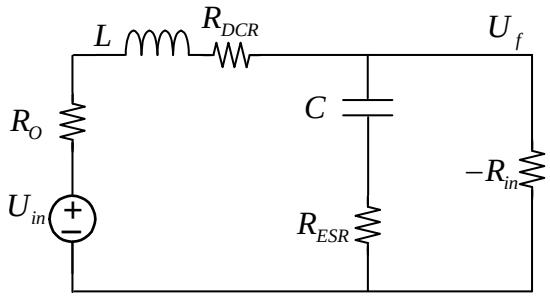

Figure 18. Equivalent Circuit for Stability Analysis

R_{ESR} is normally much smaller than $-R_{in}$, so the paralleled impedance of the capacitor, and the input impedance can be expressed as Equation 16 and $G_{fv}(s)$ can be expressed as Equation 17.

$$-R_{in} // \left(\frac{1}{sC} + R_{ESR}\right) \approx \frac{-R_{in}\left(1 + sCR_{ESR}\right)}{1 - sCR_{ESR}} \tag{16}$$

$$G_{fv}(s) = \frac{\hat{u}_f(s)}{\hat{u}_{in}(s)} = \frac{R_{in}\left(1 + sCR_{ESR}\right)}{s^2 LCR_{in} + s\left[R_{in}C\left(R_O + R_{DCR} + R_{ESR}\right) - L\right] + \left(R_{in} - R_O - R_{DCR}\right)} \tag{17}$$

For stability, there should be no positive pole for $G_{fv}(S)$, then

$$LCR_{in} > 0$$

$$R_{in}C\left(R_O + R_{DCR} + R_{ESR}\right) - L > 0$$

$$R_{in} - R_O - R_{DCR} > 0 \tag{18}$$

So the stability requirement is as Equation 19 and Equation 20, and the damping ratio is as Equation 21.

$$R_{in} > \frac{L}{C\left(R_O + R_{DCR} + R_{ESR}\right)} \tag{19}$$

$$R_{in} > R_O + R_{DCR} \tag{20}$$

$$\zeta = \frac{\left[R_{in}C\left(R_O + R_{DCR} + R_{ESR}\right) - L\right]}{2\sqrt{LCR_{in} \times (R_{in} - R_O - R_{DCR})}} \tag{21}$$

Normally it is not very hard to meet Equation 19 and Equation 20. But in some cases, even though meets Equation 19 and Equation 20, if R_{in} is too small, according to Equation 21, the damping ratio of the system is also small, which brings large oscillation. Normally this happens with the condition of large output current and large duty cycle, and the input cap is using MLCC which has smaller ESR. That's why in Figure 9 and Figure 10, when load is heavy, the oscillation amplitude is large.

4.2 Damping the Input Filter

If oscillation happens after adding a LC filter circuit, normally decreasing the inductor value or increasing the capacitor value may increase the damping ratio and remove the oscillation, but this will also change the target LC filter characteristic. Sometimes replacing MLCC with electrolytic capacitor may also solve the problem. But the large ESR of the electrolytic capacitor will also bring large input voltage ripple when the MOSFET is switching. Another way is to add an additional damping circuit after the LC filter circuit like Figure 19. The resistor is to damp the filter, and because we only want to damp the middle frequency amplitude peak value, there is no need to use a pure resistor as the damping circuit. Rather, a series capacitor C_d can be used to avoid large power dissipation on the resistor. A capacitor much larger than C is required for the LC filter to detect R_d at the middle frequency, $C_d \geq 4C$ may be an acceptable value, and there is no need to use good-quality capacitor like C to saving cost.

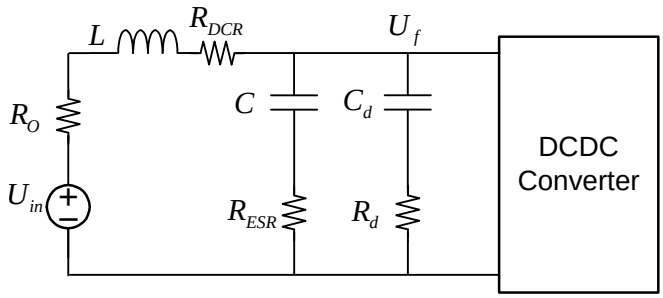

Figure 19. LC Filter With Damping Circuit

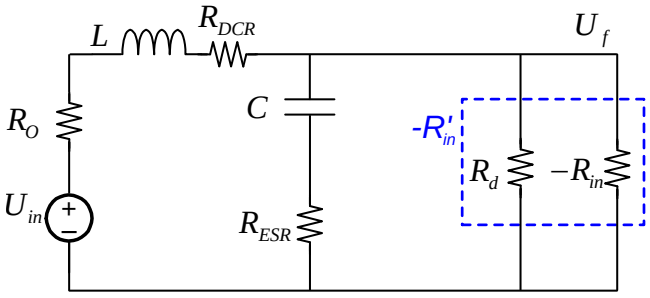

Figure 20. Equivalent Circuit at Middle Frequency

By applying the damping circuit, the approximate circuit at middle frequency is as Figure 20, the equivalent input impedance is shown in Equation 22: by adding the damping circuit, the absolute value of the equivalent input impedance value will increase, which increases the damping ratio of the LC filter.

$$-R_{in}^{'} = \frac{(-R_{in}) \cdot R_d}{-R_{in} + R_d} = -R_{in}\left(\frac{1}{1 - R_d / R_{in}}\right) \tag{22}$$

By adding additional damping circuit, EVM test result and the Simplis simulation result are as Figure 21 and Figure 22, which shows good consistency.

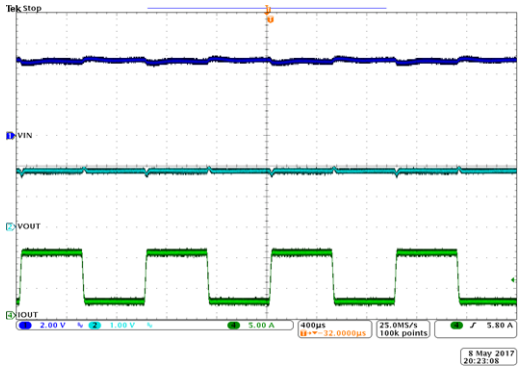

Figure 21. Load Transient Test on EVM

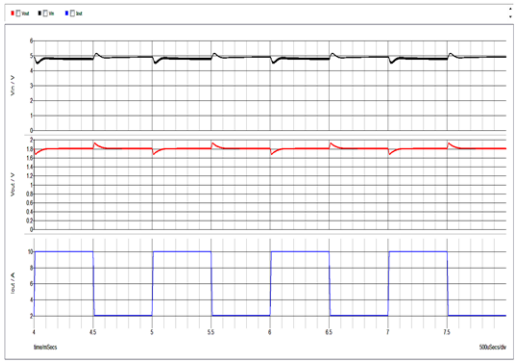

Figure 22. Load Transient Test of Simplis Simulation

5 Conclusion

An LC filter is widely used to optimize the EMC during DC-DC design, but improper design of the LC filter may cause the stability problem. This paper analyzes the influence of the input filter on the closed-loop gain, also explains how the closed loop brings the negative incremental input impedance and influence the LC filter. At the end, this paper describes stability criteria for LC filter design and also suggests some methods to solve oscillation problem when adopting LC filter.

6 References

1. R.D. Middlebrook, “Input filter considerations, in design and application of switching regulators” 1976 IEEE
2. Texas Instruments, *Input Filter Design for Switching Power Supplies* application note
3. Texas Instruments, *Low Pin Count, Low VIN (2.5V to 5.5V Synchronous Buck DC-to-DC Controller* TPS40040/1 data sheet
4. Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DCDC Converters* application report
5. R. Ahmadi, D. Paschedag, and M. Ferdowsi, “Closed-loop input and output impedances of DC-DC switching converters operating in voltage and current mode control,” *Proc. IECON ’10*, 2010, pp. 2311–2316.
6. R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd ed. New York: Kluwer, 2001.
7. Marian K. Kazimierczuk, Pulse Width Modulated DC-DC Power Converters, 2nd ed. Ohio: Wiley, 2016.

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