Application Report
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Applying External Phase Control Circuit for UCC28063

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ABSTRACT

Most power supplies are designed to focus on higher efficiency rating value at light-load operating conditions. Operating in phase mode, this circuit impacts the efficiency rating level for the PFC control circuit block. This document describes how to use an external phase control circuit to improve efficiency for the UCC28063 power factor correction (PFC) controller at light-load conditions.

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Trademarks

1 Introduction

With the advantages of low audible noise, high efficiency, low ripple, and good electromagnetic interference (EMI) performance, the UCC28063 interleaved PFC controller is designed for end equipment and display applications in particular. In addition, most customers want higher efficiency in normal load conditions and light-load conditions. The UCC28063 has single- and dual-phase control, using the PHB pin. In some cases, however, the internal phase control is not accurate. In these cases, more suitable methods are necessary.

2 Normal Theory of Phase Control UCC28063 Operation

Under light-load conditions, switching losses may dominate over conduction losses, and efficiency may be improved if one phase (channel) is turned off. At a certain power level, the reduction of switching losses is greater than the increase in conduction losses. Turning off one phase at light load can help meet light-load efficiency standards. This process is one of the major benefits of interleaved PFC, and especially valuable for meeting more than 80 design requirements. The PHB input can be used to force the UCC28063 to operate in single-phase mode. When PHB is driven below 0.8 V, channel B stops switching, and channel A automatically doubles to compensate. The device resumes dual-phase mode when PHB is raised above 1 V. For customized phase management, an external circuit can detect the conditions for switching to single-phase operation, and drive PHB accordingly. To operate continuously in two-phase mode (normal mode) when phase management is not desired, connect PHB to VREF.

Table 1. Phase With UCC28063 Modulator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_T On-time factor, phases A and B	VSENSE = 5.8 V	3.6	4	4.4	µs/V
K_T On-time factor, single phase, A	VSENSE = 5.8 V, PHB = 0 V	7.2	8	8.9	
Phase B to phase A on-time matching error	VSENSE = 5.8 V		±2%	±6%	
V_{PHBF} PHB threshold failing, to single phase operation	To GDB output shutdown, VINAC = 1.5 V	0.7	0.8	0.9	V
V_{PHBR} PHB threshold failing, to two phase operation	To GDB output running, VINAC = 1.5 V	0.9	0.1	1.1	

3 Theory of Automatic Phase Control Operation

Phase B may be shed through user control, or set up as an automatic light-load efficiency management feature. When the voltage applied to the PHB pin is below the VPHBF threshold, the Phase B and the phase fail detector are disabled. The commanded on-time for Phase A is doubled to minimize the output voltage transient, which would otherwise occur. Alternatively, PHB may be tied to the COMP pin for automatic phase shedding at light load.

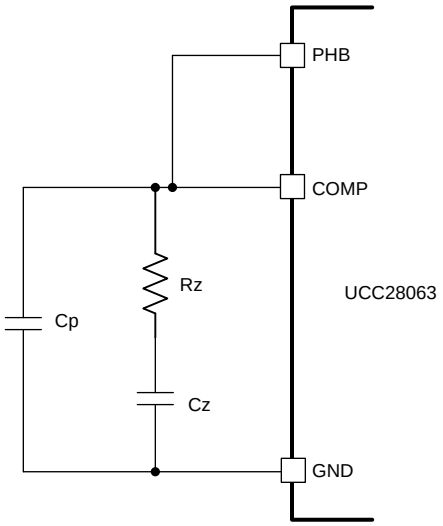

Figure 1. Original Automatic Phase Control Circuit With the UCC28063

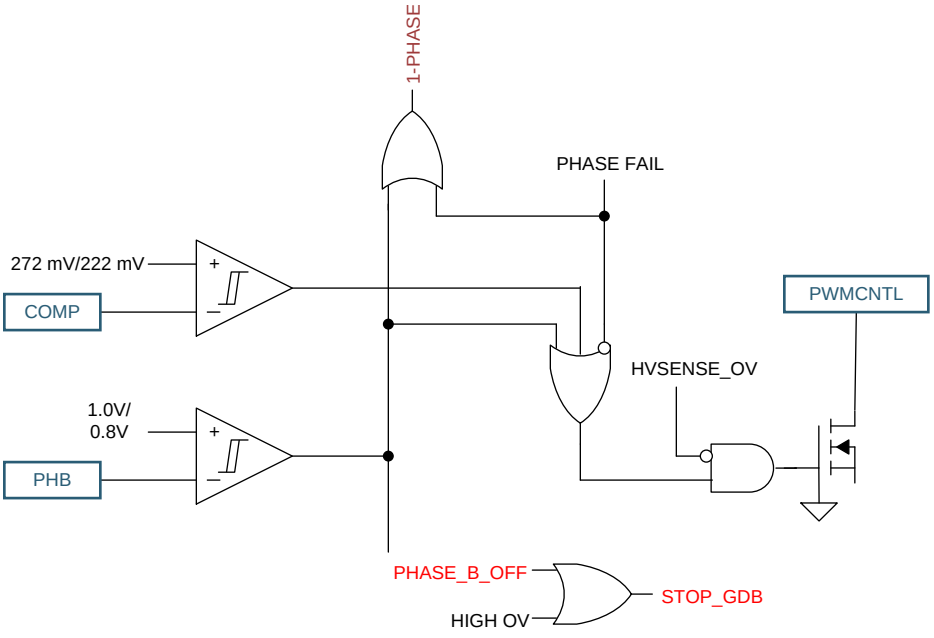

Figure 2. Internal Block of Phase Control With the UCC28063

4 Phase Control Operation

4.1 External Phase Mode Control Circuit of the UCC28063

Figure 3 shows an accurate phase-mode control of the PFC converter; adjust the phase control level using the external circuit at light-load conditions.

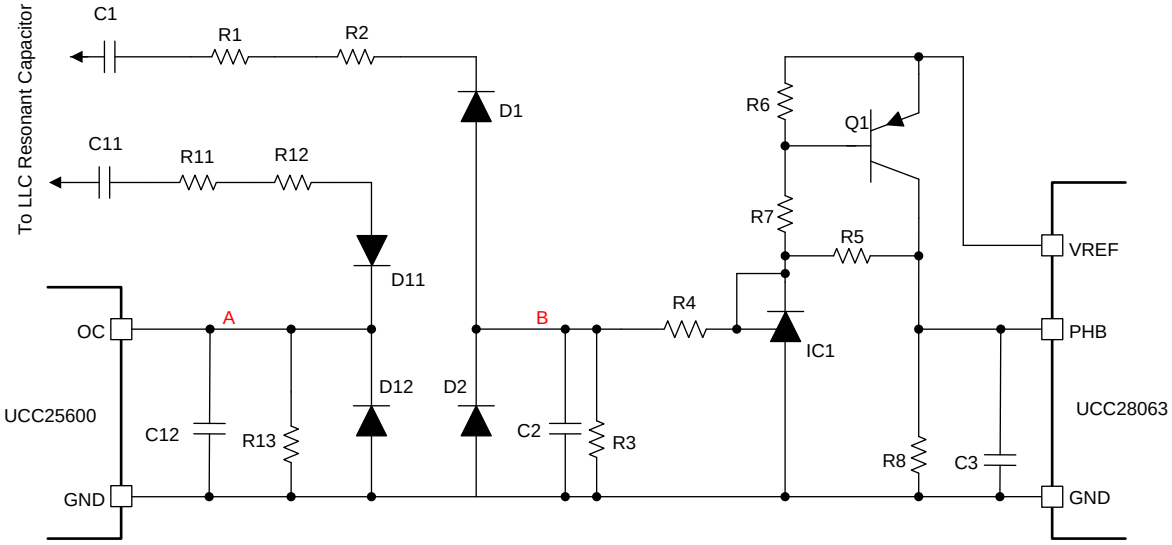

Figure 3. External Phase Control Circuit With UCC28063 and UCC25600

4.2 Detailed Operation for the External Phase Mode Control Circuit of the UCC28063

The original current-sensing network feeds into the LLC (C11, R11, R12, D11, D12, R13, and C12). A second current-sensing network feeds into the TL431 (C1, R1, R2, D1, D2, C2, and R3). This second network generates a higher voltage than the first, because R3 >> R13. If the LLC current is high enough to generate more than 2.5 V across R3, then the TL431 turns on, and its cathode pulls low; this turns Q1 on and pulls the PHB pin high.

The UCC28063 operates in two phase modes if the PHB pin is high. As the LLC current reduces, the voltage across R3 also reduces. If the current reduces enough, the voltage across R3 will reduce below 2.5 V, the TL431 turns off, and its cathode current falls to zero. This turns Q1 off; PHB is then pulled low by R8. C3 provides noise filtering. Adding R5 and R4 provides some additional hysteresis in the operation of the TL431. This hysteresis increases the separation between the turn-on current and the turn-off current. For a more accurate threshold level, use a 2.5-V TL431 instead of a 1.25-V TL431.

The level of hysteresis can be changed by increasing or decreasing the value of R5. Increasing R5 reduces the level of hysteresis. R5 and R4 form a load in parallel with R3, thus the value of R5 + R4 should be kept high to avoid loading the signal level across R3. The voltage at the reference input to the TL431 is not clamped in this circuit; current into the TL431 reference is limited by R4. The absolute maximum rating for this pin is 10 mA, which would require approximately 75 V across R3; however, this circuit will not reach that voltage.

4.3 Test Results for the External Phase Mode Control Circuit of the UCC28063

Figure 4 shows how to set the external circuit components values to optimize phase-shedding control with the UCC28063 and UCC25600. The testing power rating is P_{IN} 250 W, and the V_{INAC} range is from 90 V_{AC} to 264 V_{AC}.

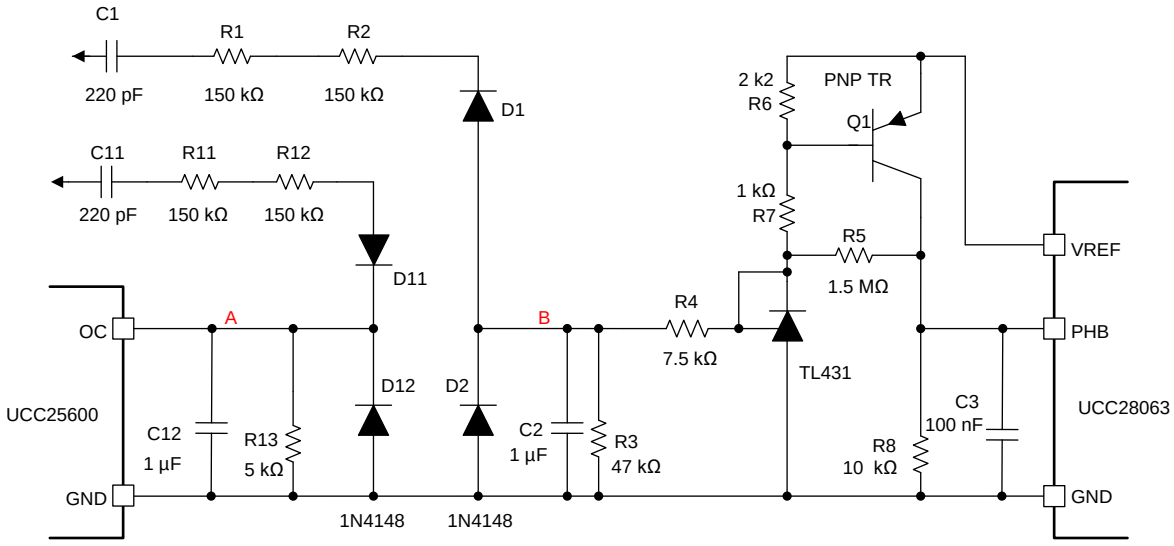

Figure 4. External Phase Control Circuit With the UCC28063 and UCC25600

Table 2 shows the current level value of single- and dual-phase operation, depending on input voltage conditions.

Table 2. Operating 13 V_{OUT} Current Level of Phase Control of the UCC28063

VINAC	GDB off (A)	GDB on (A)
90	3.07	3.46
115	3.08	3.47
180	3.25	3.66
230	3.40	3.80
264	3.46	3.85

Figure 5 shows the waveform of operating in single phase (phase B off), and Figure 6 shows the waveform of operating in dual phase (phase B on) at 90 V_{AC} conditions. Figure 7 shows the waveform of operating in single phase (phase B off), and Figure 8 shows the waveform of operating in dual phase (phase B on) at 264 V_{AC} condition. According to these results, phase-shedding control circuit operates with more accuracy than a traditional circuit.

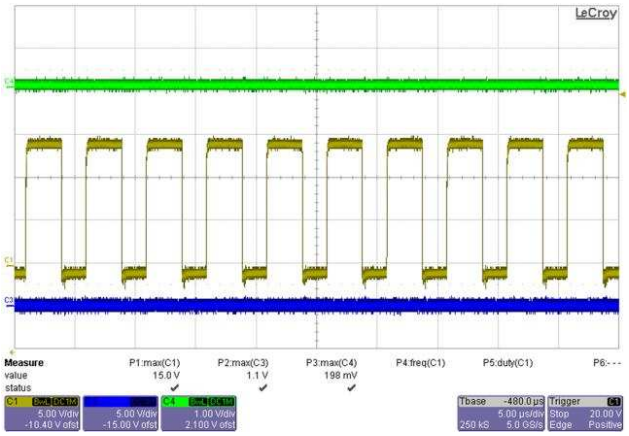

Figure 5. Waveform of Operating Single Phase (90 V_{AC})

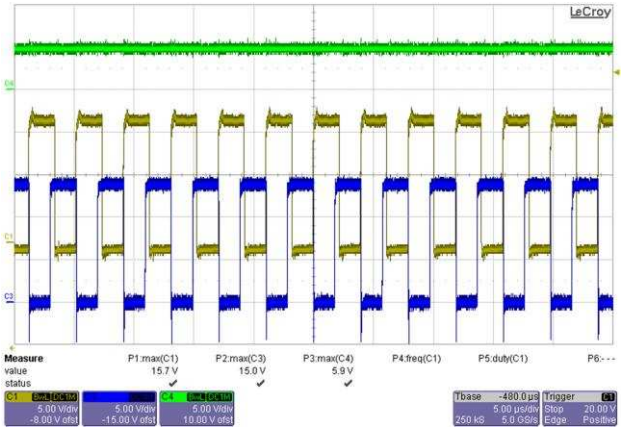

Figure 6. Waveform of Operating Dual Phase (90 V_{AC})

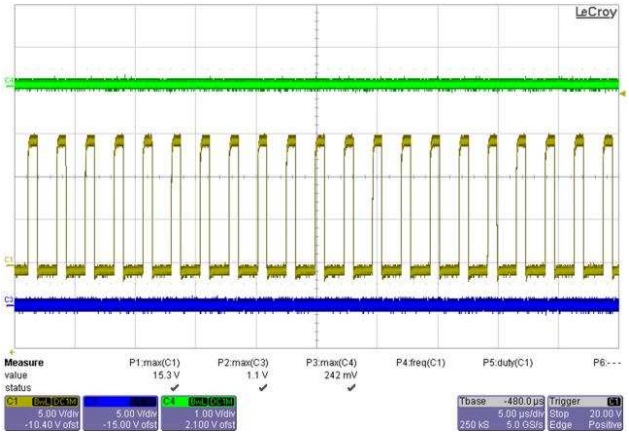

Figure 7. Waveform of Operating Single Phase (264 V_{AC})

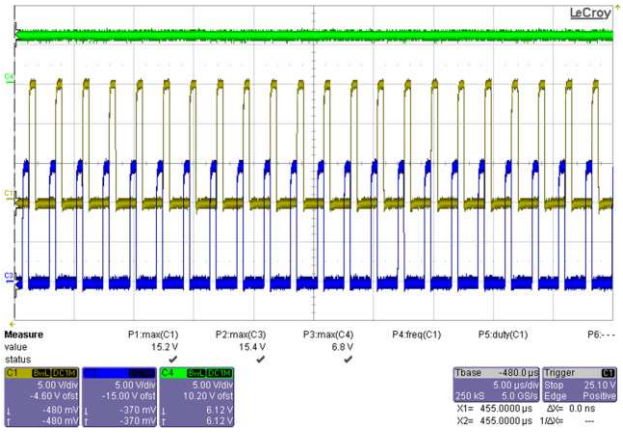

Figure 8. Waveform of Operating Dual Phase (264 V_{AC})

Figure 9 shows a temperature diagram of operating in single phase (phase B off), and Figure 10 shows a temperature diagram of operating in dual phase (phase B on) at P_{IN} = 50-W conditions.

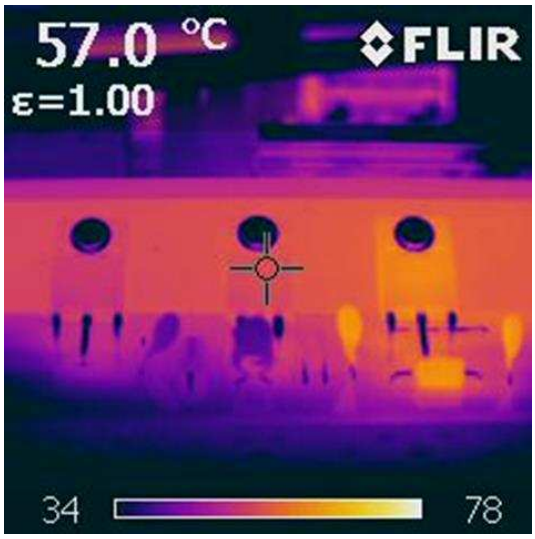

Figure 9. Temperature PFC FET of Operating Single Phase

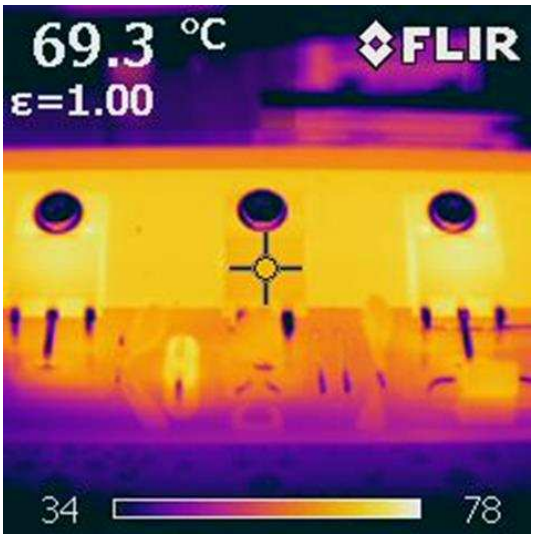

Figure 10. Temperature PFC FET of Operating Dual Phase

With good phase shedding control and an external circuit, Table 3 shows a decrease in temperature of PFC FET of approximately 12°C to 15ºC.

Table 3. Operating 13 V_{OUT} Current Level of Phase Control of UCC28063

Condition (PIN:50W)	GDB off (ºC)	GDB on (ºC)
FET_A	57.0	69.3
FET_B	57.3	72.5

5 Conclusion

For more accurate phase shedding control, the user requires a complex external phase-shedding control circuit instead of a traditional external circuit, using a comp pin base with various test results. This circuit operation is important to match component values and the threshold level between the PFC controller (UCC28063) and the LLC controller. Using this external phase-shedding circuit can achieve lower power dissipation at light-load conditions.

6 Reference

- *UCC28063 Natural Interleaving™ Transition-Mode PFC Controller With Improved Audible Noise Immunity* (SLUSAO7)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Date	Revision	Description
October 2017	*	Initial Release

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