Application Report
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Inverted SEPIC made SIMPLE

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ABSTRACT

There can be quite a few applications that require a conversion from a negative input voltage to a negative output voltage and there are a few ways to go about doing it. The telecom industry is one such example where the rails are usually negative. This design space along with being limited is not well explored. In this application note we will go over the use of an integrated boost regulator in the inverted SEPIC topology to convert a negative input voltage to a negative output voltage.

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1 Introduction

The LM2586 is part of the LM258x family of SIMPLE SWITCHER® boost regulators from Texas Instruments. The internal NPN is capable of handling a voltage of 65V and has a current limit of 4A. The maximum input voltage that the device can handle is 40V. Thus this device makes a good candidate for wide V_{IN} solutions. The design shown here is created for a typical input of -5V and output of -12V at 1A load current, with a common ground between input and output. But it can handle an input voltage range of -5V to -24V. The following sections will talk about the operation.

2 Application Details

The basic operation of this circuit is that of an inverted SEPIC topology. The inverted SEPIC is usually used with devices that have a high side switch (e.g. a buck switcher) because it lets a user design for an output voltage that can be higher or lower than the input voltage. The switching device in this topology needs to be able to withstand a voltage of $+V_{IN}$ and $–V_{OUT}$ with respect to ground which limits the use of most DC/DC integrated buck regulators. But since we are working with negative rails, we can use a device with a low side switch such as the LM2586 in the inverted SEPIC topology and reference the device ground to $–V_{IN}$.

When the NPN is turned on, there are two current paths. One path is from ground, through primary inductor L_1, the internal NPN, $-V_{IN}$ rail and the input capacitor. The second current path is from ground, the output capacitor, secondary inductor, the coupling capacitor, internal NPN, $–V_{IN}$ rail and the input capacitor. During the on time the switch node is at a voltage of $–V_{IN}$ with respect to ground and the voltage at the other end of the coupling capacitor is $–V_{IN}-V_{OUT}$ with respect to ground. Therefore the coupling capacitor is now charging up to V_{OUT}. When the NPN is turned off, the voltages across the two inductors are reversed and the current through them starts ramping down. During the off time the diode, D1, is forward biased. There are two current paths during the off time as well. The first path is from $-V_{OUT}$, secondary inductor L_2, diode D_1, and output capacitor. The second current path is from ground, primary inductor L_1, coupling capacitor, diode D_1 and output capacitor. The switch voltage during the off time is $+V_{OUT}$ with respect to ground and the voltage on the other side of the coupling capacitor is a diode drop above ground. Therefore the device chosen has to be able to sustain a total voltage of $V_{IN}+V_{OUT}$ across it.

The distinct advantage of this topology is that the output sees constant current like that in the buck topology. This makes the output ripple much cleaner and smaller. Figure 1 shows the steady state waveform with the secondary inductor current, switch voltage and the output voltage ripple. While Figure 2 shows the design schematic. Reference 1 talks about the actual design equations and component selection.

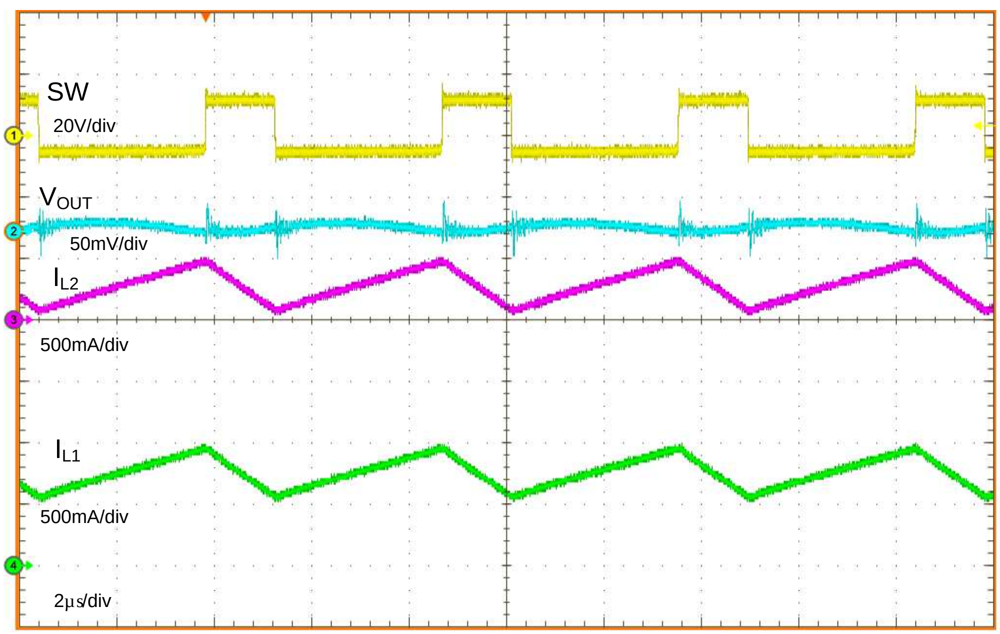

Figure 1. $-5V_{IN}$ $-12V_{OUT}$ 300mA I_{OUT}

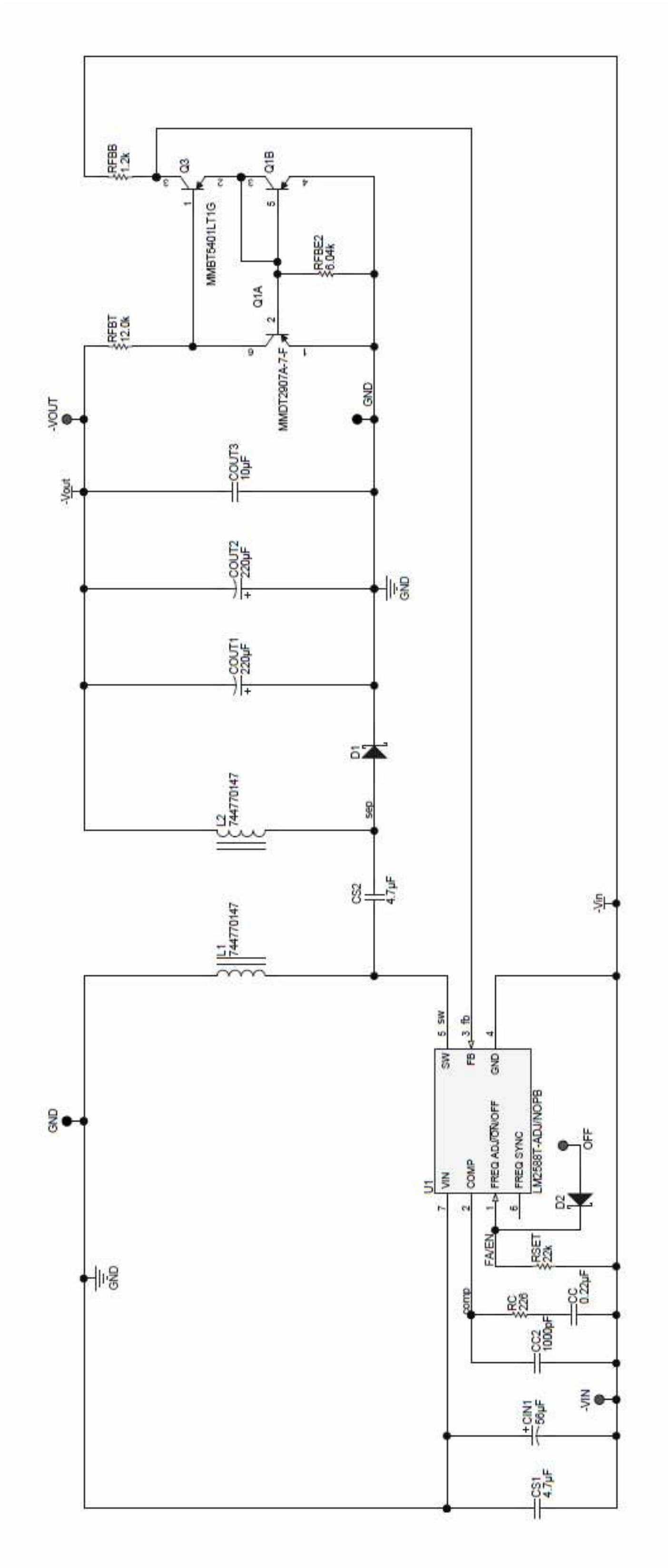

Figure 2. Design Schematic

In this design, the ground of the IC is referenced to the negative input voltage. A current mirror is used to set the feedback current and consequently the regulated output voltage. Use of an ordinary two transistor current mirror would cause the output to have a dependency on the V_{BE} of the transistor. In order to remove that dependency a third transistor, Q_3, and resistor R_{FBE2}, are connected as shown in the design schematic. From the schematic we can see that the voltage at the upper feedback resistor will be two diode drops below ground, i.e. $-2V_{BE}$. The lower feedback resistor is chosen such that there is 1mA of current flowing through it. Therefore we get,

$$R_{FBB} = \frac{V_{REF}}{0.001} \tag{1}$$

The reference voltage V_{REF} for the LM2586 is 1.2V. Therefore R_{FBB} is set to be 1.2kΩ. An additional resistor, R_{FBE2} is connected between ground and the common base of the two transistors. This resistor helps pull more current from ground to FB and that current gets added to the current flowing through the upper feedback resistor. This current can be realized as

$$I_{RBE2} = \frac{V_{BE}}{R_{BE2}} \tag{2}$$

Without this resistor, R_{FBE2}, the current flowing through the upper feedback resistor would be

$$I_{RFBT} = \frac{V_{OUT} - 2 \cdot V_{BE}}{R_{FBT}} \tag{3}$$

With the addition of this resistor, this current is now re-written as

$$I_{RFBT} = \frac{V_{OUT} - 2 \cdot V_{BE}}{R_{FBT}} + \frac{V_{BE}}{R_{FBE2}} \tag{4}$$

From Equation 4 we can observe that the value of R_{FBE2} will affect the output voltage. If it is set to be exactly half of the upper feedback resistor, R_{FBT}, then we could get an output voltage that would not depend on the transistor's V_{BE}. Therefore when R_{FBE2} is set to $R_{FBT}/2$, we get

$$I_{RFBT} = \frac{V_{OUT} - 2 \cdot V_{BE}}{R_{FBT}} + \frac{2 \cdot V_{BE}}{R_{FBT}} \tag{5}$$

This can be written as

$$I_{RFBT} = \frac{V_{OUT}}{R_{FBT}} \tag{6}$$

We set the feedback current to be 1mA. Therefore setting I_{RFBT} to 1mA, we can find the required value for R_{FBT}.

$$R_{RFBT} = \frac{V_{OUT}}{I_{RFBT}} \tag{7}$$

The two PNPs forming the current mirror should have very close matching so as to get a well-matched current and consequently lesser variation in V_{OUT}. The best way to ensure that is to find a device that has two PNPs packaged together. This way the two V_{BE}s will change together with temperature. Another note to keep in mind is that while laying out the board, the transistors should be kept away from the high current paths.

3 Test Results

The following scope plots and efficiency data were taken on the custom PCB. Figure 3 shows the line regulation at I_{OUT} of 400mA. Because of the modified current mirror, there is very little variation on the output with input voltage.

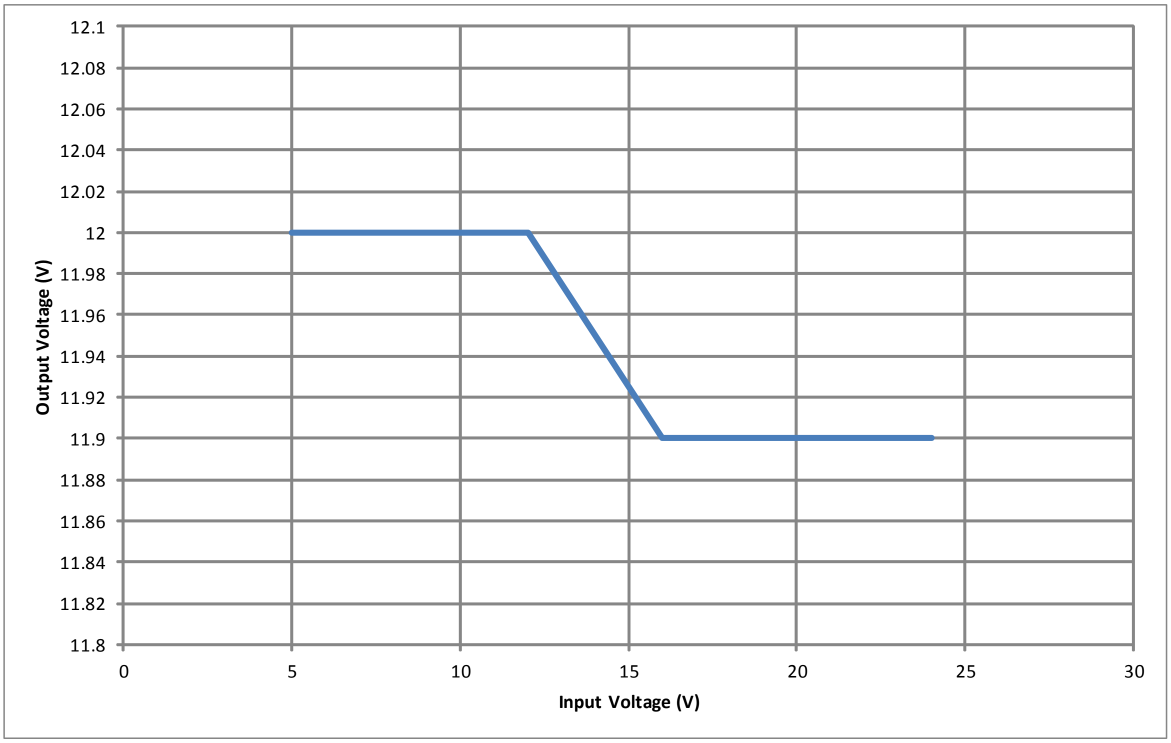

Figure 3. Line Regulation, I_{OUT} = 400mA

Figure 4 shows the efficiency of the design with respect to the load current and different V_{IN}s.

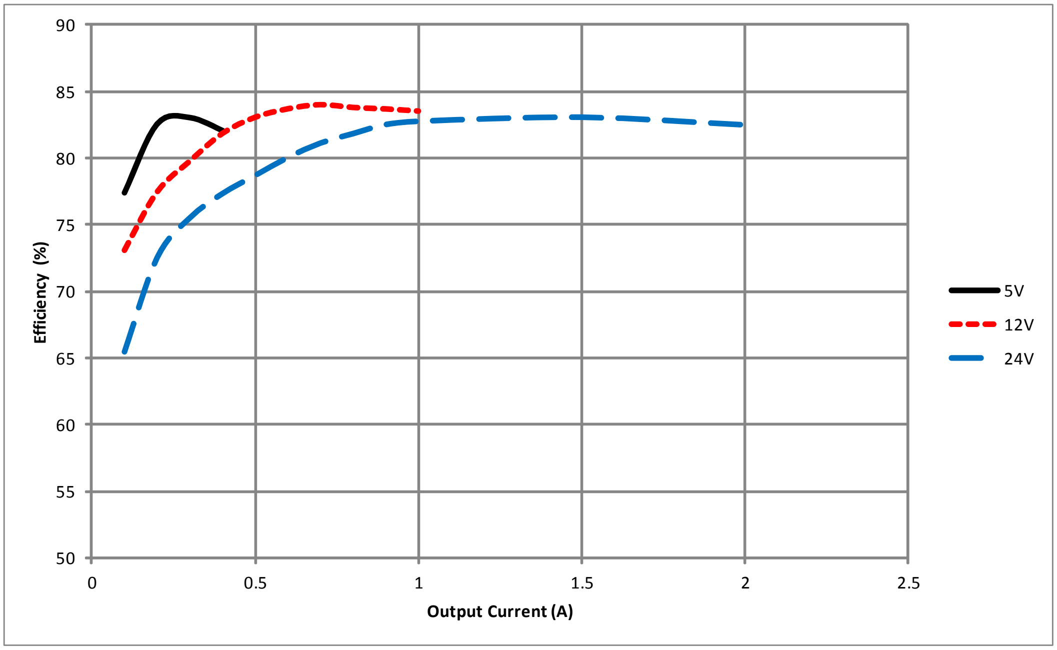

Figure 4. Efficiency Vs. I_{OUT}, V_{OUT} = -12V

Figure 5 shows the load regulation of the design with the input voltage set to -12V.

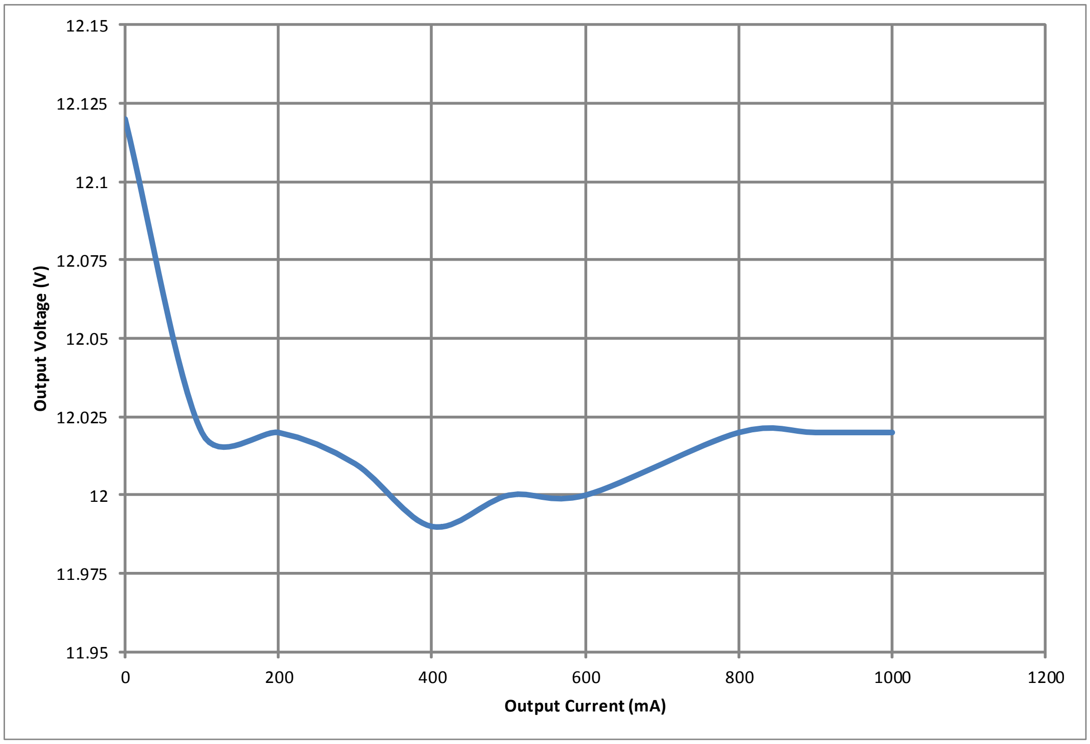

Figure 5. Load Regulation, V_{IN} = -12V

Because of a relatively high switch current limit of 4A, the LM2586 can allow high output currents. Figure 6 shows the max load that the device can drive vs. the input voltage it is operating at.

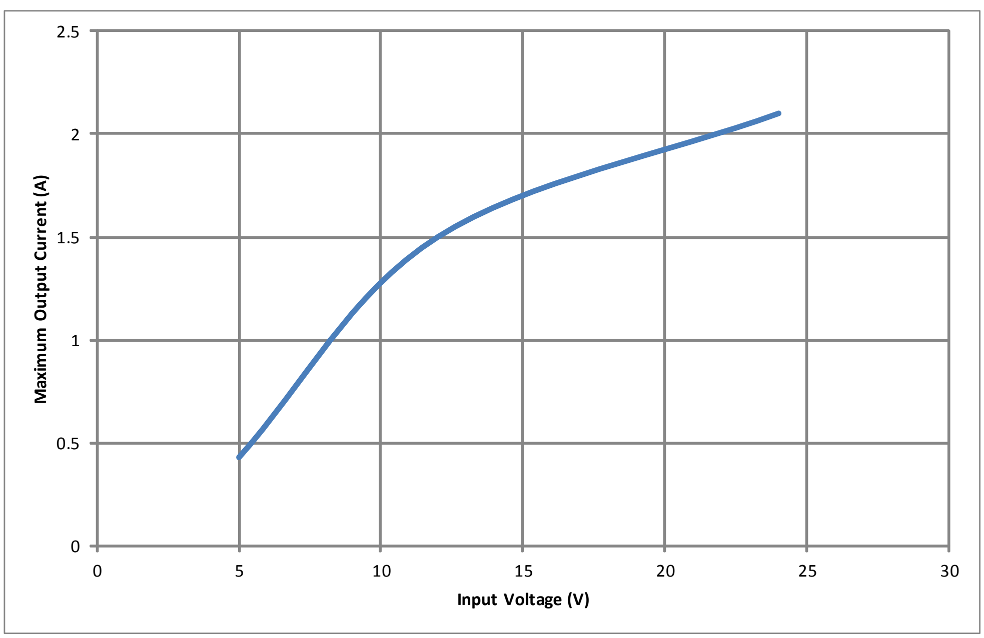

Figure 6. Maximum Output Current Vs. Input Voltage

As mentioned before, one advantage of the inverted SEPIC is that the output sees constant current. This means that the RHP zero is eliminated in this topology. This makes the design a little easier to compensate and the resulting load transient response would be faster. Figure 7 shows the result of a 200mA to 1A load transient at the output.

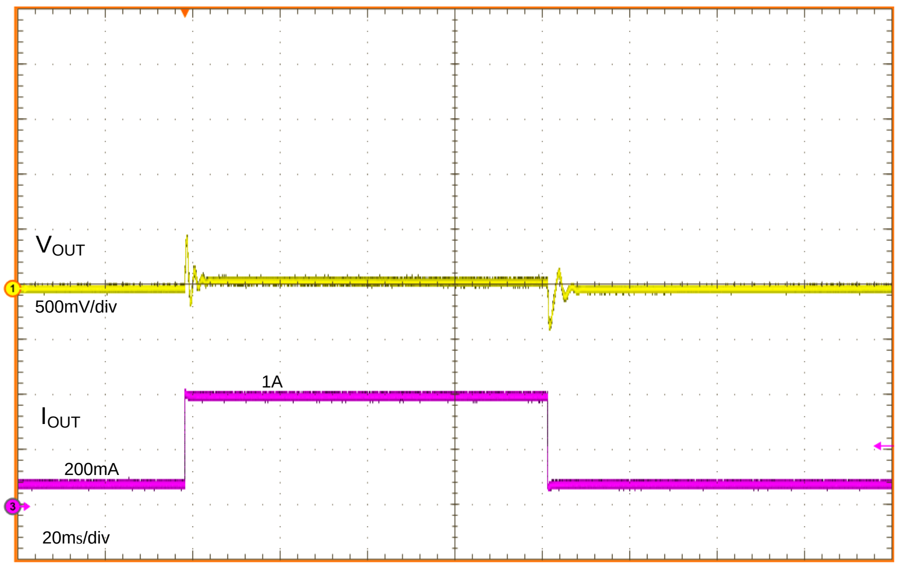

Figure 7. Load Transient V_{IN} = -12V, V_{OUT} = -12V, I_{OUT} = 200mA to 1A

Figure 8 shows the startup behavior of the design. In certain systems inrush currents shown aren't tolerated. In order to reduce the inrush currents a longer softstart is desired. To add more softstart time an external circuit can be added. Please refer to application note titled Soft-start Using Constant Current Approach to learn more about this.

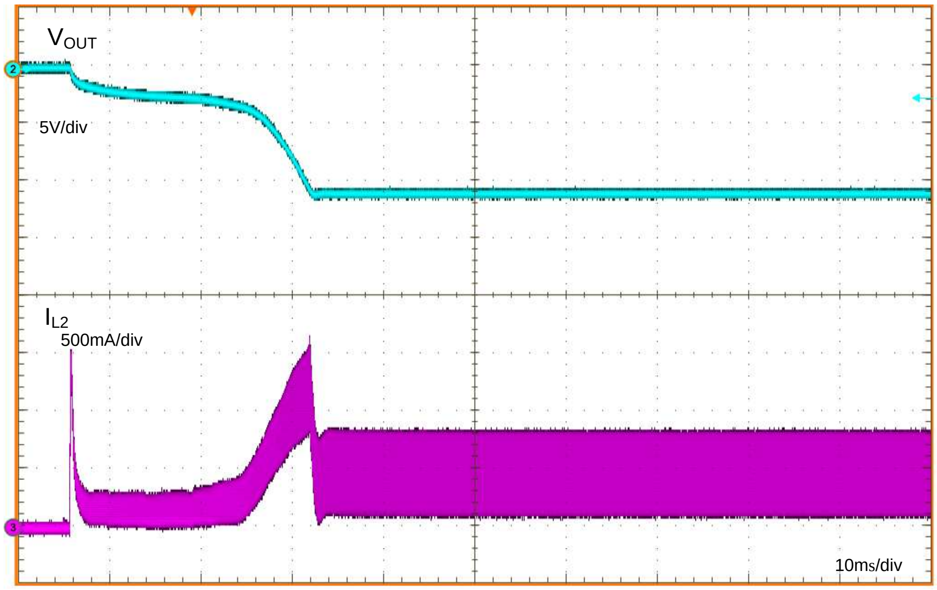

Figure 8. Startup V_{IN} = -12V, V_{OUT} = -12V, I_{OUT} = 500mA

Table 1. Design BOM

DESIGNATOR	DESCRIPTION	PART NUMBER
C_C	CAP, CERM, 0.22 µF, 16 V, +/- 5%, X7R, 0805	0805YC224JAT2A
C_{C2}	CAP, CERM, 1000 pF, 100 V, +/- 5%, C0G/NP0, 0805	08051A102JAT2A
C_{IN1}	CAP, AL, 56 µF, 50 V, +/- 20%, 0.34 ohm, SMD	UUD1H560MNL1GS
C_{IN2}	CAP, CERM, 10 µF, 100 V, +/- 20%, X7R, 6x5x5mm	CKG57NX7R2A106M500JH
C_{OUT1}, C_{OUT2}	CAP, AL, 220 µF, 35 V, +/- 20%, 0.15 ohm, SMD	EEE-FC1V221P
C_{S2}	CAP, CERM, 4.7 µF, 100 V, +/- 10%, X7S, 1210	C3225X7S2A475K200AE
C_{OUT3}	CAP, CERM, 10 µF, 50 V, +/- 10%, X5R, 1206_190	CGA5L3X5R1H106K160AB
D_1	Diode, Schottky, 100 V, 2 A, PowerDI123	DFLS2100-7
D_2	Diode, Schottky, 40 V, 1 A, SOD-123	1N5819HW-7-F
L_1 , L_2	Inductor, Shielded Drum Core, Ferrite, 47 µH, 2.7 A, 0.076 ohm, SMD	744770147
Q_1	Transistor, Dual PNP, 60 V, 0.6 A, SOT-363	MMDT2907A-7-F
Q_3	Transistor, PNP, 150 V, 0.5 A, SOT-23	MMBT5401LT1G
R_{FBE2}	RES, 6.04 k, 1%, 0.125 W, 0805	CRCW08056K04FKEA
R_C	RES, 226, 1%, 0.125 W, 0805	CRCW0805226RFKEA
R_{FBB}	RES, 1.21 k, 1%, 0.125 W, 0805	CRCW08051K21FKEA
R_{FBT}	RES, 12.1 k, 1%, 0.125 W, 0805	CRCW080512K1FKEA
R_{SET}	RES, 22.1 k, 1%, 0.125 W, 0805	CRCW080522K1FKEA

4 Conclusion

Thus we see that just by adding a few external components, a SIMPLE SWITCHER® boost regulator like the LM2586 could be used in an inverted SEPIC topology to obtain a negative output from a negative input. The showcased design has good line regulation and load transient response.

5 References

1. *Designing DC/DC converters based on ZETA topology*

IMPORTANT NOTICE

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