Application Report

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Cost Effective Transformer-less OFFLINE SUPPLY for Light-Load Applications

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ABSTRACT

This design idea provides a simple non-isolated AC/DC power supply for low power applications. The design uses a "capacitive-dropper" front-end combined with a LM46000 SIMPLE SWITCHER® buck regulator from Texas Instruments. The circuit provides 3.3 V at a minimum of 100 mA from a line supply of 90 VAC to 265 VAC. Theory of operation as well as design equations and performance results are given.

Contents

List of Figures

List of Tables

1 Introduction

Many times a simple off-line power supply is required for low power applications such as E-meters, battery chargers, etc. Typically, the need is to convert the line voltage to a small DC value such as 3.3 V or 5 V. This can be done with a line frequency power transformer or a complex AC/DC off-line power supply. Both approaches have well known disadvantages of weight, size, and/or complexity. A better option is shown in Figure 1.

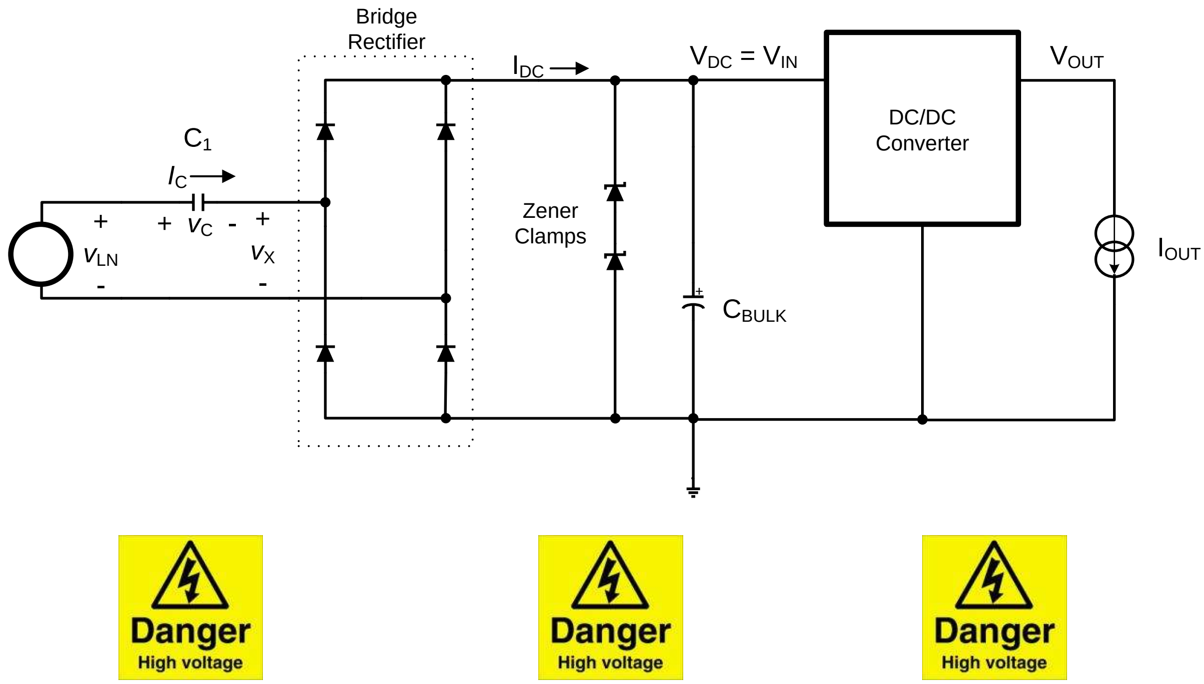

Figure 1. Basic Schematic

Here we first convert the line voltage to an intermediate unregulated DC rail (V_{DC}) and then use a Wide V_{IN} range DC/DC converter to supply the load. The front-end is the well-known full-wave "capacitive-dropper". The Zener diodes clamp the input voltage to the DC/DC converter under no-load conditions. The input voltage to the DC/DC converter ($V_{DC} = V_{IN}$) is set to a relatively high value, so that the current required from the "capacitive-dropper" can be kept low. For this design we use the LM46000 as the DC/DC converter and V_{DC} is set to 48 V. The LM46000 converts this down to 3.3 V. For a line voltage range of 90 VAC to 265 VAC, this design can supply at least 100 mA to the 3.3 V load. The high step-down ratio, possible with the LM46000, allows the 100 mA load to appear as less than 10 mA load to the front-end. This permits a small value of C_1 to be used.

It is easy to see that this circuit is connected directly to the line supply and is not isolated. EXTREME CAUTION must be used when experimenting with this design. The user must ensure that the intended application for this power supply, including the load on the LM46000, is completely isolated from any contact with grounded entities; including people, animals and test equipment. All safety precautions must be observed when taking measurements. Test equipment with grounded inputs can not be used with this circuit without proper isolation. The user is also responsible for any fusing, transient protection, and/or EMI filtering required on the input to this circuit.

2 Theory of Operation

The idea behind this circuit is that the series capacitor C_1 acts as a lossless resistance and the reactance of the capacitor will set the maximum current that can be provided. Since a normal electrolytic capacitor cannot handle the stresses resulting from the line voltage, we use "X"-type capacitors which would be rated for the maximum line voltage in our range. From Figure 1 we can understand that the current I_C through the cap C_1 would be flowing when there is a voltage differential across the capacitor. The capacitor current would steadily increase while v_{LN} is increasing. When the line voltage reaches the peak voltage, C_1 stops charging, because the slope of the differential voltage across it goes to zero. Figure 2 shows the relevant waveforms; where we have the following definitions:

v_{LN} = line voltage

v_C = C_1 voltage

i_C = C_1 current

v_X = Voltage at input of bridge rectifier

V_{LN} = RMS line voltage

V_{DC} = V_{IN} = DC intermediate bus voltage and input voltage to DC/DC

V_{OUT} = Output voltage of DC/DC

I_{OUT} = Output current of DC/DC = user load current

V_D = One diode drop

F = line frequency = 1/T

η = Efficiency of LM46000

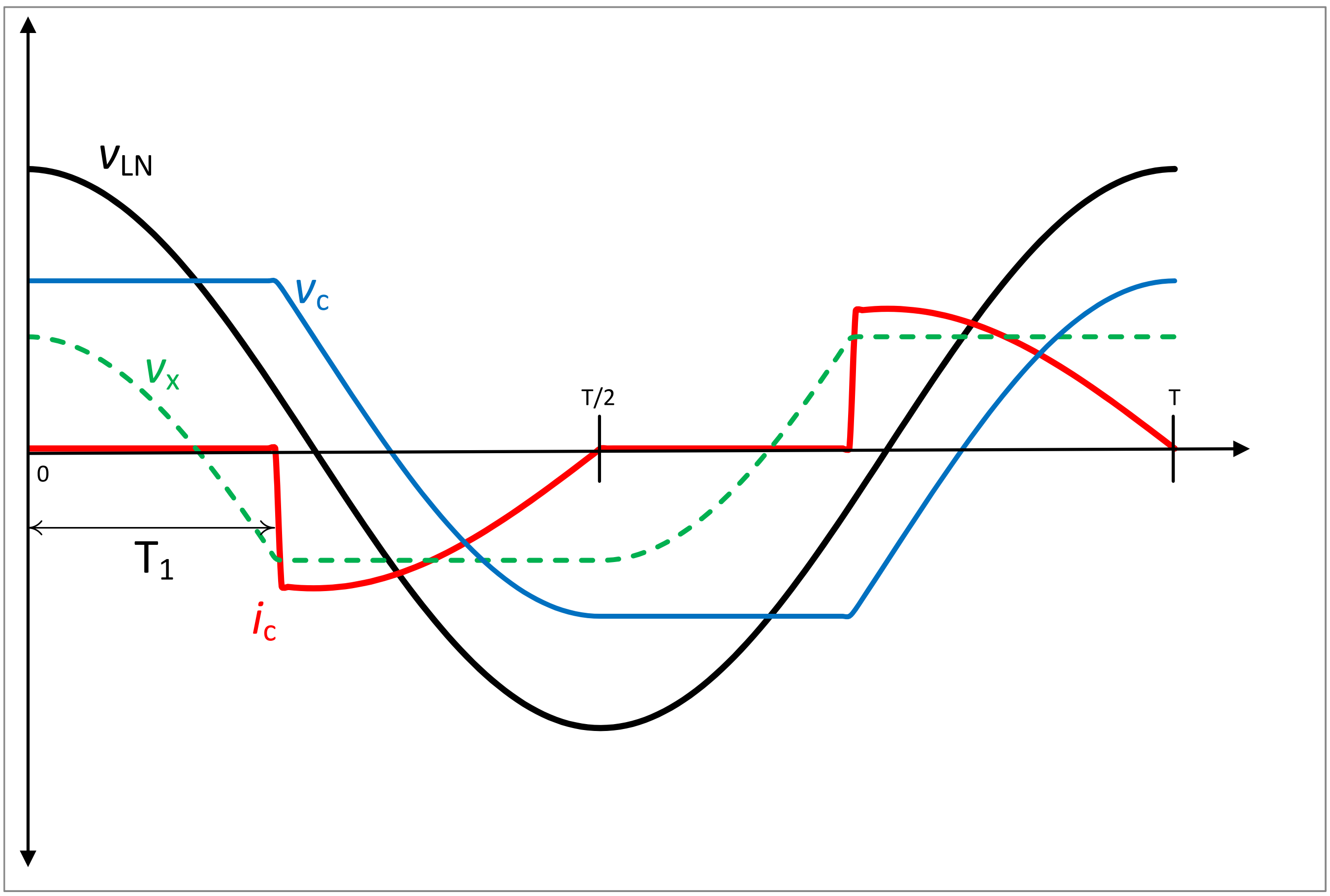

Figure 2. Voltage and Current Waveforms

The peak capacitor current can be obtained as follows:

$$I_P = 2\pi \cdot F \cdot C_1 \cdot V_{LN} \cdot \sqrt{2}$$

where

- I_P = Peak C_1 current (1)

To know the amount of DC current (I_{DC}) coming from the bridge rectifier, we would first need to know the time duration, T_1, for which the capacitor current is zero. Observing the timing in Figure 2 we can see that at time T_1 one of the diode pair turns on. Thus the voltage across the capacitor at time T_1 would be equal to the peak line voltage minus V_{DC} . From that time T_1 can be equated to be as follows:

$$T_1 = \frac{1}{2\pi \cdot F} \cdot \cos^{-1}\left(1 - \frac{\sqrt{2} \cdot (V_{IN} + V_D)}{V_{LN}}\right) \tag{2}$$

Knowing time T_1, we can find the DC current value. The I_{DC} is basically the area under the rectified capacitor current curve (i_C). The area can be found by integrating the curve from time T_1 to T/2 and multiplying by 2. The expression for I_{DC} is shown as follows:

$$I_{DC} = 4 \cdot V_{LN} \cdot \sqrt{2} \cdot F \cdot C_1 \cdot \left(1 - \frac{(V_{IN} + V_D)}{\sqrt{2} \cdot V_{LN}}\right) \tag{3}$$

This is the DC current that the capacitor C_1 can provide to the input of the LM46000. As mentioned previously, the advantage of interfacing a Wide V_{IN} DC/DC converter with the "capacitor drop" front-end is that a fairly small duty cycle can be possible. This means that the input current requirement will also be fairly small for a required load current. The DC input current to the LM46000, I_{INDC}, can be estimated by assuming the worst case efficiency of the switching converter shown as follows:

$$I_{INDC} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{4}$$

The worst case situation in the cap drop circuit will occur at lowest line voltages. The capacitor C_1 needs to be sized such that at lowest line voltage of 90 VAC it can still provide enough current to keep the bulk caps charged to 48 V. At lowest line, the Zener diodes will not see any current flowing through them and the I_{DC} will be equal to I_{INDC}. Knowing this value, we can then calculate the amount of capacitance we need at minimum V_{LN} of 90 VAC as shown:

$$C_1 = \frac{I_{DC}}{4 \cdot V_{LN} \cdot \sqrt{2} \cdot F \cdot \left(1 - \frac{(V_{IN} + V_D)}{\sqrt{2} \cdot V_{LN}}\right)} \tag{5}$$

3 Application Circuit and Plots

WARNING

CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING, AND USE OF THE CIRCUITS FOUND IN THIS DOCUMENT.

LETHAL VOLTAGES ARE PRESENT IN THESE CIRCUITS THAT MAY CAUSE INJURY.

THE USER MUST ENSURE THAT SAFETY PROCEDURES ARE FOLLOWED WHEN WORKING ON THESE CIRCUITS.

Let's look over some BOM calculations for the capacitor dropping circuit.

3.1 Dropping Capacitor

The dropping capacitor C_1 is sized for the lowest line voltage thus ensuring that the load current is maintained even at the worst case. For our design requirements and from Equation 5 the cap C_1 is sized to be about 0.56 µF rated for 375 VAC. Care must be taken to not oversize this capacitor. Oversizing this capacitor would increase I_{DC} and would cause greater power dissipation in the Zener diodes at higher line voltages. This capacitor must be rated for the highest peak line voltage.

3.2 Zener Diodes

The LM46000 is rated for a maximum input voltage of 60 V and a load current of 500 mA. Therefore V_{DC} can be clamped at a high voltage of 48 V. The Zener voltage established V_{DC}. As shown in the schematic two Zener diodes of 24 V each have been used in series to obtain a clamping voltage of 48 V. It is important to size the Zener diodes for the right power requirement. From schematic in Figure 1, we can observe that

$$I_Z = I_{DC} - I_{INDC} \tag{6}$$

At low line voltages of 90 VAC, to maintain load at the output of the converter all of I_{DC} would be supplied to the input of the converter. The Zener current I_Z would be zero then. But with increasing line voltages, I_{DC} would be more than what the switcher requires and therefore I_Z would no longer be zero. At high line voltage I_Z would be considerably high and would therefore cause some heating in the device. The worst case is when all of I_{DC} flows in the Zener. The power in the Zener is then:

$$P_Z = I_{DC} \cdot V_{DC} \tag{7}$$

3.3 Bulk Capacitor

A bulk electrolytic capacitor of 680 µF is used to hold the 48 V with low ripple voltage. Keeping the ripple voltage on the intermediate rail low will also help with keeping the output voltage ripple low. Having enough bulk capacitance is also important to maintain enough voltage at the input of converter in case of a fast load transient at the output of the converter. A range of 470 µF to 680 µF was tested to be appropriate. Figure 3 shows the voltage ripple at the input of the LM46000. The 680 µF cap results in a 100 mV ripple at 120Hz. Since the ripple at V_{DC} is at a relatively low frequency, it is important to keep the ripple low because it cannot be filtered effectively by the inductor and the output capacitor of the LM46000.

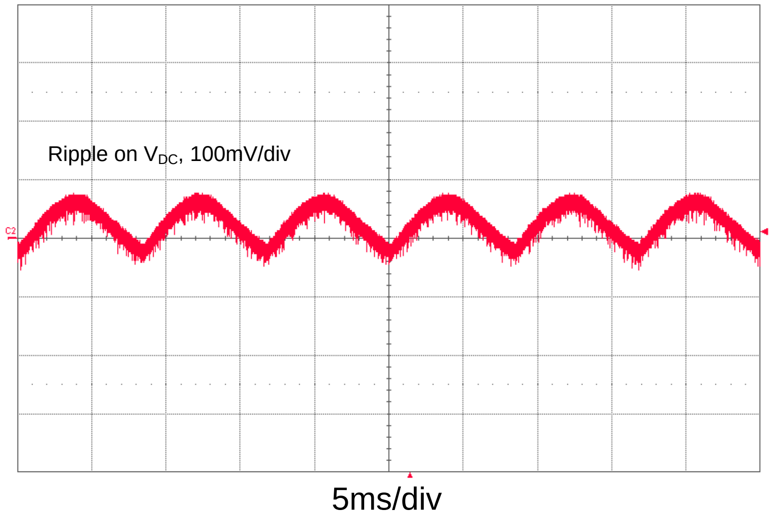

Figure 3. Voltage Ripple at V_{DC}

The newly released LM46000 Wide V_{IN} DC/DC converter was interfaced with the "capacitive drop" front-end to obtain the schematic as shown in Figure 4.

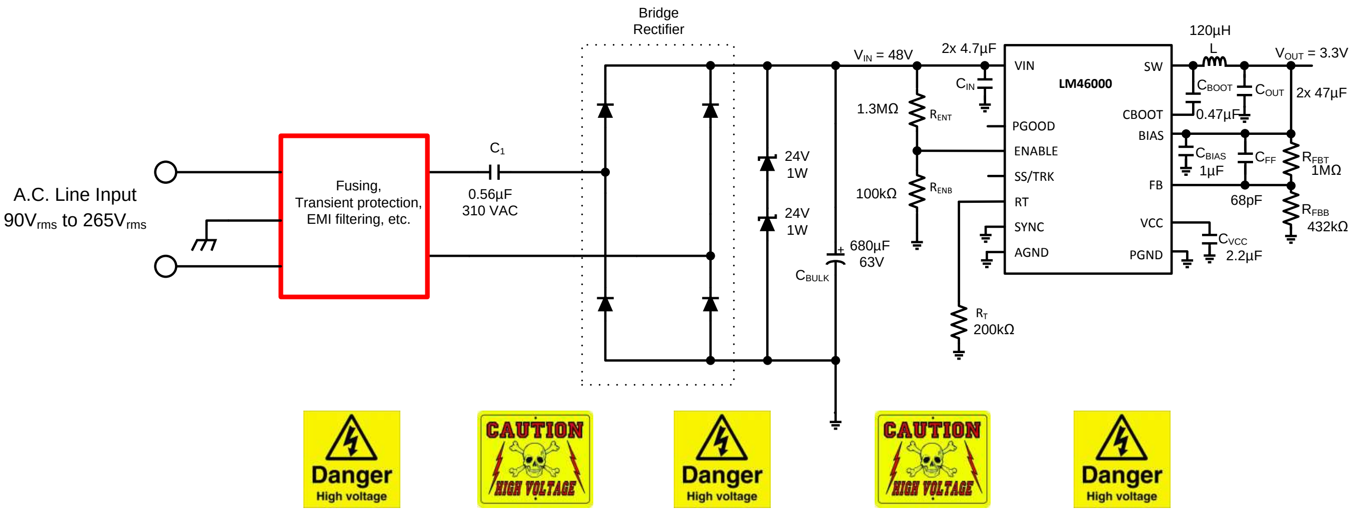

Figure 4. Application Schematic

Table 1. Application Requirements

Parameter	Value
V_{LN}	90 VAC to 265 VAC
V_{OUT}	3.3 V
I_{OUT}	100 mA
η at 120 VAC and 160 mA	71 %
I_{RMS} from line at 120 VAC	23 mA

The BOM for the LM46000 can be calculated for V_{IN} of 48 V to V_{OUT} of 3.3 V. The design can be obtained from the datasheet for LM46000. The data sheet has detailed calculations for the entire BOM. The rising UVLO threshold on the LM46000 was set to about 30 V. This helps with limiting the inrush currents and potential voltage crash at the input of the converter. The resulting falling UVLO threshold is about 25 V.

For the application circuit shown in Figure 4 load regulation test was performed at 120 VAC line voltage and line regulation test was performed at 100 mA I_{LOAD}. At light loads, the LM46000 enters the PFM mode. In this mode the switching frequency is folded back to improve the efficiency. In PFM operation, a small positive DC offset is required at the output voltage to activate the PFM detector. This can be seen in Figure 5. Please refer to the LM46000 data sheet (SNVSA45) for more information.

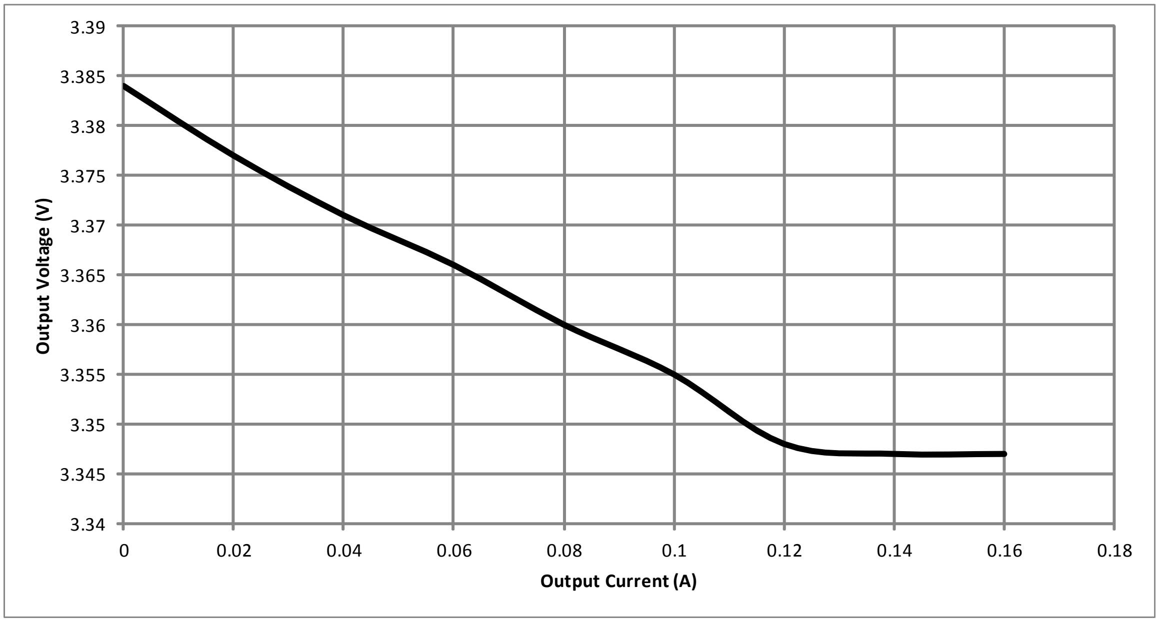

Figure 5. Load Regulation

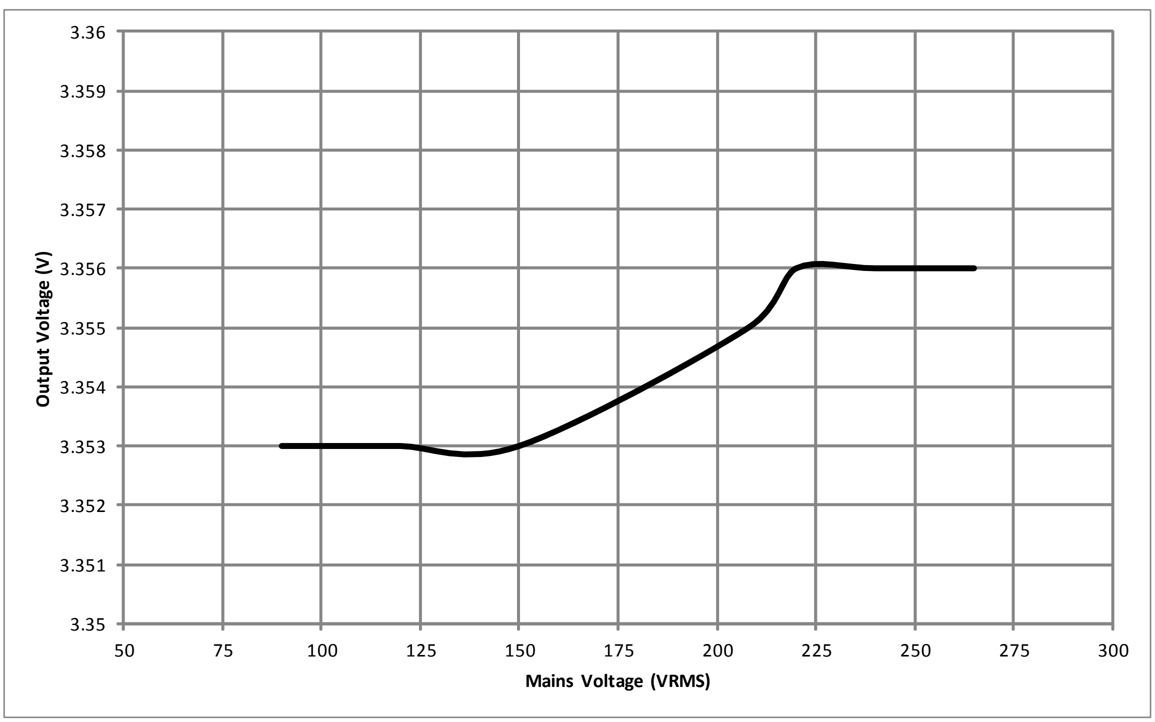

Figure 6. Line Regulation

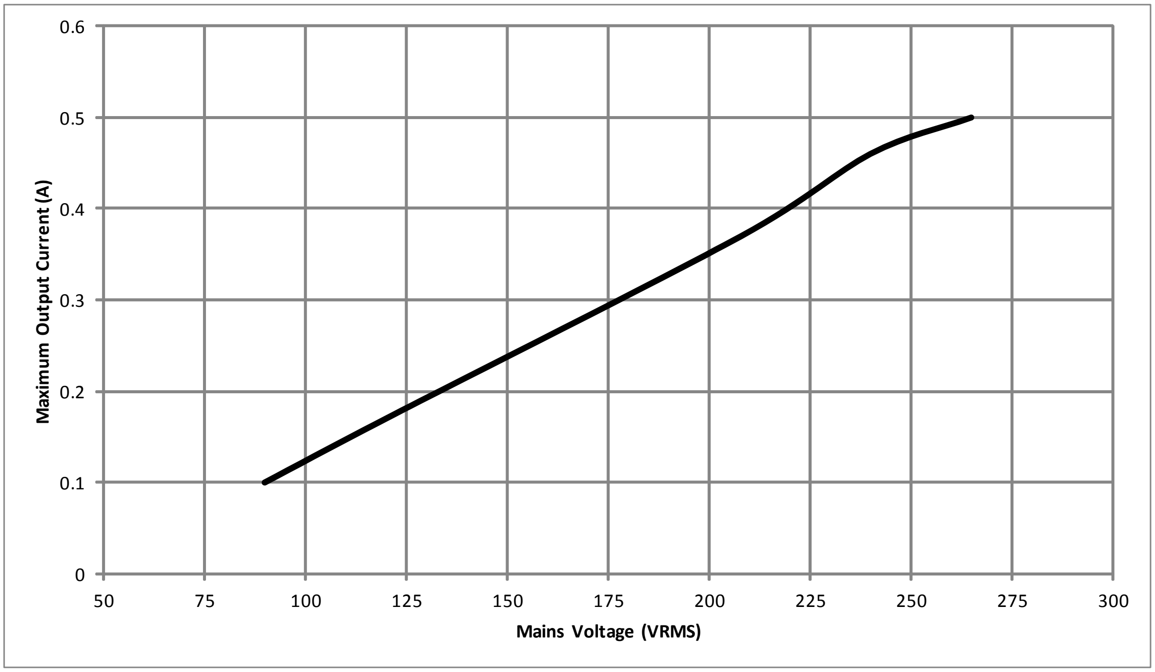

Figure 7. Max Output Current vs Line Voltage

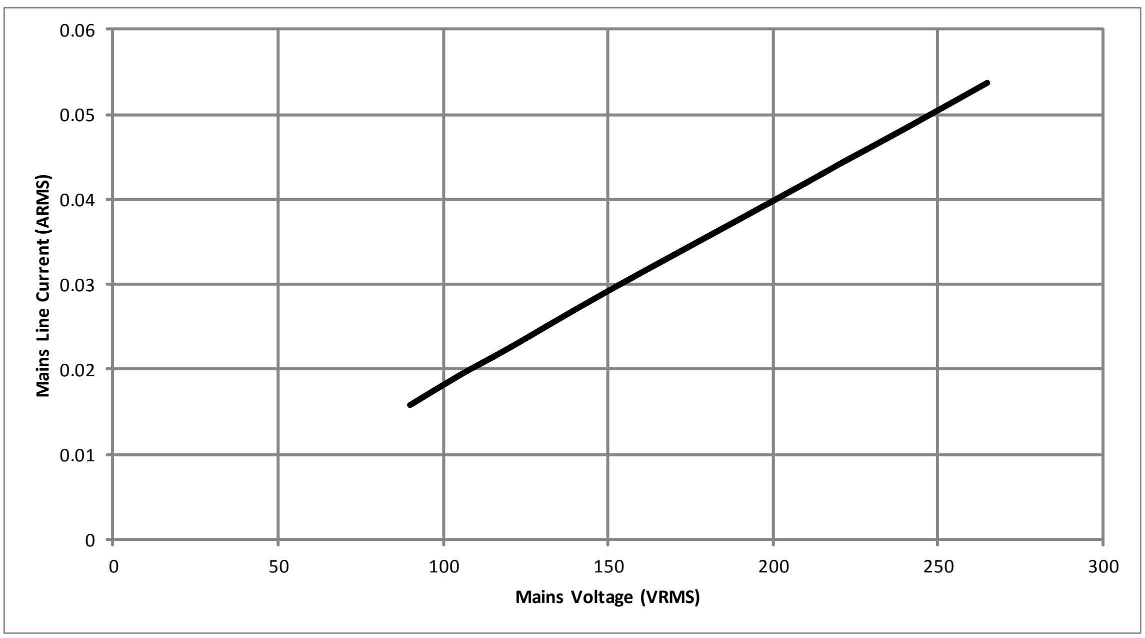

Figure 8. Line Current Vs Line Voltage

With increasing line voltage, more current can be delivered to the input of the LM46000. This means that more current can be delivered at the output also. At the max line voltage of 265 VAC about 500 mA of current can be delivered to the output of the LM46000. Figure 7 shows the max current capability at increasing line voltages.

4 Conclusion

The cap drop circuit is an easy cost effective approach for low load AC-to-DC conversion. Interfacing with a Wide V_{IN} DC/DC converter can be further useful to draw relatively higher loads at the output while keeping the current drawn from the line low. A maximum of 500 mA can be obtained from the output of the LM46000 at 265 VAC line voltage. While this circuit is easy to make, utmost care should be taken to create a bench prototype and appropriate filtering and protection circuit should be added.

5 References

1. A Capacitor-Fed, Voltage-Step-Down, Single-phase, Non-Isolated Rectifier Authors: Nathan O. Sokal, K. Kit Sum, David C. Hamill

Revision History

Changes from Original (May 2015) to A Revision	Page
• Changed to V_{LN} from V_{LINE}	6

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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