Application Report
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Layout Considerations for LMG5200 GaN Power Stage

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ABSTRACT

Gallium Nitride (GaN) based power FETs are finding increasing use in high efficiency power converters. GaN FETs provide zero reverse recovery charge (Qrr) and very low gate charge. These features result in very high switching performance. Voltage slew rates on the order of 50 V/ns or higher for GaN FETs is common.

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1 Introduction

Gallium Nitride (GaN) based power FETs are finding increasing use in high-efficiency power converters. GaN FETs provide zero reverse recovery charge (Qrr) and very low gate charge. These features result in very high switching performance. Voltage slew rates on the order of 50 V/ns or higher for GaN FETs is common. [1]

Such high switching speeds causes a very significant increase in the rate of current commutation compared to conventional silicon power FETs. Special considerations during package design of LMG5200 power stage ensures that the common source inductance, gate loop inductance and power loop inductance can be significantly reduced.

To achieve optimum performance, it is critical to use an appropriate layout of external components when designing with the LMG5200 power stage. The proper placement of capacitors provides high-frequency decoupling for the gate driver and bootstrap input capacitors is critical to ensure that there is no loss of gate drive during high-voltage switching and current commutation.

It is critical that the board has the lowest thermal resistance possible between the LMG5200 power stage and the ambient temperature and under worst case operating conditions the system does not overheat and cause catastrophic failures. This application report provides guidelines for a multilayer board design to ensure that the maximum benefit of an integrated gate driver and GaN FET half bridge module is obtained both thermally and electrically.

This application report is divided into two sections, the first section is specific to a DC-DC converter layout for the LMG5200 power stage. The first section covers both the electrical and thermal considerations required to ensure that maximum performance from the switch mode supply could be observed. While this application report uses a buck power stage as an example, the principle can be extended to any DC-DC converter as long as the critical loops are identified.

The second section covers the fundamentals of layout and delves into non-idealities for components used in power converters. The second section provides the physics behind why the proposed layout practices are observed for LMG5200-based converters.

2 LMG5200 Power Stage Layout

To understand the impact of board level parasitics on the performance of the LMG5200 power stage, the various key loops are identified in Figure 1. High power loop inductance (shown in red) causes significant overshoot on the switch node. The overshoot causes a loss of efficiency due to increased switching losses. To minimize this loop inductance, it is critical to use the layout techniques described here to effectively eliminate the parasitic loop inductance.

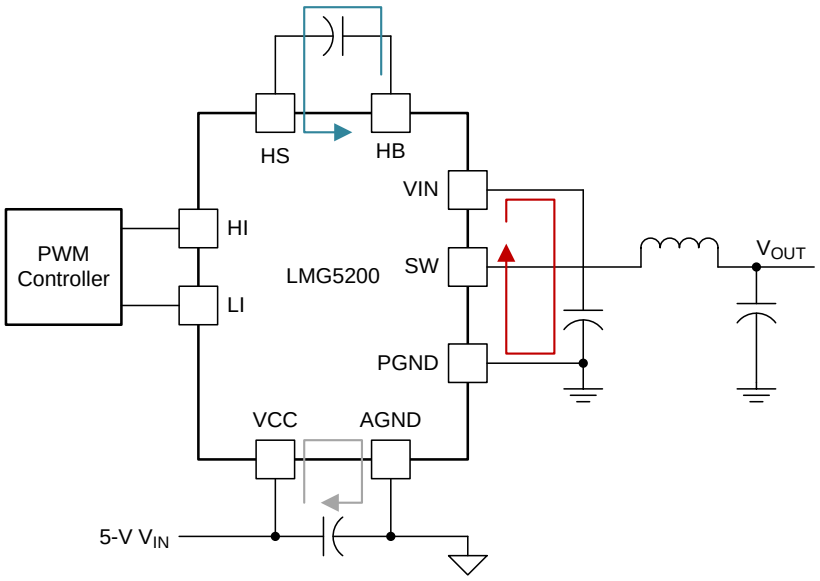

Figure 1. Buck Converter Application Using the LMG5200 Power Stage

The addition of parasitic switch node capacitance is also a switching loss mechanism as the parasitic capacitor is charged and discharged with each switching cycle to the switch node voltage. Minimize the switch-node capacitance by reducing the overlap between the switch-node plane and the ground and VIN planes. To minimize the added switch node capacitance it is recommended that there be a cutout for the switch node in the metal 2 plane and possibly the subsequent layers as well. In addition, sensitive control and analog signals should be kept away from the SW pin and the switch-node net to minimize coupling and interference. The power inductor (or transformer) should be located as close to the IC as possible to minimize the area of the switch-node,reducing parasitic capacitance and EMI. [2] [3]

To eliminate spurious loss of input power, minimize the parasitic inductance from the input decoupling capacitors to VCC and AGND. Similarly, to prevent power loss in the high-side driver and cause undervoltage lockout, the added inductance between the bootstrap capacitor and HB-HS should be minimized by choosing an appropriate capacitor and suggested layout techniques.

Figure 2 shows the best practices for minimizing board level parasitics for a multilayer board. It should be noted that the board stack up is critical to minimize the parasitic impedances. Distance between top layer and metal 2 should be made as small as possible. It is preferred that metal 2 be made to have the return path to ensure effective inductance cancellation. Distance between top layer and metal 2 should be made as small as possible (≤5 mil) to help with reducing the parasitic inductance as described in Figure 2.

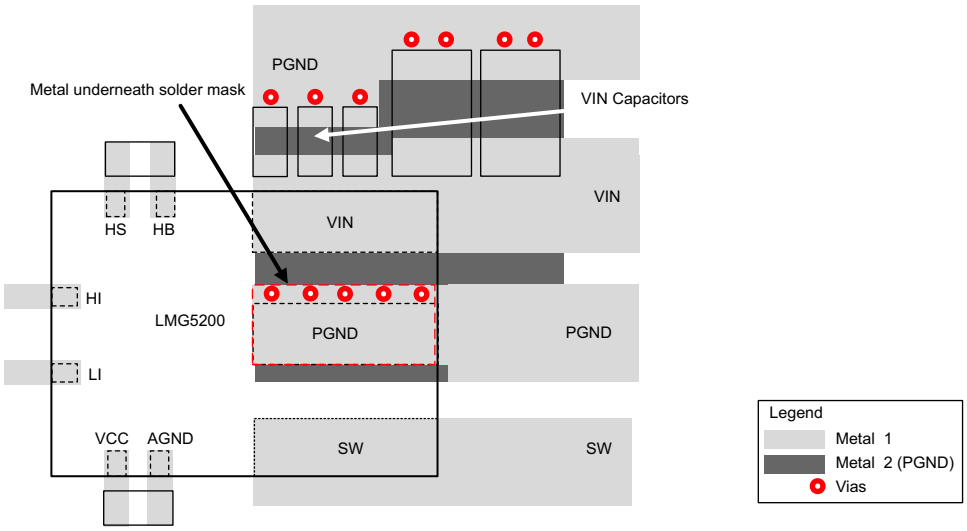

Figure 2. Board Layout

Proper supply bypass of the low-side and high-side drivers is essential in providing stable switching performance without malfunction. Using 0402 sized capacitors, placed immediately adjacent to the IC on the top layer will ensure that the trace inductance for the bootstrap capacitor to HS-HB will be minimized. Similarly choosing a 0402 capacitor for VCC decoupling will also minimize the trace from the capacitor to the VCC, AGND pins and reduce the parasitic inductance. A high amount of inductance in these loops will cause a loss of gate drive to the high side and low side, which will hurt efficiency and circuit performance. If the inductance is high, a spurious loss of the drive signal below the undervoltage lockout threshold causes the device to turn off the gate supply completely to prevent damage to the GaN FETs.

Figure 3 shows the PCB cross section for the LMG5200 power stage. Note that the input capacitors are close to the VIN pin on the top layer (same layer as power stage). The metal 2 is immediately below the top layer with minimal spacing between the top layer and metal 2 (≤5 mil). This ensures that the power loop inductance is minimized. As discussed in *Section 3*, Equation 2 add the number of vias needed to minimize extra resistance and minimize inductance. Vias also help to reduce the thermal resistance to the board. A 12-mil core via typically has a thermal resistance in the order of 75°C/W. In the design of the buck converter, 12 vias are used for an output of 6 A. These via are placed as close as possible to the pad without violating the pad to via clearance required by the PCB manufacturer. This helps in reducing the thermal resistance and the electrical resistance also of note is that 12-mil vias are used where possible as these have a higher current capability. [4]

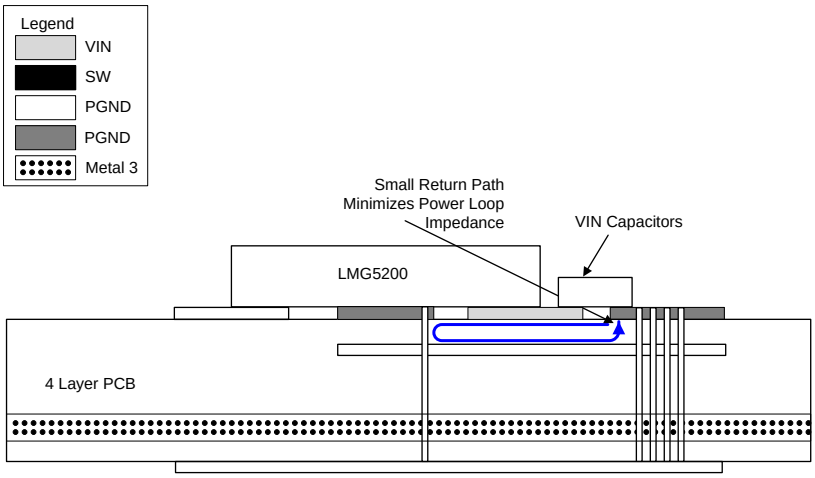

Figure 3. Cross-Section of the LMG5200 PCB Layout

As a general rule, 12-mil vias with 1 oz copper, has maximum current carrying capacity of 0.75 A. Figure 4 shows the power stage schematic for this layout example.

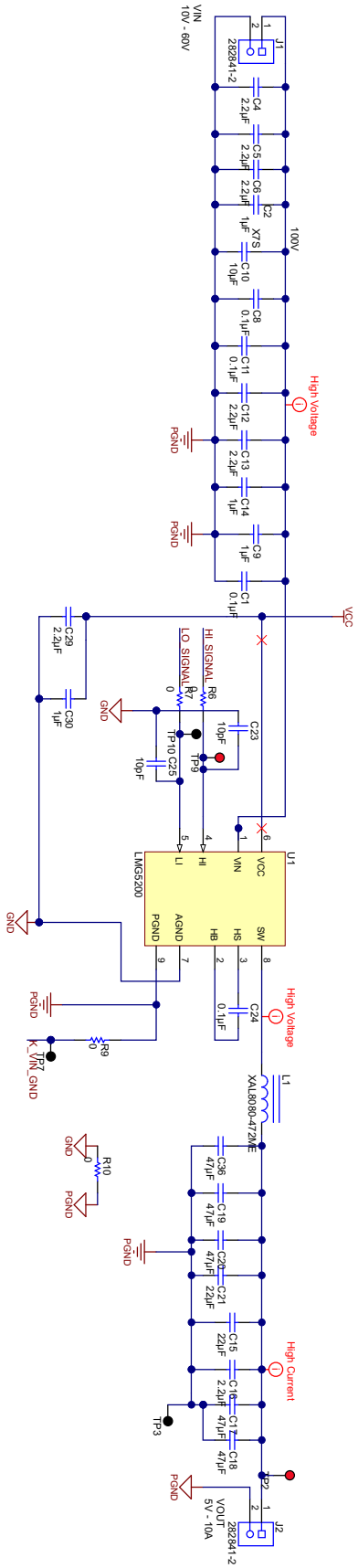

Figure 4. Power Stage Schematic

As shown in Figure 5 through Figure 9, U1 is the indicator for the LMG5200 power stage and L1 is the indicator of the inductor. C1 and C13 indicate the high-frequency capacitors and need to be in close proximity to the LMG5200 power stage. An adequate number of vias must be added to the system to ensure sufficient thermal conductivity in close proximity of heat source. In the board layout shown in Figure 4, more than 20 vias are added to the GND, VIN, and VOUT nodes. The added via thermal resistance is very small (less than 1°C/W), adding more vias does not necessarily improve the board thermal performance as the board-to-ambient thermal resistance remains present and becomes a large part of the junction-to-ambient resistance.

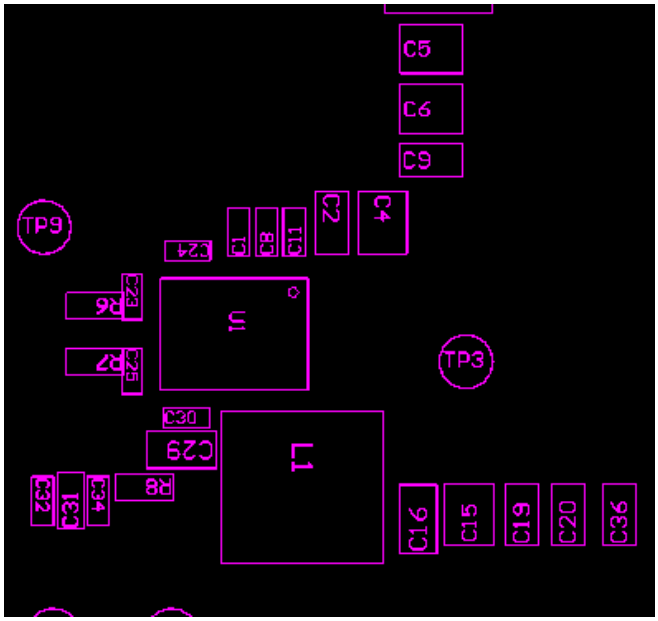

Figure 5. Placement of Components

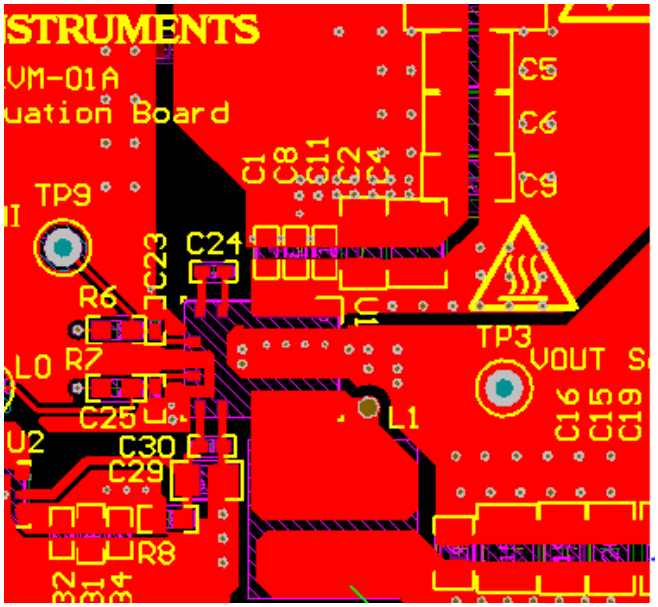

Figure 6. Top Layer

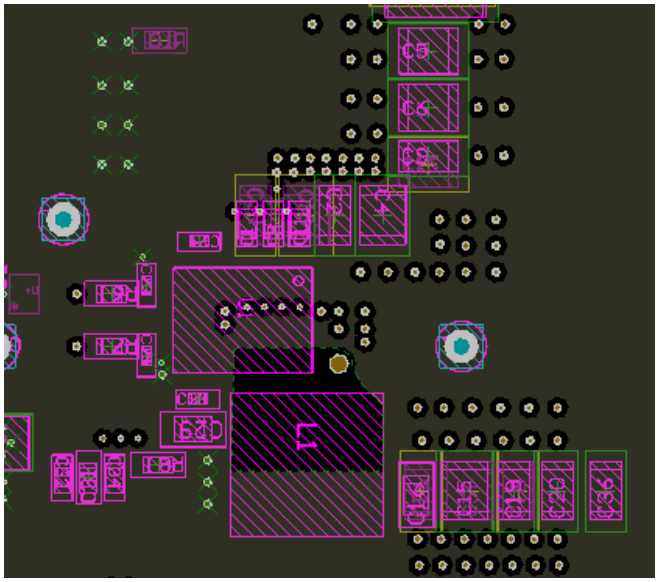

Figure 7. Ground Plane

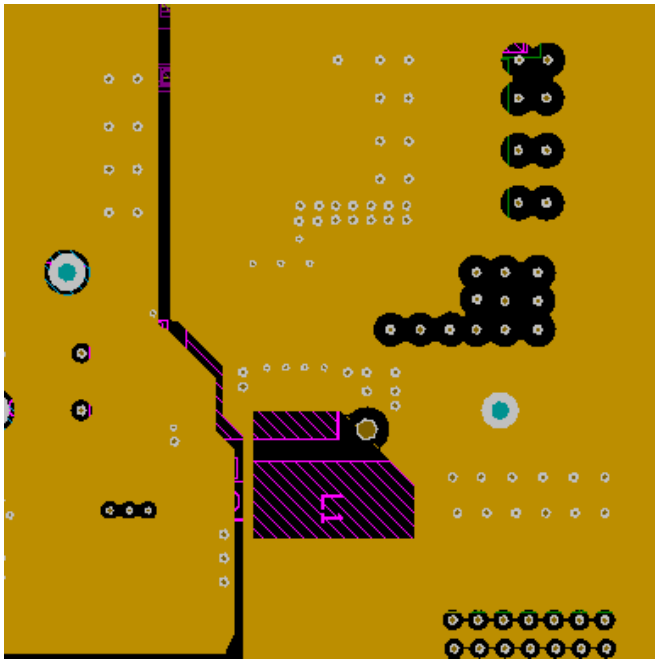

Figure 8. Middle Layer

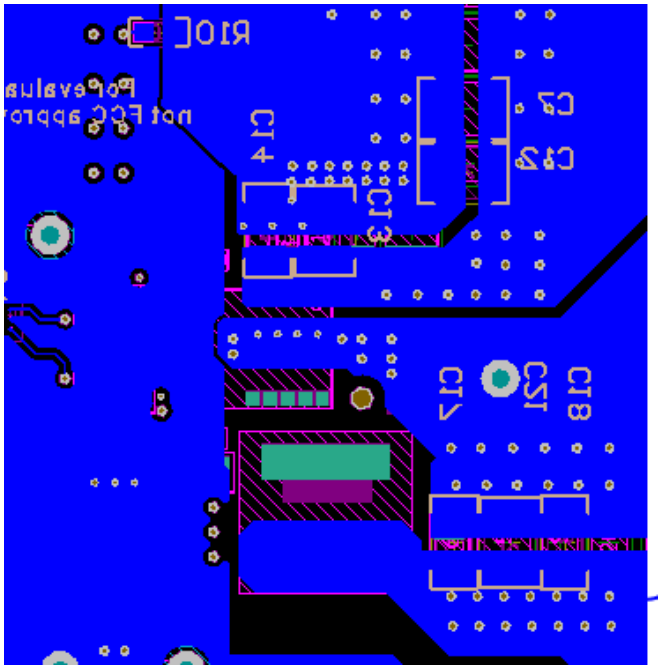

Figure 9. Bottom Layer

Figure 10 is the waveform of the switch node probed in the LMG5200 showing minimal overshoot and extremely low power loop inductance.

Figure 10. Switch Node Waveforms

Thermal performance of LMG5200 for the board layout are shown in Figure 11 and Figure 12 under these conditions:

- V_{IN} = 48 V
- V_{OUT} = 5 V
- I_{LOAD}= 5 A
- f_{SW} = 1 MHz
- T_A = 25°C

In this condition, the converter is 90% efficient, with approximately 0.5 W of dissipation in the inductor and 2W of dissipation in the LMG5200.

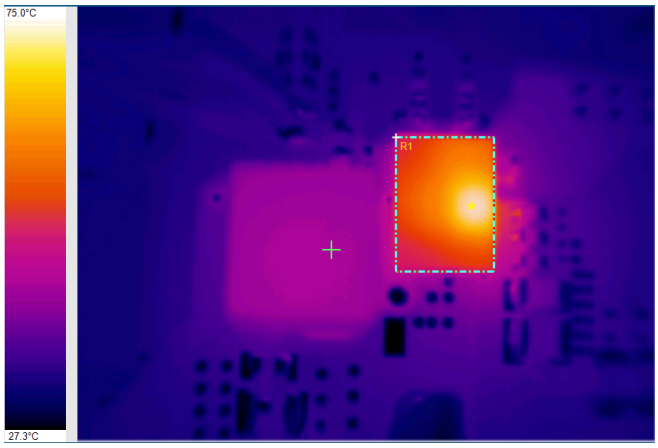

Figure 11. With No Airflow, 2-W Dissipation

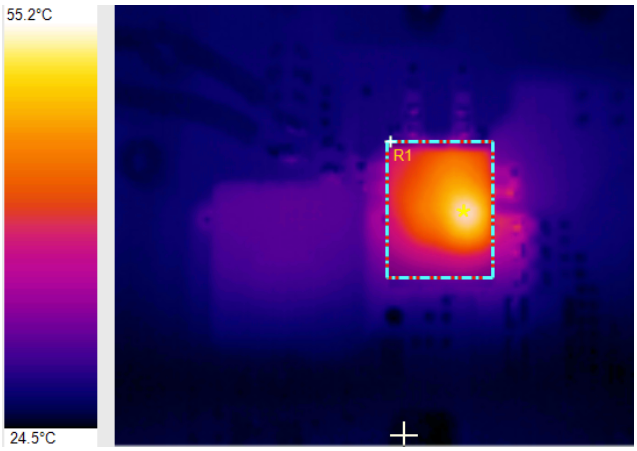

Figure 12. WIth Airflow, 2-W Dissipation

With no airflow and approximately 2-W dissipation, the average case temperature is 61.5°C and maximum case temperature is 75°C. With airflow, the average case temperature is 43°C and maximum case temperature is 55.2°C. These conditions are measured with ambient air at 25°C

3 Fundamental of Board Level Parasitics

Resistance of the printed circuit board provides an additional power loss mechanism in DC-DC converters. With good layout practices and the right selection of components, this loss mechanism can be reduced. This section describes how to calculate the resistance of common PCB features: rectangular traces and vias.

Equation 1 calculates the resistance of any conductor.

$$R = (\rho \times l)/A \quad (1)$$

where

- ρ is the resistivity of copper
- l is the length of the trace
- A is the cross sectional area conducting the current

NOTE: When choosing a board material, it is important to note that plated copper has a resistivity of 6 μΩ/cm, which is significantly higher than pure copper which is 1.7 μΩ/cm.

Vias on PCBs use plated copper where the resistance is significantly higher, so an adequate number of vias should be considered when designing boards for high current. In some PCBs, plating is also applied to the surface (top and bottom layers) to increase the copper thickness. If the board is designed to be a one-plate-one board, this implies that the addition of the extra plated copper only provides about 25% reduction for in the resistance for a 2 oz. board compared to a 1 oz. board with no plated copper.

NOTE: Copper resistance varies linearly with temperature and doubles from 25°C to 280°C.

3.1 Vias

Vias can also add significantly to resistance. Use Equation 2 to calculate the resistance of vias.

$$R = \frac{\rho l}{\pi \times (r_0^2 - r_1^2)} \tag{2}$$

Traces add not only resistance but add inductance and capacitance as well. Added inductance is in the order of 6 nH/cm for a conductor without appropriate return path in close proximity.

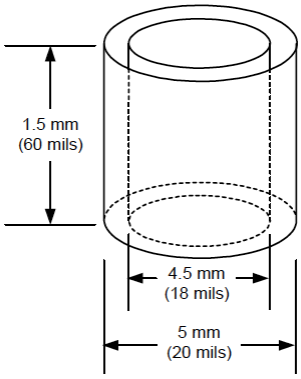

Figure 13. Via Dimensions

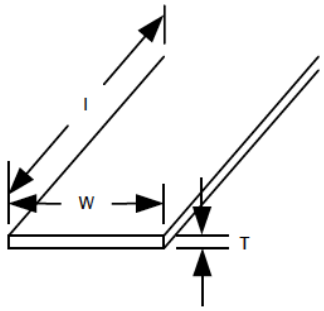

Figure 14. Inductance Dimensions

Self-inductance of a trace can be accurately calculated as shown in Equation 3 (note trace dimensions are in cm) and assumes transmission line behavior of the trace and is useful as a guide for calculating the approximate trace inductance.

$$L = 2 \times l \times \ln\left(\left(\frac{1}{T + W}\right) + \frac{1}{2}\right) \tag{3}$$

Effective use of ground return planes in close proximity to the trace can significantly reduce the inductance of the trace. If H is the distance between the trace and the ground plane, then the calculated inductance is as follows

$$L = \frac{2 \times H \times v \times l}{W} \tag{4}$$

where

- L is the loop inductance, in nH
- l is the length of the trace, in cm
- W is the width of the trace, in cm
- H is the height of the trace above the ground plane, in cm

Ground plane effectiveness is determined not only by the distance between the conducting trace and the plane (H) but also by the width of the ground plane. To ensure that there is effective cancellation of inductance it is necessary that the ground plane be much wider than conducting trace.

Knowing the impact of ground planes on effective cancellation of inductance, this technique can be used to significantly reduce the power loop inductance and gate loop inductance. Because these loops carry significant .

Capacitive coupling between PCB layers can yield advantages and disadvantages in power PCB design. The capacitance between traces can be identified as described in Equation 5.

$$C = \frac{\varepsilon_0 \times \varepsilon_r \times A}{t}$$

where

- A is the area of the copper planes
- ε_r is the relative permittivity of the PCB dielectric
- ε_0 is the permittivity of air
- t is the distance between the conductors (in meters) (5)

Capacitive coupling can be used to advantage for creating coupling between the input and ground planes which can be used for high frequency decoupling in addition to the decoupling capacitors added to the system. Also it is important to note that to minimize the switching node capacitance a cutout directly underneath the inductor and the associated traces in the PGND plane and the subsequent planes helps minimize the added parasitic capacitance on the switch node.

4 Conclusion

GaN FETS are finding use in high frequency DC-DC converters. Special layout techniques are required to ensure that maximum performance of the DC-DC converter is obtained. Advantages and disadvantages of some commonly used techniques to design for the LMG5200 power stage have also been discussed. A fundamental overview on board level parasitics has been provided as a background for some of the layout choices that are made which should provide the designer with best practices for high frequency DC-DC converters board design.

5 References

1. White Paper: *Advancing Power Supply Solutions Through the Promise of GaN* (SSZY017)
2. Application Report: *Layout Tips for EMI Reduction in DC / DC Converters* (SNVA638)
3. Henry Ott, *Noise Reduction Techniques in Electronic Systems* (John Wiley and Sons, 1988)
4. Application Report: *Semiconductor and IC Package Thermal Metrics* (SPRA953)

Revision History

Changes from Original (March 2015) to A Revision	Page
• Changed typo in part number in graphic	3

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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