AN-2296 SM72295: Highly Integrated Gate Driver for 800VA to 3KVA Inverter

ABSTRACT

This application note describes the design principles and circuit operation of TI's highly Integrated Gate driver in the Low Frequency Inverters.

The inverter industry is expected to witness many technological innovations in the coming years to cater to a larger number of applications and new categories of end users. The demand from retail showrooms, small offices and residential use is primarily for 800VA, 1 kVA, 1.4 kVA and 2 kVA inverters. Being a highly fragmented, competitive and growing market, it is in desperate need of constant Innovation and Integration.

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1   Introduction

Gate Driver is a power amplifier that accepts a low-power input from a controller IC and produces the appropriate high-current gate drive for a power MOSFET. The gate driver must source and sink current to establish required Vgs. A gate driver is used when a pulse width- modulation (PWM) controller cannot provide the output current required to drive the gate capacitance of the MOSFET. Gate drivers may be implemented as dedicated ICs, discrete transistors, or transformers. They can also be integrated within a controller IC. Partitioning the gate-drive function off the PWM controller allows the controller to run cooler and be more stable by eliminating the high peak currents and heat dissipation needed to drive a power MOSFET at very high frequencies.

1.1   Basics of Gate Drive Requirement

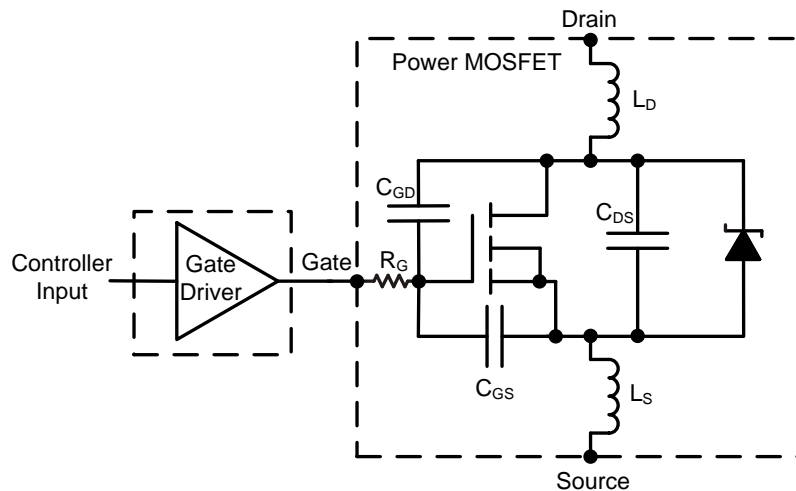**Figure 1. Simplified Model of a Non Inverting Gate Driver IC and a Power MOSFET**

A Real MOSFET's Properties

* Fundamentally a voltage controlled switch.
* Inherent parasitic capacitors.
* Rds(ON) is not negligible.

This leads to the requirement of Gate driver which must source and sink current to establish required threshold voltage from Gate to Source Vgs.
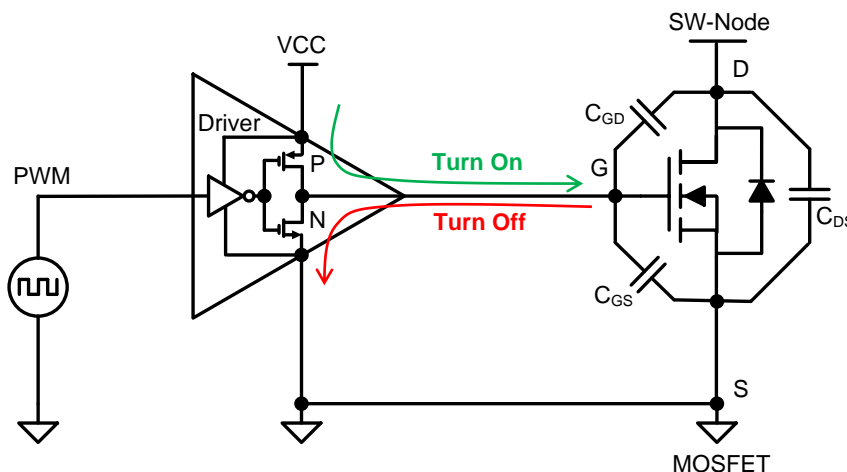

Figure 2. A Closer Look of Driver Driving the MOSFET

Figure 1 shows the simplified model, including the parasitic components that influence high-speed switching, gate-to-source capacitance (CGS), the gate-to-drain capacitance (CGD), and drain-to-source capacitance (CDS).Values of the source inductance (LS) and drain inductance (LD) depend on the MOSFET's package. The other parasitic component is RG, the resistance associated with the gate signal distribution within the MOSFET that affects switching times. An important attribute for the gate driver is its ability to provide sufficient drive current to quickly pass through the Miller Plateau Region of the power-MOSFET's switching transition. This interval occurs when the transistor is being driven on or off, and the voltage across its gate-to-drain parasitic capacitor (CGD) is being charged or discharged by the gate driver. Figure 3 plots total gate charge as a function of the gate-drive voltage of a power MOSFET. Total gate charge (QG) is how much must be supplied to the MOSFET gate. to achieve full turn-on. It is usually specified in nanocoulombs (nC).
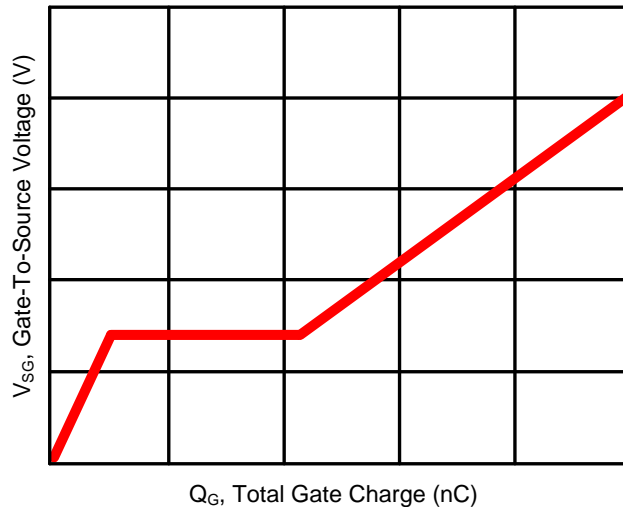

Figure 3. Power MOSFET Gate Drive Characteristics

1.2 *Bootstrap circuit Principle for High Side Gate Drive*

The gate drive requirements for a power MOSFET utilized as a high side switch, in applications like Full bridge, half-bridge converters or synchronous buck converters can be summarized as follows:

- Gate voltage must be 6 to 12V higher than the source voltage. To fully enhance a high side switch, the gate to source voltage would have to be higher than the threshold voltage plus the minimum necessary voltage to fully enhance the MOSFET

- The gate voltage must be controllable from the logic level, which are normally referenced to ground. Thus, the control signals need to be level shifted to the source terminal of high side MOSFET (HS node), which in most applications, swings between ground and the high voltage rail.

The Bootstrap supply technique is a simple, cost-effective way to power the upper MOSFET's gate and provide bias supply to the floating logic sections of the Gate Driver. Only two components (a Bootstrap diode and capacitance) per bridge phase are needed to implement the Bootstrap supply.
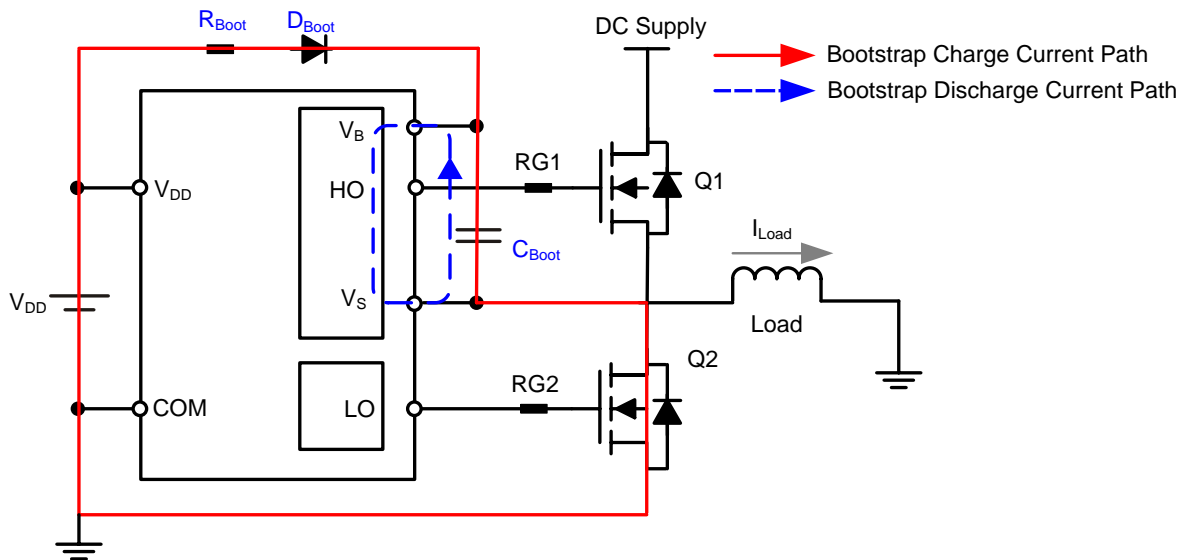
Figure 4. Bootstrap Supply Circuit

Using this circuit, the Bootstrap Capacitor is charged to ground through the Low side FET. When the Low side FET is turned off, the bottom of the capacitor flies up and this creates a voltage greater than Vcc. This voltage is applied to the High side gate driver.

1.3 Low Frequency 600VA to 3KVA Pure Sine Wave Inverter Design

There is a dual mode of operation in a residential Inverter ie Mains mode and Inverter mode. As shown in Figure 5, the Input AC voltage is fed to the transformer through a switch (relay). In the mains mode, when input AC is present and is within valid range, the switch is closed and the input AC directly goes to the output load. The same AC is fed to transformer, and the H-bridge consisting of MOSFETs or IGBTs are driven through microcontroller or DSP to charge the battery. A bridge less rectification principle is used to charge the battery by boosting the voltage produced in the transformer primary using the inductance of the winding, by switching the lower MOSFET banks. The lower MOSFET switches are switched and upper switches kept turned OFF, The body diodes of the upper MOSFETS will act as rectifiers. The pulse width of the switching pulses of the lower bank is proportional to the output charge current.
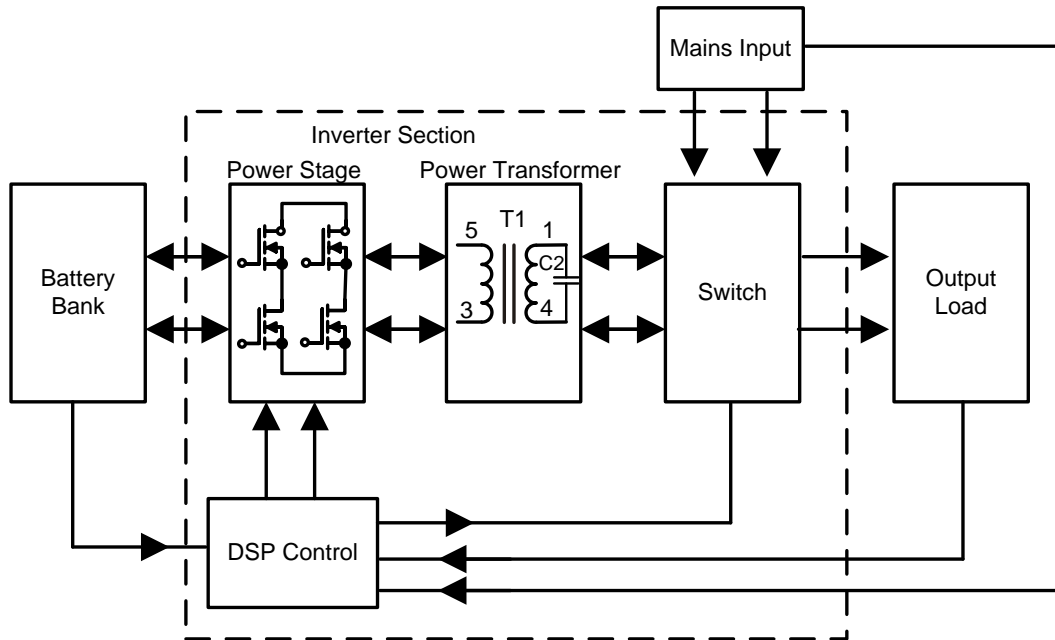
Figure 5. Inverter's Block Diagram

The DC/AC inversion can be achieved using any one of the two following methods.

The method in which the low voltage DC power is inverted, is completed in two steps. The first is the conversion of the low voltage DC power to a high voltage DC source, and the second step is the conversion of the high DC source to an AC waveform using pulse width modulation.

Another method to complete the desired outcome would be to first convert the low voltage DC power to AC, and then use a transformer to boost the voltage to 120/220 volts. The widely used method in the current residential inverter is the second one . Here if the AC fails or is out of valid range (AC Voltage Sense is required), the switch between Mains Input and Output Load opens. H-bridge circuit converts battery DC voltage into AC using high frequency PWM (5 kHz to 15 KHz) thus feeding the same transformer which is being used for charging in the mains mode. The output of transformer contains a capacitor which filters it to make 50 Hz AC.
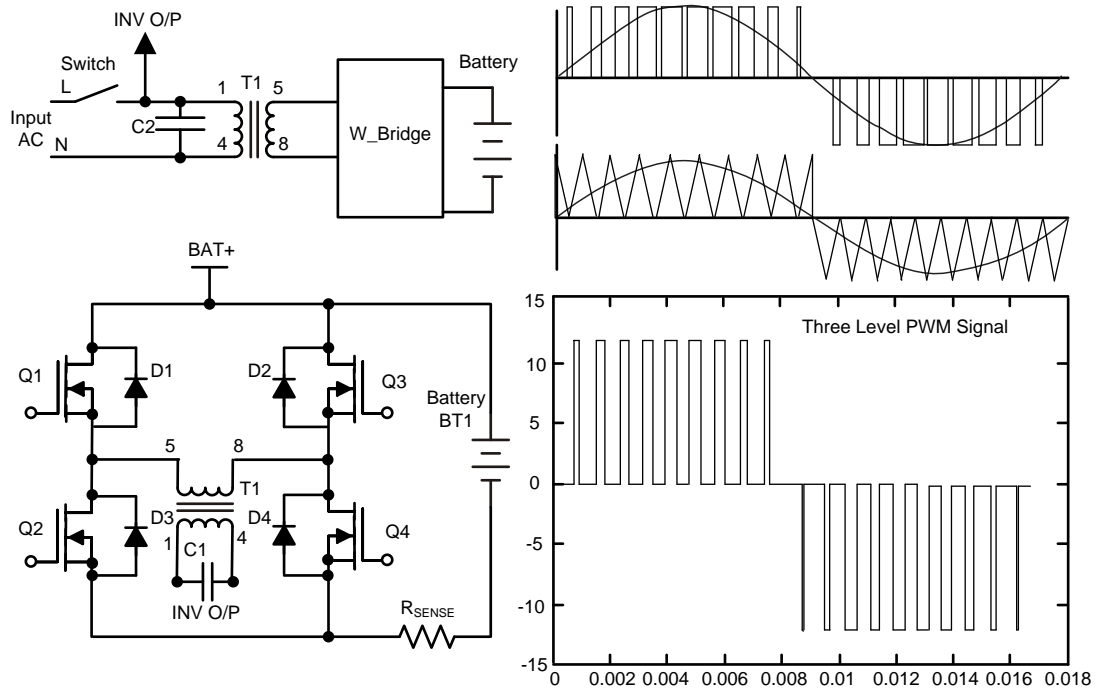
Figure 6. Gate Drive Inputs in Inverter Mode
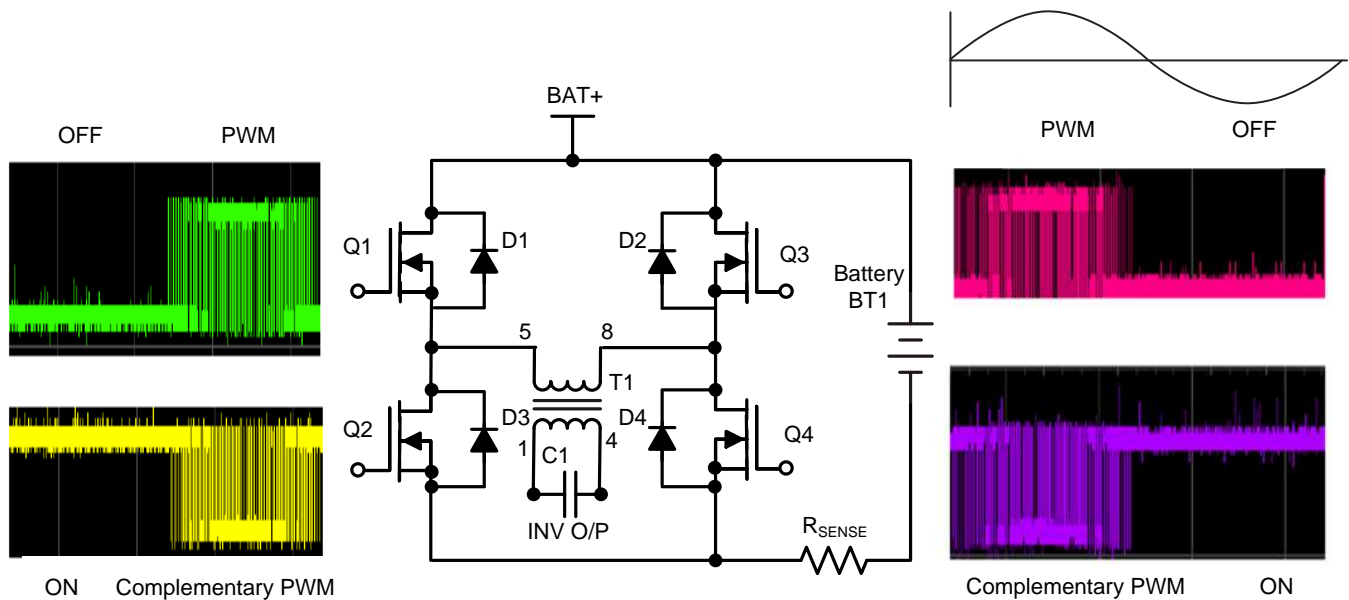
Figure 7. Inverter Mode Operation

For the Positive Half of the Sine Wave generation, Q2 is always high ,Q1 is always off , Q3 is applied with 6.4KHz (6.4KHz to 20KHz) PWM corresponding to Positive Half cycle 50Hz sine wave and Q4 is applied with corresponding complementary (to Q3) PWM . For the Negative Half 50Hz sine wave generation , Q4 is always high , Q3 is always off , Q1 is applied with 6.4KHz PWM corresponding to positive half cycle 50Hz sine wave and Q2 is applied with Q1's complementary PWM .

2   SM72295– Achieving High Integration in Current LF Inverter Design

The SM72295 is a full bridge MOSFET driver with 3A (higher no. of FETs in parallel for high power) peak current drive capability with

1. Integrated ultra fast 100V boot strap diodes (can easily support up to 5KVA rated inverters)
2. Two high side current sense amplifiers with externally programmable gain and buffered outputs which can be used for measuring the Battery charge and discharge current – Additional current sense amplifiers and buffers are not required
3. Programmable over voltage protection – which can be used for Charge complete detection or for driver shutdown feature in case of a fault condition
4. Can be directly interfaced with a microcontroller
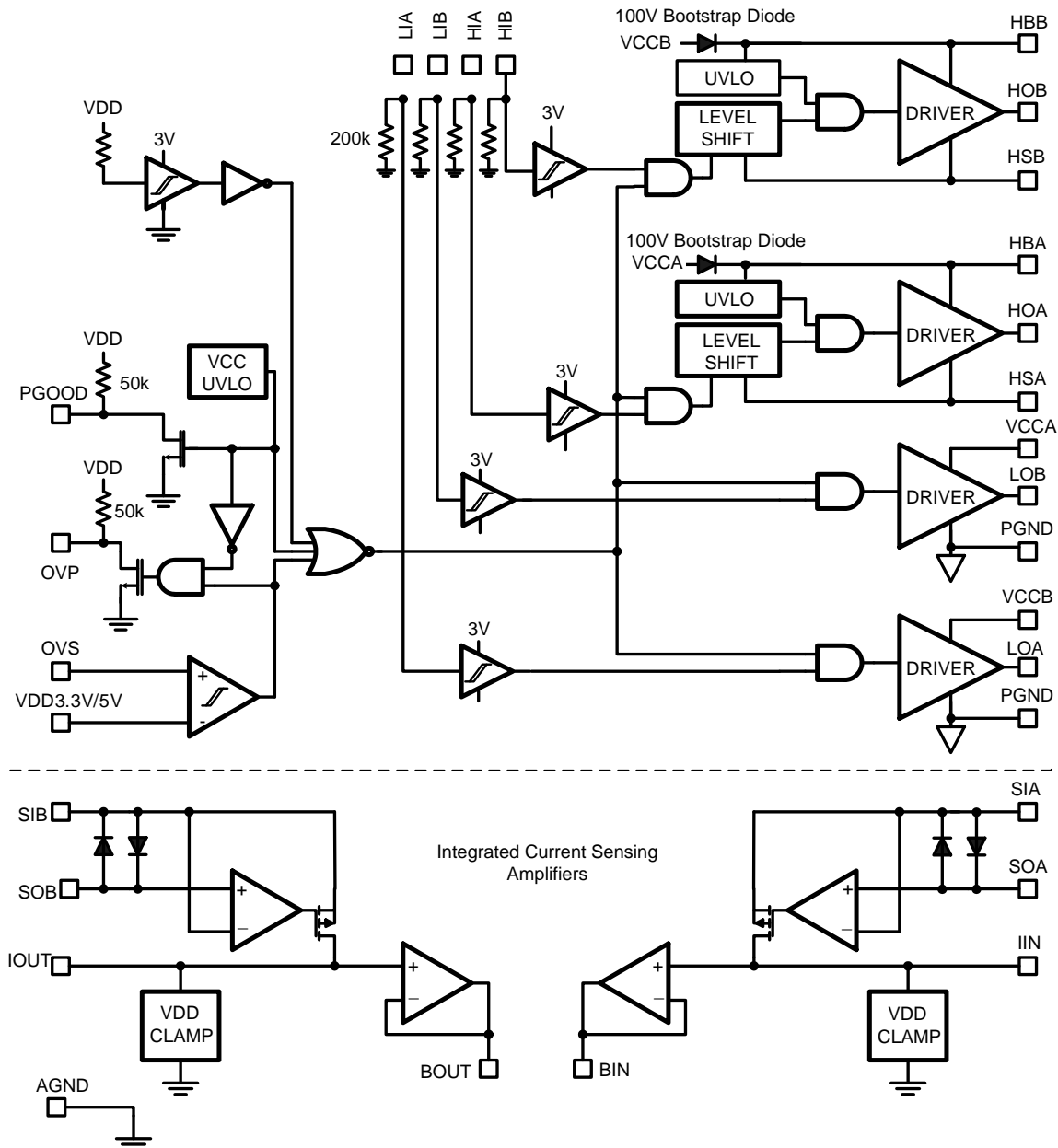

Figure 8. Block Diagram of SM72295 Gate Driver

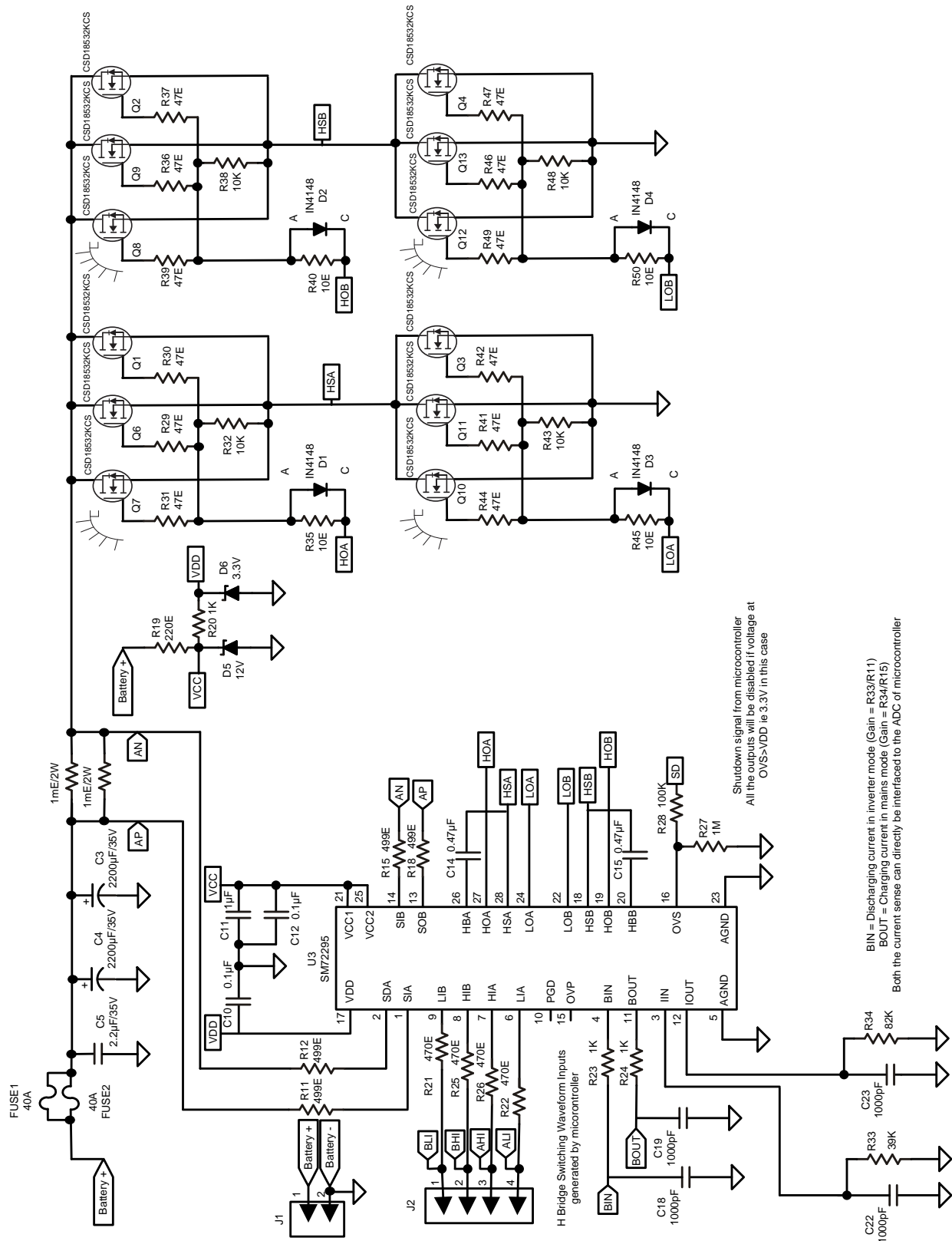## 2.1   Application Schematic — SM72295 in 800VA Pure Sine Wave Inverters

Figure 9. SM72295 in 800VA pure Sine Wave Inverters

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2.2 Easy Design Guidelines for Integrated Current Sensing

In the Inverter design, the charge current during the Mains mode and discharge current during the inverter mode is needed to be measured and given to the ADCs of microcontroller or DSP.

In SM72295, Current sensing is provided by two transconductance amplifiers with externally programmable gain and filtering to remove ripple current to provide average current information to the control circuit. The current sense amplifiers have buffered outputs available to provide a low impedance interface to an A/D converter.
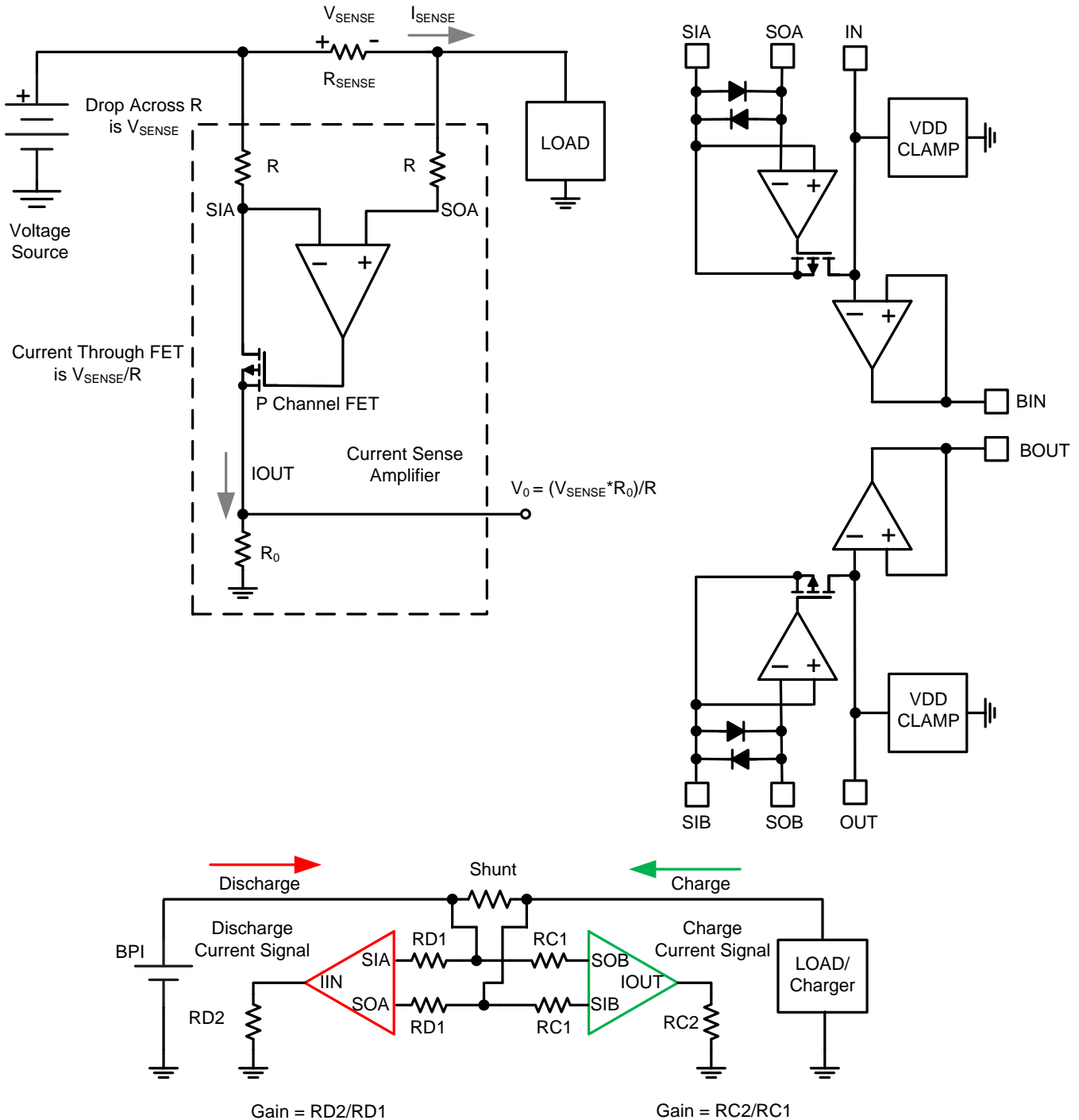

Figure 10. Integrated Current Sensing Amplifier

Hence the charge and the discharge current can easily be measured by giving individual gain to each of them. The charging current is generally pretty less than the possible Discharging current in 800VA Low Frequency inverter. The Maximum charging current for 150-165AH battery is close to 15A while the discharging current can goes upto 60A-70A.

2.2.1   Steps of Current Sense Design

1. Current Sense Resistance is chosen based on Max current and respective power dissipation on Current Sense resistance. In this Design, two 2W 1 milliohm resistances in parallel were chosen so that even at 70A Discharge current in Inverter mode, the power dissipation is 2.45W which is much lesser than allowed 4W(2W each of parallel 1milliohm Resistance).

2. There is VDD (3.3V) clamped at the Current Sense amplifier output and hence the gain should be maintained in such a way that the output is not clamped in the area of interest. The Discharge current gain is achieved through R33 / R11 (refer to application Schematic) which comes out to be the gain of 78 in this application. Even at 70A discharge current, the BIN= 2.73V which is lower than VDD clamp.

3. Since the Maximum Charge current in this application is close to 15A, the gain of this section is maintained higher through R34/R15 ratio.

2.3   Layout Guidelines

The optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. Low ESR / ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak currents being drawn from VDD during turn-on of the external MOSFET.

2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (VSS).

3. In order to avoid large negative transients on the switch node (HS pin), the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.

4. Grounding Considerations

   (a) The first priority in designing Grounding Consideration is a part in layout Guidelines. connections is to confine the high peak currents that charge and discharge the MOSFET gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.

   (b) The second high current path includes the Bootstrap capacitor, the Bootstrap diode, the local ground referenced bypass capacitor and low-side MOSFET body diode. The Bootstrap capacitor is recharged on a cycle-by-cycle basis through the Bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

3   Test Results in 850VA Pure Sine Wave Inverter Applications

3.1   Inverter Mode

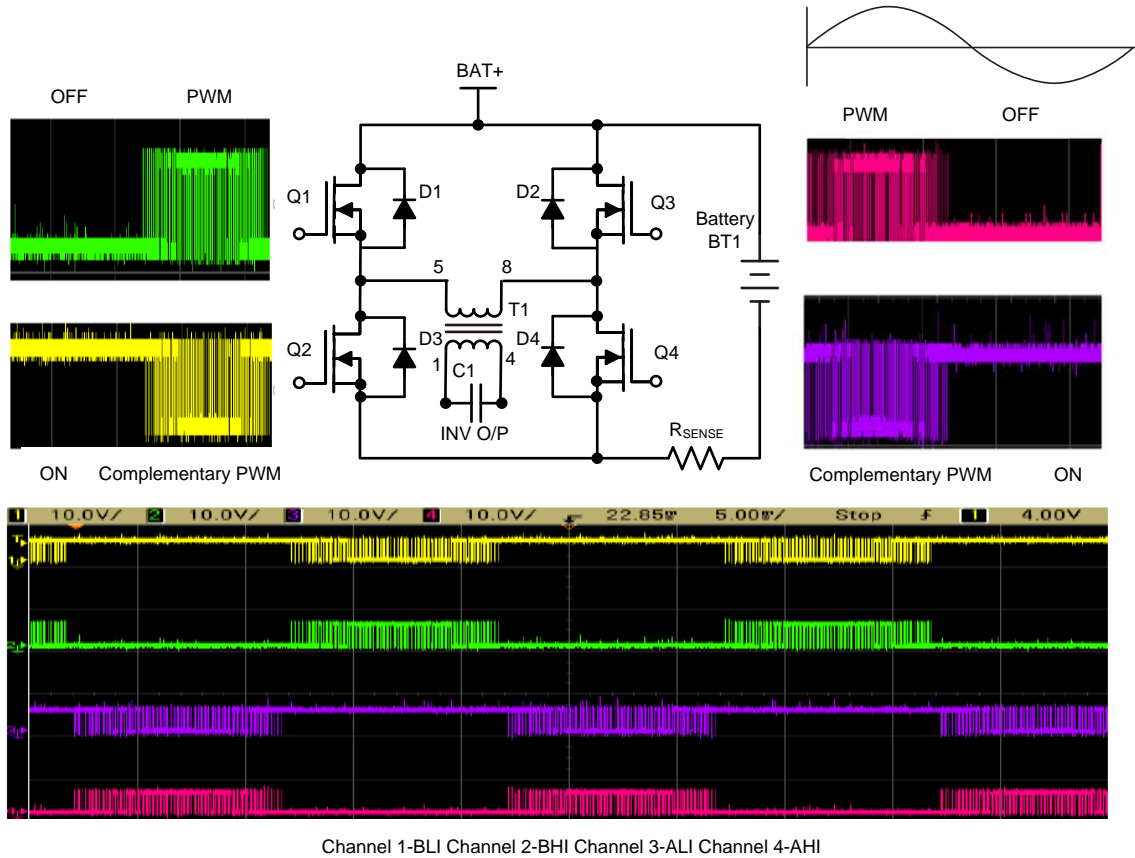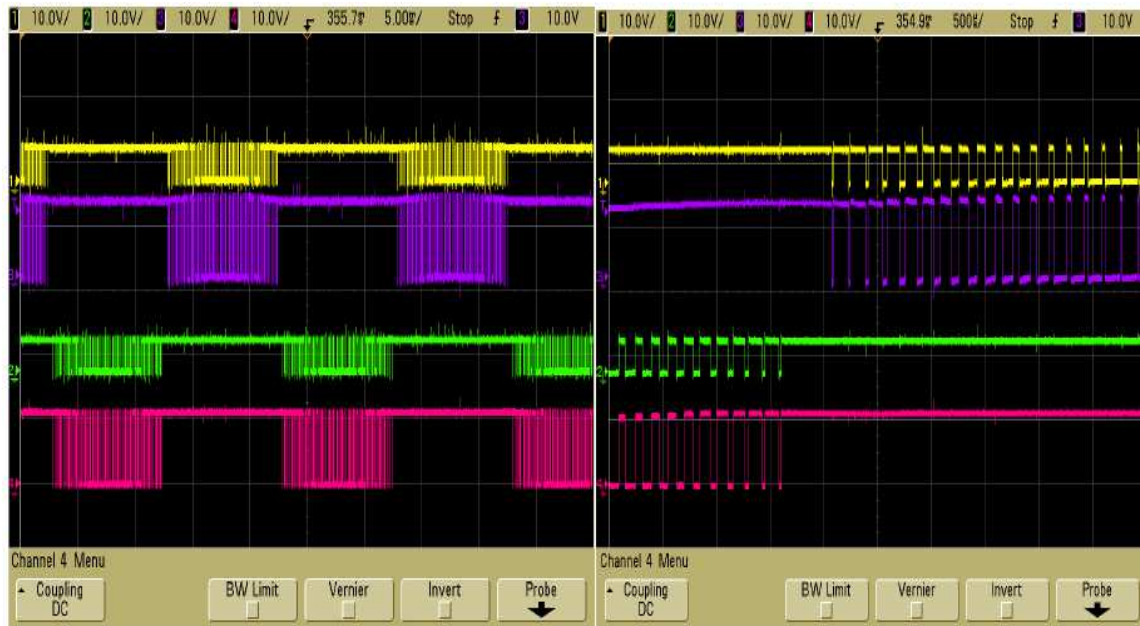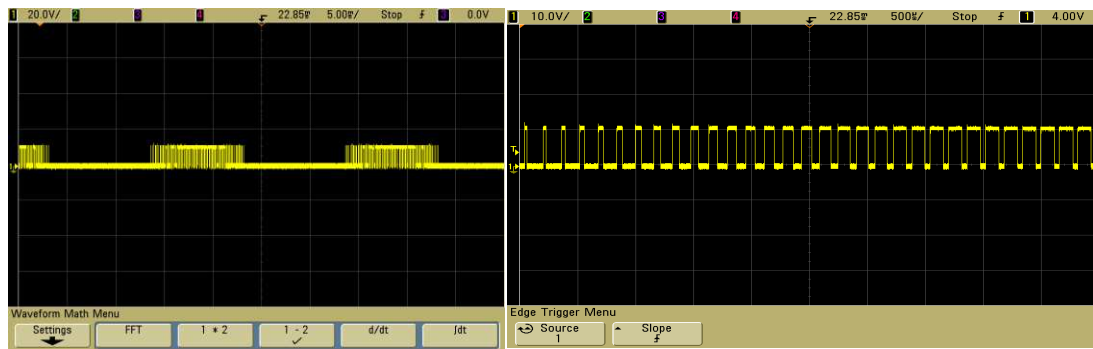Channel 1-BLI Channel 2-BHI Channel 3-ALI Channel 4-AHI

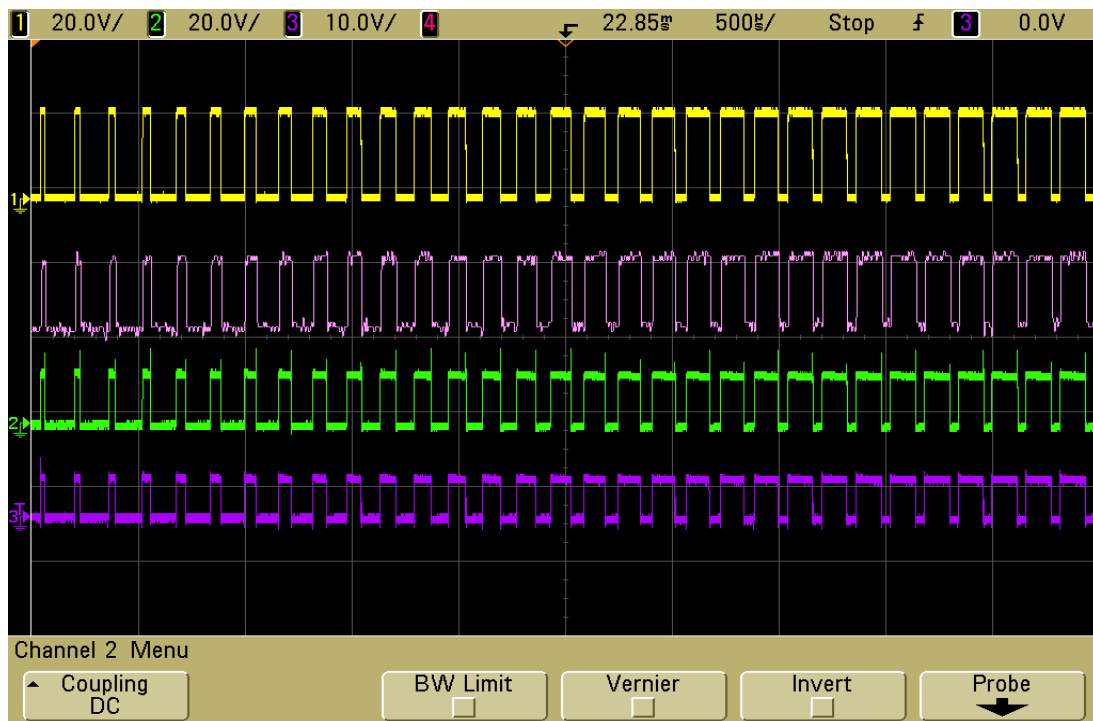**Figure 11. Inputs to Gate Driver in Inverter Mode with Load of 700VA**

Channel 1-ALI Channel 2-ALO Channel 3-BLI Channel 4-BLO

Figure 12. Signal Integrity from Input to Output Gate Drives in Low Side MOSFETs on 700VA Load in Inverter Mode.
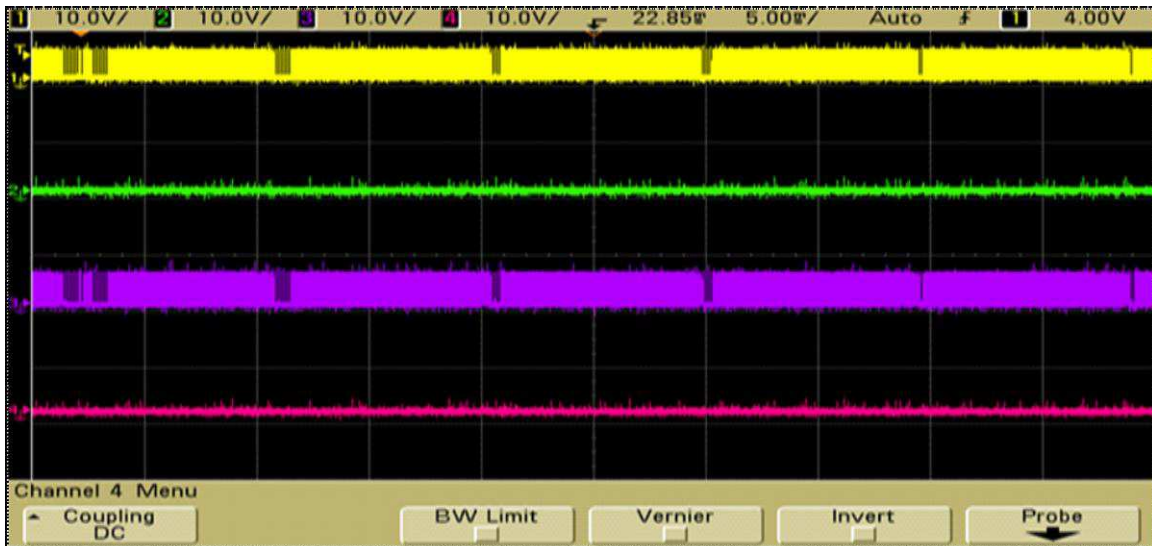
Channel 1- Probe Across BHO and BHS

Channel 1- BHO Channel 2-BHS Channel 3- BHI Channel between 1 and 2 – Maths 1-2 for VGS

Figure 13. Signal Integrity from Input to Output Gate Drives in High Side MOSFETs on 700VA Load in Inverter Mode

3.2 Charger Mode/Mains Mode

1. During Mains mode, the same transformer which is used in DC/AC inversion by boosting battery voltage to line voltage in inverter mode, is connected to the mains power using a relay. A bridge less rectification principle is used to charge the battery by boosting the voltage produced in the transformer primary using the inductance of the winding, by switching the lower MOSFET banks..

2. The lower MOSFET switches are switched and upper switches kept turned OFF, The body diodes of the upper MOSFETS will act as rectifiers. The pulse width of the switching pulses of the lower bank is proportional to the output charge current.
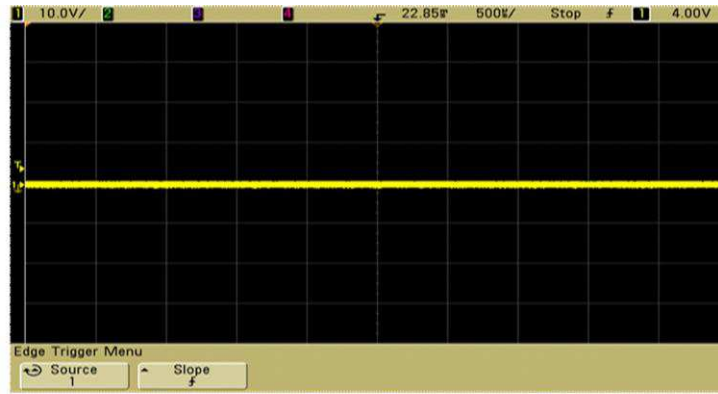
Channel 1 – BLI Channel 2-BHI Channel 3-ALI Channel 4-AHI

Figure 14. Inputs to Gate Driver in Mains Mode With AC Mains Input of 220V
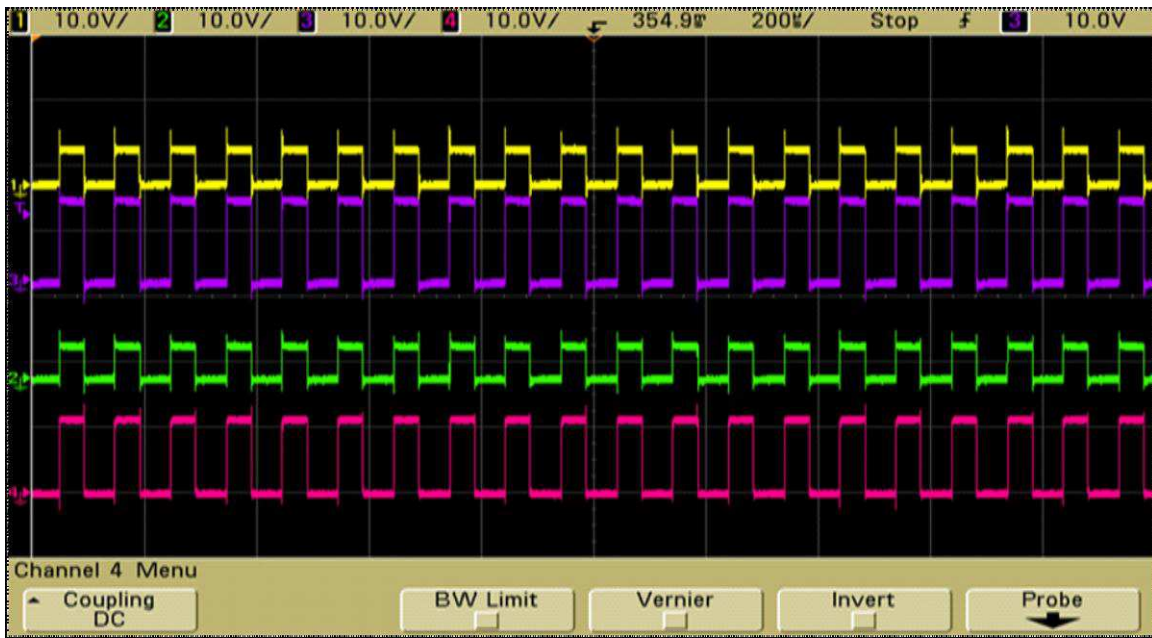
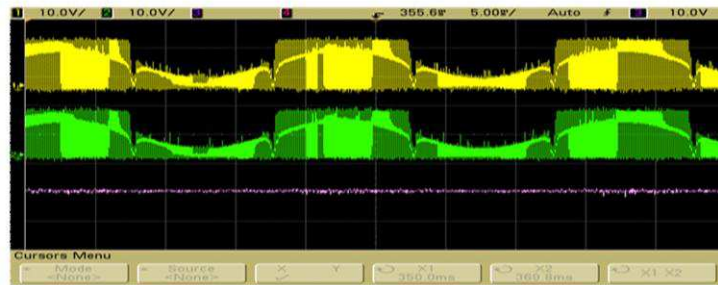Channel 1-BLI Chanel 2-BLO Channel 3-ALI Channel 4-ALO

Figure 15. Signal Integrity from Input to Output Gate Drives in Low Side MOSFETs in 220V AC Mains Mode.

Channel 1: Probe across BHO and BHS

Channel 1-BHO Channel 2-BHS Channel 3-Math 1-2 for VGS

Figure 16. Signal Integrity from Input to Output Gate Drives in High Side MOSFETs in 220V AC Mains Mode.

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