LM26400Y

Powering Multi-Rail Systems Using the LM26400Y Regulator

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ANALOG edge℠

Powering Multi-Rail Systems Using the LM26400Y Regulator

Application Note AN-1703

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Today's electronic systems typically have multiple DC voltage rails that are powered by point-of-load regulators. The input rail to these regulators can be an AC adapter, an intermediate bus, a battery, or a USB power rail. Often it is desirable to find a power solution that can handle a relatively wide input range, is reasonably integrated, and simple to use. National Semiconductor's LM26400Y dual buck switching regulator addresses such applications. It has an operating input voltage range of 3V to 20V and a guaranteed maximum duty cycle of 90% so it is able to handle a large range of step-down conversions. The LM26400Y device has integrated power FETs and internal-loop compensation. The two packages offered, TSSOP and LLP, have an exposed pad that allows unimpeded heat flow from the die to the PCB surface.

Many Features Enable Flexibility

Figure 1 is a simplified block diagram of the LM26400Y regulator. The device features separate soft-start, enable pins, and internal bootstrap diodes. Sequencing of the regulator can be controlled by toggling the enable pins at different times or slewing the soft-start pins at different rates. The integrated bootstrap diodes can simplify designs when a bootstrap bias is not readily available in the system. The two channels switch at the same 500 kHz frequency but are 180° out of phase, reducing the AC current in the input capacitors.

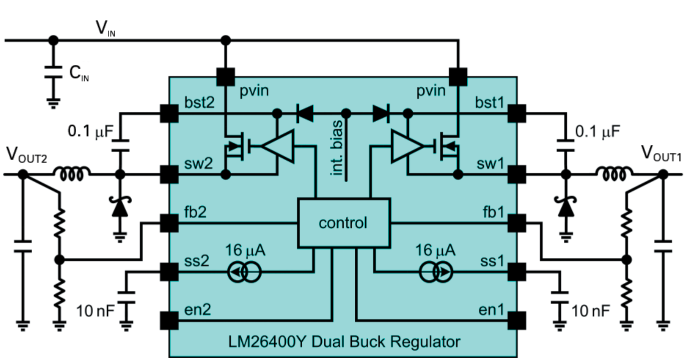

Figure 1. Simplified View of the LM26400Y Regulator

FPGA Power-Up

In this article, the LM26400Y is powering a popluar FPGA off of an input voltage range of 4.75V to 13.2V. The example uses an FPGA-based subsystem that has six functions in the chip that need power as listed below:

Supply	Function	Voltage
VCCINT	Core	1.2V
VCCAUX	Auxiliary	2.5V
VCCO_0-3	4 I/O Banks 0-3	1.2/1.5/1.8/2.5/3.3V

To interface effectively with different output buffer standards, the four I/O banks can work at five different voltage levels.

To design a power supply solution for the FPGA, more must be known about the application. The power required by the six functions in the chip can vary dramatically depending on the utilization ratio. The power estimation tool provided by the FPGA vendor translates the usage scenario into terms a power designer can readily utilize:

	VCCINT	VCCAUX	VCCO_0	VCCO_1/2/3
Voltage	1.2V	2.5V	2.5V	3.3V
Current	1.75A	0.62A	1.41A	1.27A

VCCAUX and VCCO_0 are the same voltage level and could share a voltage regulator. However, in this case, VCCO_0 needs to power up separately to satisfy peripheral device sequencing, and thus a total of four voltage rails are employed.

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All four rails may ramp up independently of each other as long as they reach their nominal voltage levels within 0.2 ms to 50 ms in a monotonic fashion. The only potential concern to meet that requirement is VCCINT. According to the datasheet, if VCCINT comes up earlier than VCCAUX, there can be a surplus current (366 mA typical) on the VCCINT rail which appears somewhere after VCCINT hits 0.5V.

The board hosting the FPGA is to be plugged into two kinds of systems, one supplying an input of 12V +/-10%, the other an input of 5V +/-5%. The FPGA voltage regulators need to handle an input range from 4.75V to 13.2V. A linear solution is not an option due to the unacceptable power losses which are worst at the 12V input.

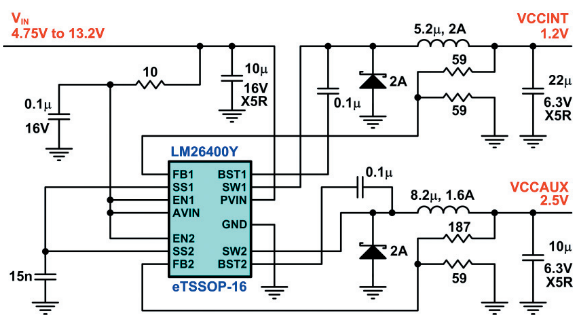

Figure 2. FPGA Power - VCCINT and VCCAUX

Based on the estimates above, plus some safety margin (because those numbers are just estimates), two switchers are required of up to 2A each for VCCINT and VCCO_0, one switcher of approximately 1A for VCCAUX and one switcher of approximately 1.5A for VCCO_1, VCCO_2, and VCCO_3 combined. One LM26400Y regulator can be used to generate VCCINT and VCCAUX and another to generate the I/Os. The schematic for the VCCINT (1.2V) and VCCAUX (2.5V) supply is shown in *Figure 2.*

The startup behavior is shown in *Figure 3.* Although the two channels share a 15 nF soft-start capacitor, VCCAUX will rise twice as fast as VCCINT due to the greater voltage-divider ratio. This allows the power designer to avoid the surplus current of a few hundred milliamps mentioned above.

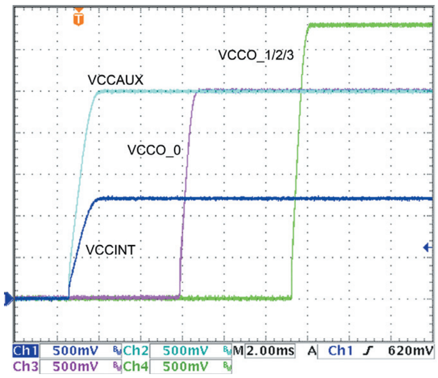

Figure 3. FPGA Solution - Startup

Regarding the other two FPGA rails, the VCCO_0 (2.5V) circuit uses the same design as VCCAUX as does the VCCO_1/2/3 (3.3V) circuit except for the upper feedback resistor. The enable pins of the VCCO circuits are not tied to the input voltage due to the potential sequencing requirement of peripheral devices. Two separate ON signals are generated by the system to turn on the VCCO circuits independently. They also have separate soft-start capacitors which are 15 nF each.

This design has been bench verified with the typical efficiency of the VCCO_1/2/3 regulator shown in *Figure 4*.

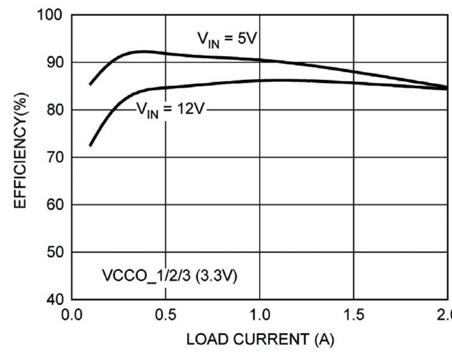

Figure 4. FPGA Solution - Efficiency

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