AN-2148 LM5051MAEVAL Evaluation Board

1 Introduction

The LM5051 evaluation board is designed to demonstrate the capabilities of the LM5051 OR-ing diode controller. One low-side N-channel power MOSFET is used per channel. The LM5051 evaluation board schematic is shown in Figure 7. The evaluation board is designed to highlight applications with a small solution size. For more information about LM5051 functional and electrical characteristics, see the *LM5051 Low Side OR-ing FET Controller Data Sheet* (SNVS702).

2 Operating Range

- Input Voltage: 48V
- Output Current Range: 0A to 5A
- Ambient Temperature Range 0°C to 50°C
- Board Size 2.25 inches x 2.60 inches

To aid in the demonstration and evaluation of low-side OR-ing diode controller solution based on the LM5051.

The load current capability is limited at 5A by the ratings of the MOSFETs, the banana jacks, and the PCB copper area and weight. The PCB layout has not been tested for currents above 5A, so this should only be done with some degree of caution.

The maximum input voltage is limited by the breakdown voltage rating of the two input protection diodes (D1,D2), and the breakdown voltage rating of the output protection diode (D4).

Typical evaluation board performance and characteristics curves are shown in Figure 2 through Figure 3. The PCB layout is shown in Figure 9 and Figure 10. An on-board push-button switch invokes the FET test mode on both channels simultaneously, while individual test points are provided for monitoring the FET test status output.

3 Evaluation Board Start-Up

Before applying power to the LM5051 evaluation board, all external connections should be verified. The external power supplies must be turned off and connected with proper polarity to the INPUT A+/B+ and INPUT A-/B- terminals. A common load is connected to the 48V+ OUT and 48V- OUT terminals.

The evaluation board will be in the normal operating mode when power is applied.

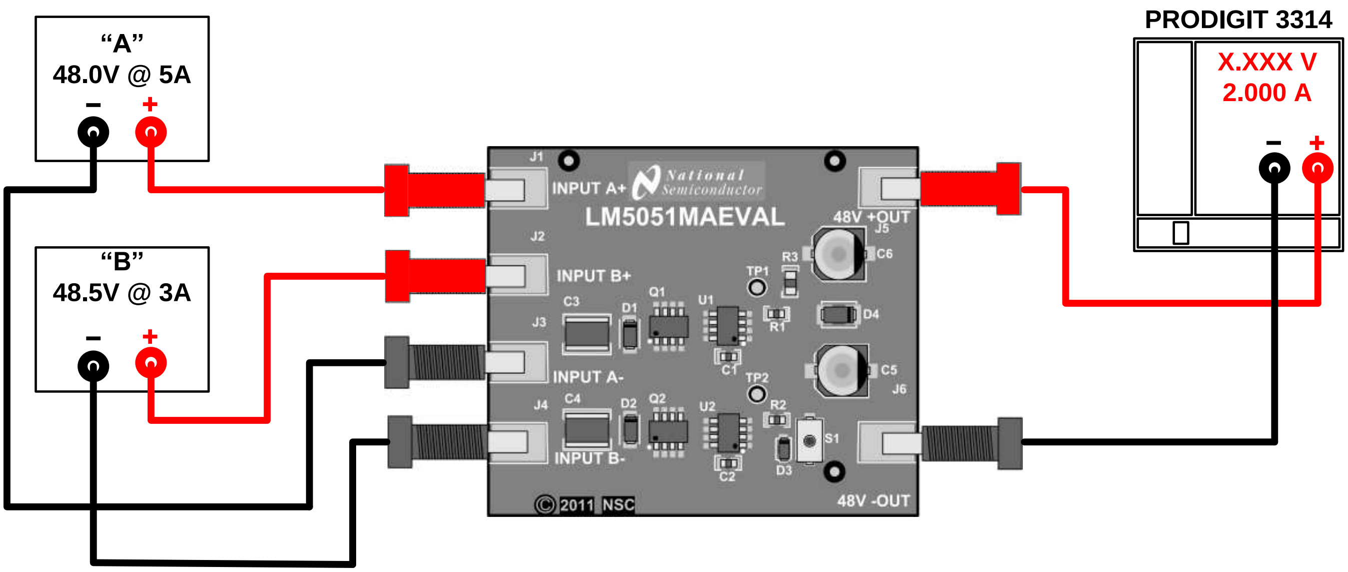


Figure 1. Typical Board Connections

4 Inductive Kick-Back Protection

Diode D1 and capacitor C3 serve as inductive kick-back protection to limit negative transient voltage spikes generated on the input when the INPUT A supply voltage is abruptly taken to zero volts. Diode D2 and capacitor C4 serve the same protective function on the INPUT B supply voltage.

Diode D4 and capacitors C5/C6 serve as inductive kick-back protection to limit positive transient voltage spikes generated on the output when an input supply voltage is abruptly taken to zero volts.

5 OR-ing Transfer

An example of OR-ing transfer is shown in Figure 2. In this example one 48.5V supply (INPUT B) is powering a 2A load at the output, while a 48.0V supply (INPUT A) is connected, but is idle. The OR-ing transfer begins when the 48.5V supply is shorted (INPUT B- is shorted to INPUT B+). This short causes reverse current through the MOSFET (Q2) and creates the required voltage ($V_{SD(REV)}$+ $\Delta V_{SD(REV)}$) on the LM5051 INN pin (U2) that will immediately cause the discharge the gate of the Q2 MOSFET.

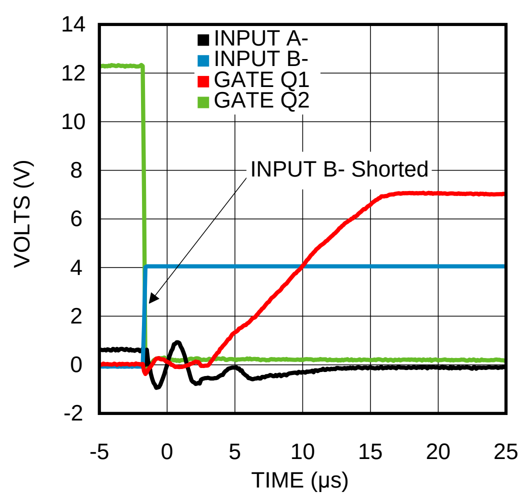


Figure 2. Forward and Reverse Waveforms

With Q2 off, the output voltage will fall until it is just below the second supply voltage by the $V_{SD(REV)}$ threshold voltage. When this happens, the gate of the MOSFET (Q1) will begin charging from the LM5051 (U1). Note that the Q1 gate voltage may not rise all the way to the maximum voltage, since the $V_{SD(REG)}$ threshold will needs to be exceeded for that to happens, see Figure 3. The gate voltage may initially settle at some intermediate value and then slowly rise as internal heating of the MOSFET causes the $R_{DS(ON)}$ to rise which, in turn, causes the drain to source voltage to rise and, in response, the LM5051 increases the gate voltage in an effort to keep the drain to source voltage regulated.

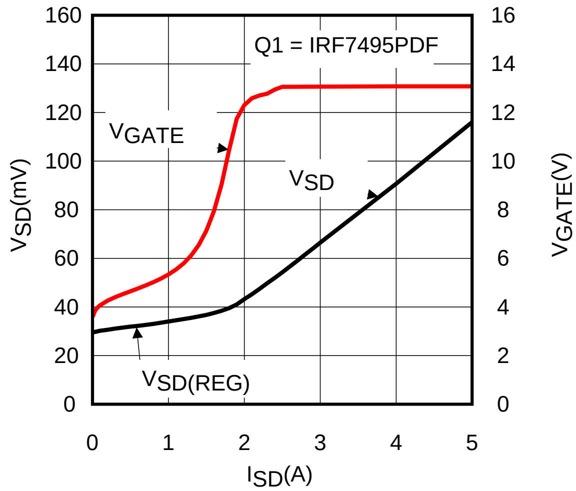


Figure 3. Gate Drive vs Drain to Source Voltage

6 Off TEST Push-Button, S1

The single push-button (S1) provided on the LM5051 evaluation board is used to control the operation of both LM5051 devices. The LM5051 Eval board has an on-board 5V (with respect to the 48V- OUT terminal) reference that is used to drive the OFF pins of both LM5051 devices to shut down the gate drives, as well as provide a voltage bias for the nFGD status output pins. For more details, see the *LM5051 Low Side OR-ing FET Controller Data Sheet* (SNVS702).

In normal operation, the LM5051 OFF pin is left open. The LM5051 internal OFF pin pull-down will ensure that both of the LM5051 devices are operating in the default active mode.

To disable both LM5051 devices, simply press the TEST push-button. Typical behavior is shown in Figure 4 and Figure 5.

The typical OFF behavior is shown in Figure 4. Pressing the TEST button applies approximately 5V to the OFF pin of both LM5051 devices. After the OFF pin rises above the $V_{OFF(IH)}$ threshold the MOSFET gate will be quickly discharged. As the gate discharges, the voltage across the MOSFET drain to source pins will increase. Since all measurements are referenced to the LM5051 INP/VSS pin, the INN pin will appear to be going negative. When the INN pin has gone more negative than the $V_{SD(TST)}$ threshold (typically - 260mV), the nFGD pin go low. The INN pin voltage will be clamped at about -600mV by the MOSFET body diode.

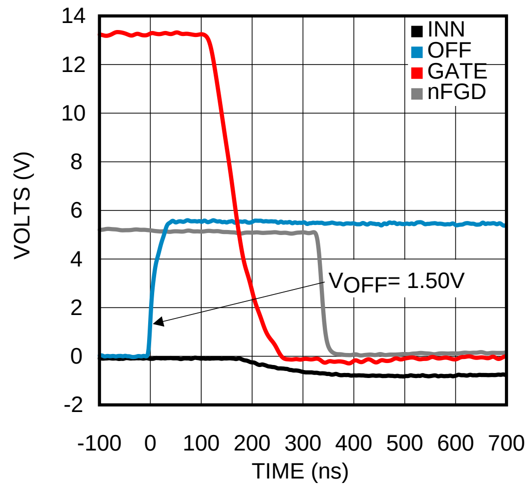


Figure 4. OFF pin Going High, Gate OFF

Typical behavior when the TEST button is released is shown in Figure 5. In this case, the OFF pin relies on the internal pull-down (typically 4.6 µA) to discharge any stray capacitance, as well as the probe capacitance. Once the OFF pin has fallen below the $V_{OFF(IL)}$ threshold, the gate drive circuitry will become active. Since, in this case, the INN pin is well below the $V_{SD(REV)}$ threshold the MOSFET gate will immediately begin charging. As the gate voltage increases the INN pin voltage will fall below the $V_{SD(TST)}$ threshold and the nFGD pin will go high. Note that the gate voltage may not rise all the way to the maximum voltage, since the $V_{SD(REG)}$ threshold needs to be exceeded for that to happen, see Figure 3. The gate voltage may initially settle at some intermediate value and then slowly rise as internal heating of the MOSFET causes the $R_{DS(ON)}$ to rise which, in turn, causes the drain to source voltage to rise and, in response, the LM5051 increases the gate voltage in an effort to keep the drain to source voltage regulated at the $V_{SD(REG)}$ threshold.

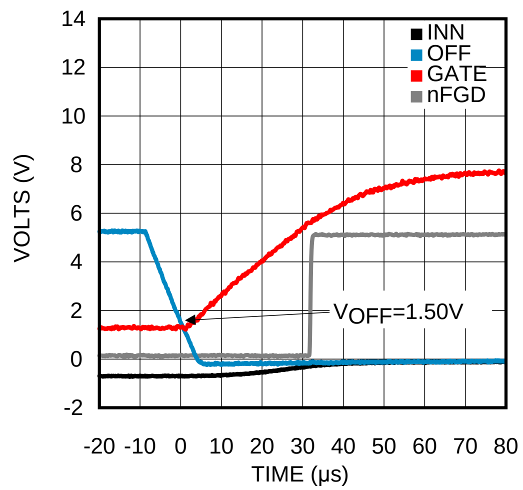
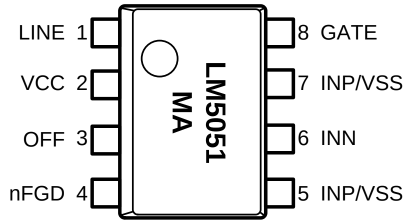


Figure 5. OFF pin Going Low, Gate Drive Active



Device Pin 5 is internally connected to Device Pin 7

Figure 6. Connection Diagram

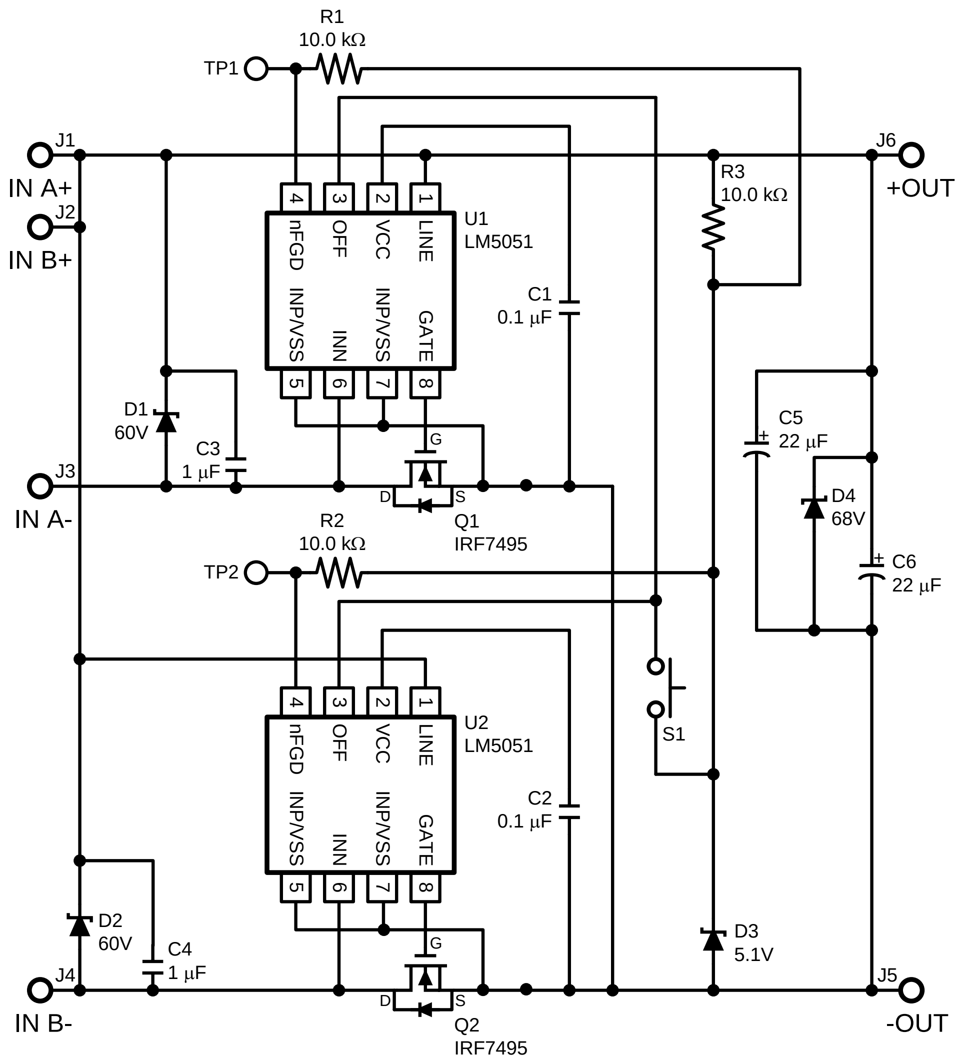


Figure 7. Schematic Diagram

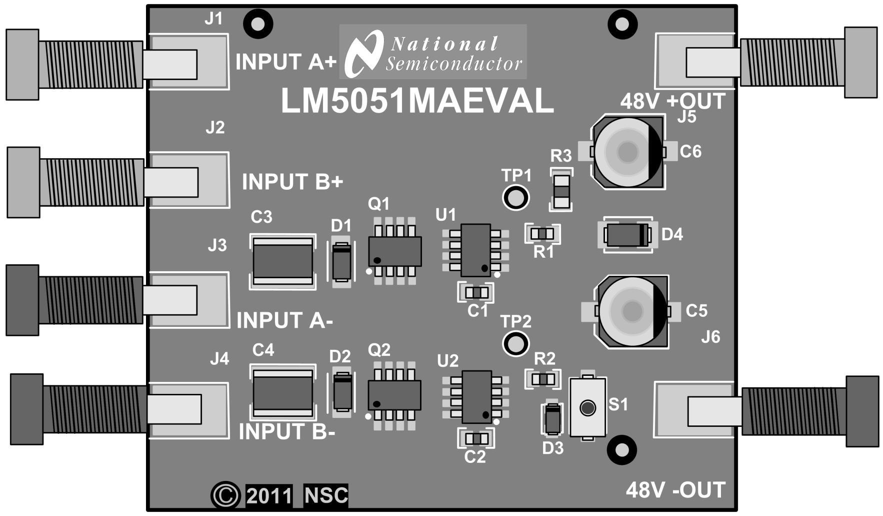


Figure 8. Component Placement

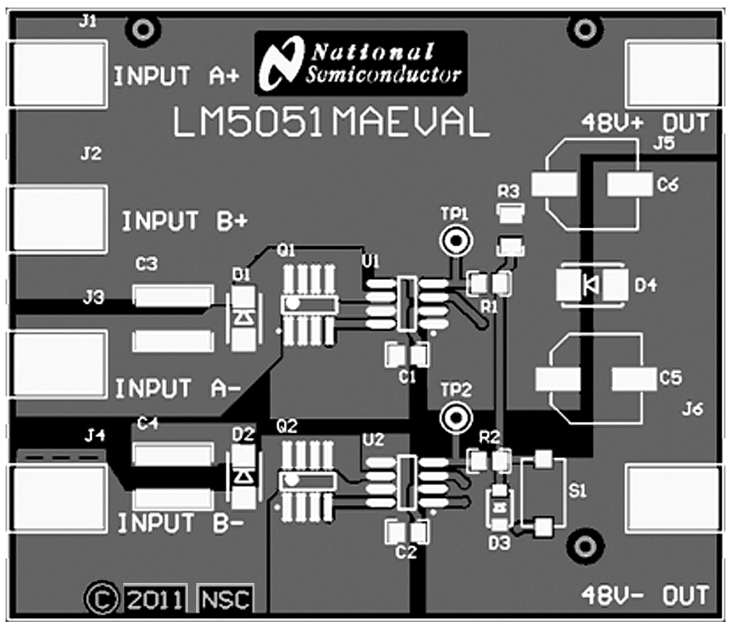


Figure 9. Evaluation Board, Top Side (Component)

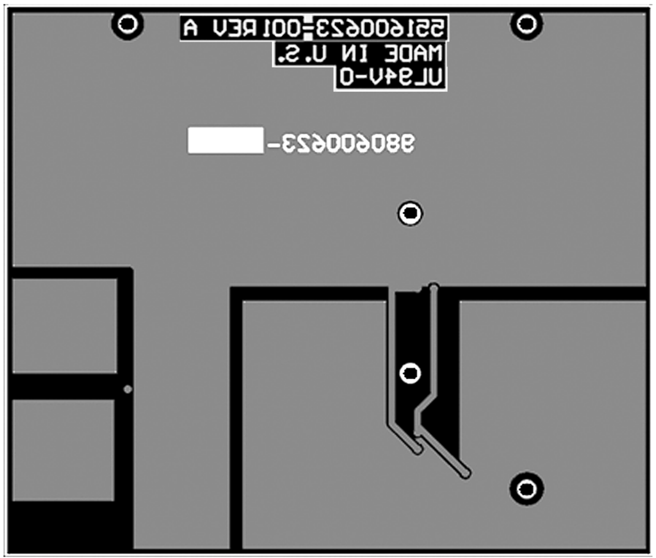


Figure 10. Evaluation Board, Bottom Side

7 Bill of Materials (BOM)

ID	Description	Manufacturer	Mfgr Part Number
U1, U2	IC; Ideal OR-ing Diode Controller	Texas Instruments	LM50501
C1,C2	Capacitor, 0.1uF, Ceramic, ±10%, 25V, X7R, 0805	AVX Corporation	08053C104KAT2A
C3,C4	Capacitor: MLCC; 1.0µF; ±10%; 100V; X7R; 1825	Vishay/Vitramon	VJ1825Y105KBBAT4X
C5, C6	Capacitor: 22 µF; ±20%; 100V; Aluminum Electrolytic; SMT	Panasonic/ECG	EEE-FK2A220P
D1, D2	Diode: Schottky Barrier Rectifier; 1A: 60V; SMA	ON Semiconductor	SS16T3G
		Micro Commercial Components	SS16-TP
D3	Diode: Zener, 5.1V, 500mW, SOD-123	ON Semiconductor	MMSZ4689T1G
D4	Diode: Zener, 68V, 3W, SMB	ON Semiconductor	1SMB5945BT3G
J1, J2, J5	Jack: Standard Banana, Insulated, Red	Keystone Electronics	6091
J3, J4, J6	Jack: Standard Banana, Insulated, Black	Keystone Electronics	6092
Q1, Q2	MOSFET N-CH, 100V 0.018Ω, 7.3A SO-8	International Rectifier	IRF7495PDF
R1, R2	Resistor: 10.0 kΩ, ±1%, 0.125W, 0805, Thick Film	Vishay/Dale	CRCW080510K0FKEA
R3	Resistor: 10.0 kΩ, ±1%, 0.250W, 1206, Thick Film	Vishay/Dale	CRCW120610K0FKEA
S1	Switch, SPST-NO, Momentary, Tactile, SMD	C&K Components	KSR221GLFS
TP1, TP2	Test Point Terminal: Miniature, 0.040in Dia Mtg Hole; White	Keystone Electronics	5002

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265