Application Report
SNVA411A–November 2009–Revised May 2013

# AN-1997 Error Amplifier Limitations in High Performance Regulator Applications

*Timothy Hegarty*

**ABSTRACT**

The development of realistic predictions to assist the power supply engineer during the control loop design process is facilitated in this application report by appropriate small-signal and bode plot analysis, the validity of which is verified through simulation results.

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## 1 Introduction

The specification of load current transient response at the output of a power supply is subject to requirements related not only to the load transient demand itself – specifically load current step magnitude and slew rate – but also to the characteristics of the power supply. In general, the voltage regulator control loop design constitutes an important element and when fast transient response is required with minimal output voltage deviation, one essential rule generally applies: high control loop crossover frequency. The trend in the industry for high performance power supplies with elevated switching frequencies continues apace. Proportionately higher loop crossover frequencies are necessary in part to keep pace with the escalating load transient slew rate demands and in part to reduce the required number and size of relatively expensive reactive filter components.

The popularity of voltage mode control and its multiplicity of variants, pervasive in step-down (and, to a lesser extent, step-up) power converters, has placed particularly significant burden on the voltage loop error amplifier (EA) as it provides the compensating gain contribution to mitigate the rapid falloff in gain related to the complex double pole of the LC filter components. Current mode controlled parts present a single-pole response and their amplifier requirements vis-a-vis voltage mode are not as stridently demanding.

Most considerations of loop compensation pay scant attention to the effects of error amplifier performance characteristics, specifically gain-bandwidth product (GBW), open-loop DC (or low frequency) gain and phase margin. The error amplifier is usually implemented as an op-amp IC or integrated in a PWM controller or regulator-based solution. The GBW and DC gain parameters are typically specified in the associated device-specific data sheet.

In turn, it becomes imperative to seek an assessment of the intricacies associated with operation at high control loop crossover frequencies with limited error amplifier bandwidth, a condition where the EA can likely induce an exigent component of phase lag that presages a dramatic impact to overall system stability. Tangible design guidelines are outlined by reference solely to the compensator stage crossover frequency.

## 2 Power Supply Control Loop Review

The generalized schematic of a single channel synchronous buck regulator using voltage mode PWM control and a voltage mode compensation (VMC) circuit is embodied in Figure 1. Noteworthy is the conventional op-amp type voltage error amplifier that represents the sine qua non of the control loop structure. The finite input and feedback circuit impedances are denoted $Z_i$ and $Z_F$, respectively.

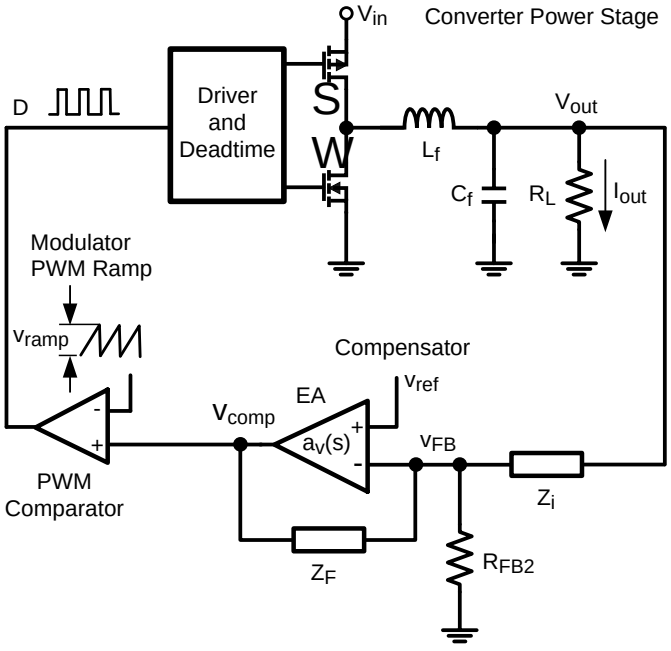


**Figure 1. Schematic of a Buck Converter Power Train and Voltage Mode PWM Control Loop Structure**

The scaled representation of the output voltage at the EA inverting input, usually termed the feedback (FB) node, is compared to a reference voltage, vref, and a compensated error voltage, vcomp, is generated at the compensation node. This error signal, typically designated COMP, is compared to a ramp voltage at the PWM comparator such that a change in COMP leads to a commensurate change in PWM duty cycle for the power stage. The ramp carrier signal is typically an increasing saw-tooth, decreasing saw-tooth or symmetrical triangular waveform to enable trailing-edge, leading-edge, or double-edge PWM modulation strategies, respectively.

## 3 Error Amplifier Review

Define the small signal EA transfer function in the s-domain as the incremental ratio of the amplifier's output voltage to its differential input voltage.

$$a_v(s) = \frac{\hat{v}_{comp}}{\hat{v}_{ref} - \hat{v}_{FB}}(s) \tag{1}$$

The inference here is that the small-signal perturbations of the parameters in Equation 1 are sufficiently small such that amplifier saturation, dynamic non-linearities, and slew-rate limiting are avoided, even at high frequencies.

Practical power supply control loop error amplifiers are usually realized using two stages – a transconductance stage followed by a gain stage [1]. The designs are normally lag compensated internally by one low frequency dominant pole that rolls off the open-loop gain and one high frequency pole located at or after crossover. Parasitic poles and zeroes typically appear in the forward path but are either cancelled or located at such high frequency that their consideration is superfluous. Thus, an open-loop EA small-signal transfer function can naturally be represented by

$$a_v(s) = \frac{A_{VOL}}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \tag{2}$$

$A_{VOL}$ is the open-loop DC or low frequency gain for a given supply rail voltage, ambient temperature, and load impedance. $\omega_{p1}$ and $\omega_{p2}$ represent the dominant pole and high frequency pole locations, respectively. The representative bode plot is encapsulated in Figure 2 using MathCad software. In this example, the DC gain, GBW, -3dB frequency, and phase margin values are 70dB, 10 MHz, 3.1 kHz, and 50°, respectively. The EA pole locations are marked by a + symbol on the gain curve in Figure 2.

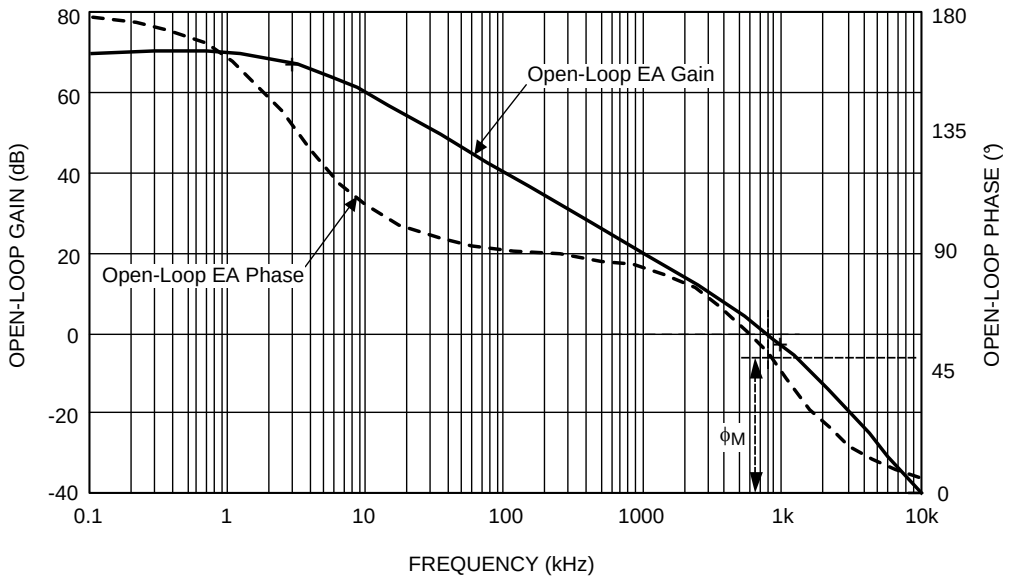


**Figure 2. Open-Loop EA Gain and Phase versus Frequency**

Of course, error amplifiers are seldom configured open-loop. By externally closing the loop around the amplifier, the DC gain can be advantageously traded off for -3dB bandwidth, as illustrated by the amplifier open-loop and closed-loop bode plots of Figure 3.

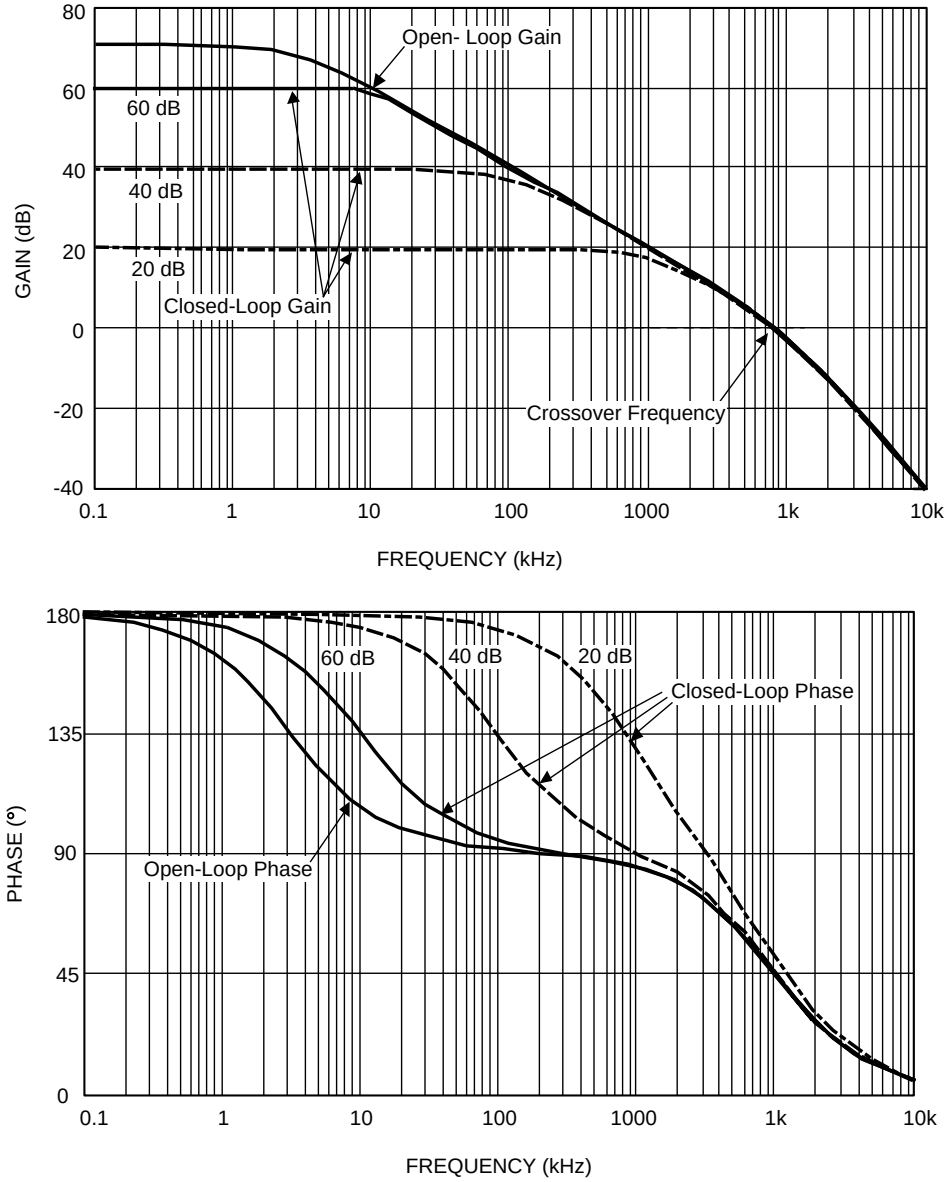


**Figure 3. (a) Gain and (b) Phase versus Frequency Curves of the Open-Loop and Closed-Loop EA**

In this instance, the closed-loop amplifier is resistively configured as an inverting gain stage with DC gain, $A_{VCL}$, set at 60dB (1000 V/V), 40dB (100 V/V) and 20dB (10 V/V) distinct levels. It is readily apparent that the closed-loop gain curves are contained in the envelope of the open-loop gain characteristic [1].

Assuming the GBW is a constant for a given amplifier with a -20dB/decade open-loop gain roll-off, the -3dB bandwidth for any closed-loop gain can be calculated from

$$BW_{closed\ loop} = \frac{GBW}{A_{VCL}} \quad (3)$$

## 4 Compensator Transfer Function

It can be shown that the $V_{out}$-to-COMP voltage compensator small-signal transfer function, including the effects of a non-ideal closed-loop EA, is given by

$$\frac{\hat{v}_{comp}}{\hat{v}_{out}}(s) = G'_c(s) = -\frac{Z_F}{Z_i}\frac{a_v(s)\frac{Z_i}{Z_i + Z_F}}{1 + a_v(s)\frac{Z_i}{Z_i + Z_F} + \frac{(Z_i \text{ II } Z_F)}{R_{FB2}}} \quad (4)$$

The effect of amplifier internal input and output impedances and input offset voltage are neglected. Also, the small-signal variation of $V_{REF}$ is zero. If the EA is ideal, then the compensator transfer function is specified as

$$\frac{\hat{v}_{comp}}{\hat{v}_{out}}(s) = G'_c(s) = -\frac{Z_F}{Z_i} \quad (5)$$

Usually, the last factor in the denominator of Equation 4 is insignificant and the expression can be simplified as

$$\frac{\hat{v}_{comp}}{\hat{v}_{out}}(s) = \frac{G_c(s)}{1 + \frac{1 - G_c(s)}{a_v(s)}} \quad (6)$$

Equation 6 can be partitioned based on the frequency in relation to the EA GBW to yield Equation 7.

$$\frac{\hat{v}_{comp}}{\hat{v}_{out}}(s) = \begin{cases} G_c(s) \text{ if } a_v(s) >> 1 \text{ and } f < \text{GBW} \\ \frac{G_c(s)}{1 - G_c(s)} \; a_v(s) << 1 \text{ and } f > \text{GBW} \end{cases} \quad (7)$$

## 5 Control Loop Requirements

The cumulative of the power stage $G_{dv}(s)$ and PWM modulator FM gains (sometimes referred to as COMP-to-output gain) is plotted in Figure 4 for a representative buck converter with the following parameters denoted using the customary nomenclature referenced in Figure 1:

- $V_{in}$ = 5 V; $V_{out}$ = 1.8 V; $I_{out}$ = 5A;
- $L_f$ = 1.0 µH, $C_f$ = 100 µF;
- $R_{DS(ON)}$ = 10 mΩ; $R_{DCR}$ = 10 mΩ; $R_{Cf\ ESR}$ = 3 mΩ;
- $f_s$ = 1 MHz; $v_{ramp}$ = 1 V pk-pk.

The overall loop gain crossover frequency is usually located between one tenth and one fifth of the switching frequency. Thus, it is not unreasonable given a switching frequency of 1 MHz to target a 200 kHz loop crossover frequency. The net gain of the power stage and modulator at 200 kHz is –29.5dB (designated $G_M$ in Figure 4). Plainly, then, a compensator gain of +29.5dB is required at 200 kHz to achieve a total loop gain of 0dB at crossover. Note that the overall loop gain is expressed as

$$T_v(s) = G_{dv}(s)\, Gc'(s)\, F_M \quad (8)$$

The compensation strategy employed with voltage mode controlled second order power stages traditionally involves use of two compensator zeros to counteract the LC filter double pole, one compensator pole located to nullify the output capacitor ESR zero and one compensator pole located at one half switching frequency to attenuate high frequency noise. The black trace in Figure 4 represents the gain necessarily generated by the compensator to achieve the required overall gain $T_v(s)$.

The compensator $G_c(s)$ bode plots for this illustrative example are shown in Figure 5. Using the aforementioned error amplifier with 10 MHz GBW and 70dB DC gain, the compensator characteristic derived via Equation 4 is superimposed. The frequency range is purposely wide to capture the low and high frequency regions where the non-ideal EA most affects the compensator characteristic. The open-loop EA gain is included for comparison.

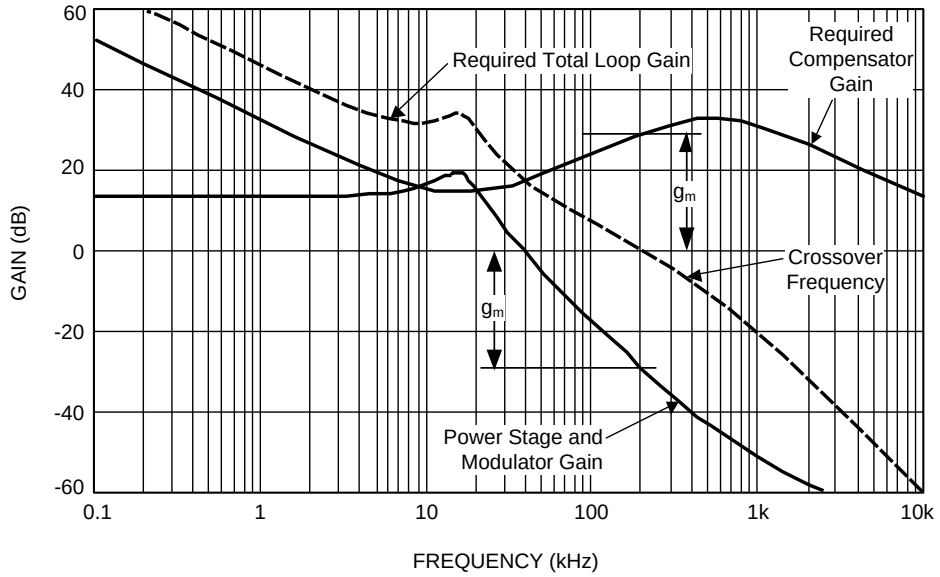


**Figure 4. Gain versus Frequency Curves of the Overall Loop Gain, Control-to-Output Gain, and Compensator Gain**

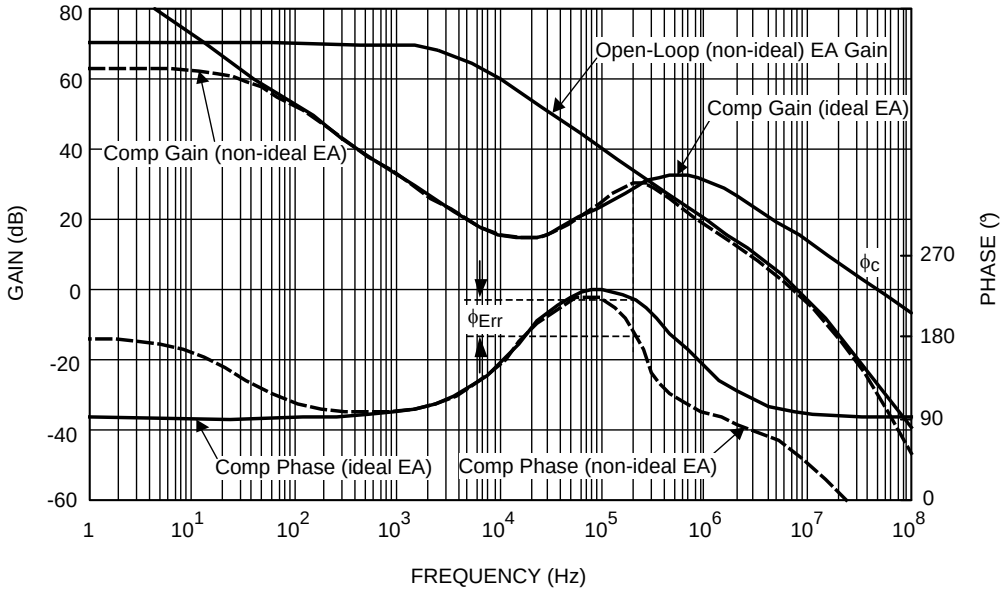


**Figure 5. Gain and Phase versus Frequency of Compensator With Ideal and Non-Ideal EA Characteristic**

There are four notables from this plot that merit further scrutiny:

- The primary concern is associated with the additional phase lag, denoted by $\Phi_{Err}$ in Figure 5, correlated to the non-ideal error amplifier that amounts to 38° at the preferred loop crossover frequency of 200 kHz.
- At low frequencies, the compensator gain with non-ideal EA is approximately 7dB below the open-loop EA DC gain level. A reduced low-frequency compensator gain can presage output voltage steady state error and impaired load regulation performance.
- The idealized compensator gain exceeds the open-loop (non-ideal) EA gain at frequencies above approximately 300 kHz whereas the actual compensator gain $G_c'$ (s) (with an embedded non-ideal EA) converges to the asymptote given by Equation 7, which is very close to the open-loop EA gain curve.

- Scarcely evident but unmistakable in Figure 5 is a relative gain bump in the compensator gain between 90 kHz and 240 kHz created by the non-ideal error amplifier. This is correlated to the Q factor inherent in the expression for $G_c'$ (s) given by Equation 4 and related to the effective resonant damping intrinsic when a +20dB/decade compensator gain component converges with the -20dB/decade characteristic of the open-loop EA gain.

## 6 Loop Characteristic Degradation

The overall loop $T_v$(s) gain and phase curves are revealed in Figure 6. The solid and dashed lines indicate the response with ideal and non-ideal EA characteristics, respectively. Clearly, the phase margin of the overall loop is acutely compromised by a relative phase lag $\Phi_{Err}$ (associated with the non-ideal EA) of 46°. The phase margin has a quantative reduction from 62° to 16° in absolute terms. Clearly, the EA has utterly inadequate performance for this challenging specification.

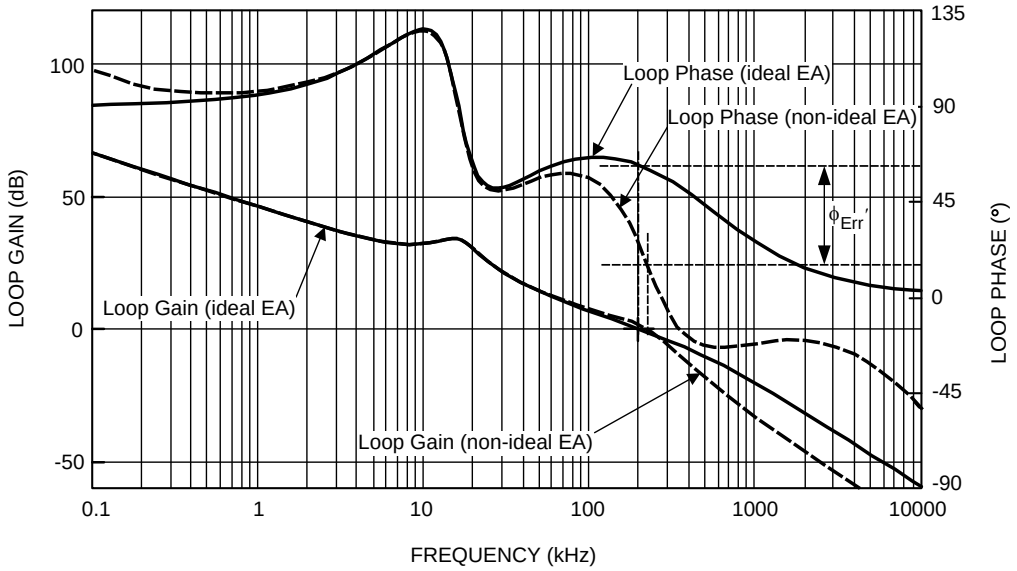


**Figure 6. Overall Loop $T_v$(s) Bode Plot With Ideal and Actual EA**

Interestingly, the non-ideal error amplifier creates a relative gain increase between 90 kHz and 240 kHz. The extra gain component, denoted by $G_{Err}$ in the bode plot of Figure 7 and magnified to emphasize additional detail around the crossover region, yields a larger loop crossover frequency of 220 kHz. On that basis alone, it is understood that the phase margin is compromised to an extent greater than the phase characteristic curve would independently imply.

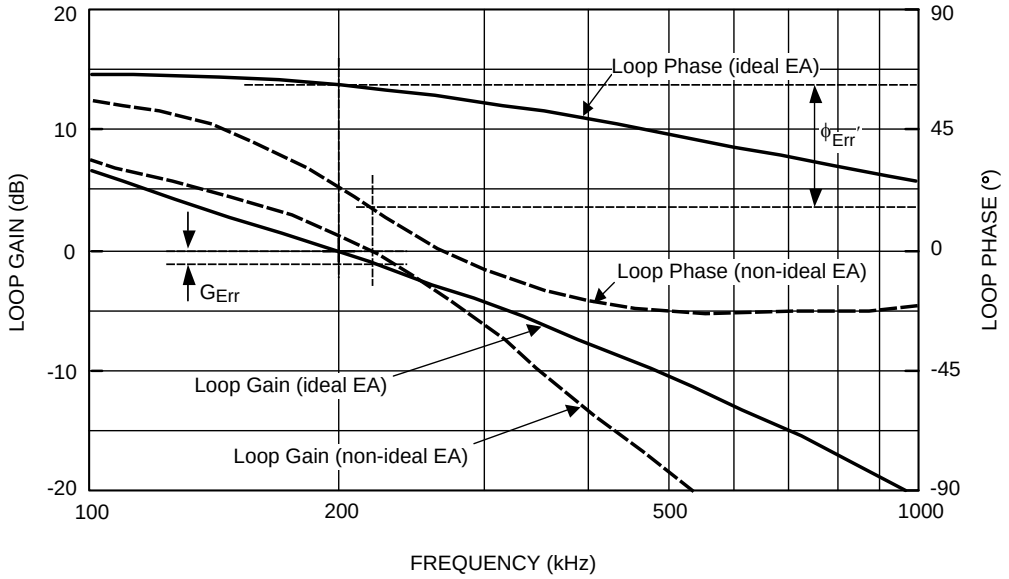


**Figure 7. $T_v(s)$ Bode Plots Scaled to Accentuate the Crossover Region**

## 7 Simulation Results

Following, and in accordance with, the working principle and circuit parameters described earlier, a circuit simulation using SIMetrix/SIMPLIS was performed with overall loop crossover frequency targeted at 200 kHz. Figure 8 illustrates the resultant overall loop bode plots with both idealized and realistic EA transfer functions embedded. The excellent correlation of the simulation results to that in Figure 6 authenticates the validity and accuracy of the small-signal analysis.

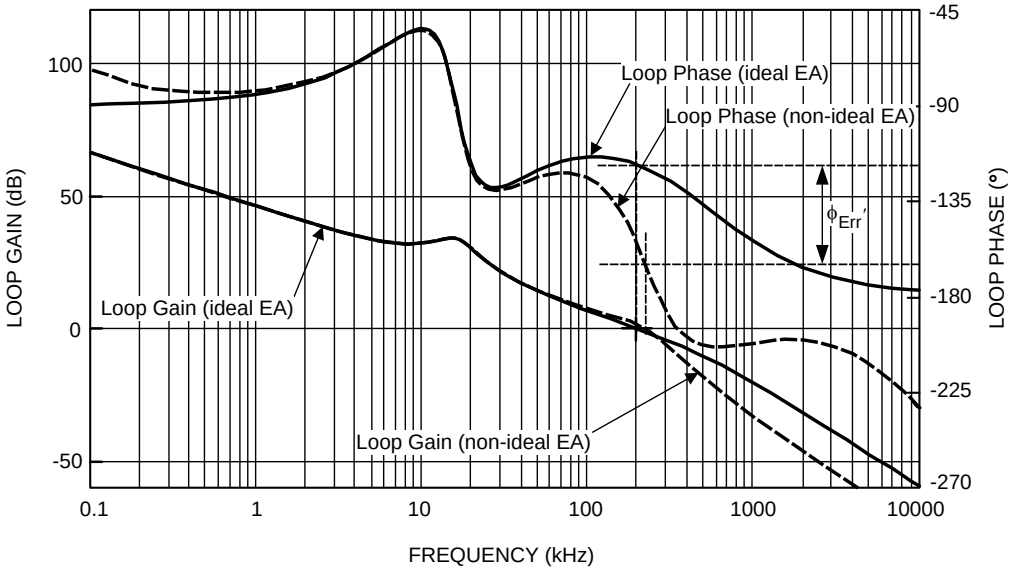


**Figure 8. Simulation Result of Overall Loop $T_v(s)$ Bode Plot With Ideal and Actual EA Models**

## 8 Error Amplifier Performance Requirements

The phase trajectories underscored by the analysis and simulation results presented in Figure 6 and Figure 8 give cause for circumspection, signifying severe phase margin degradation at best or a totally unstable system at worst. It seems mandatory to clarify the minimum error amplifier performance necessary to achieve the desired loop response and transient characteristics.

Empirically, it is accepted that a large EA DC gain is advantageous to diminish output voltage steady state error and an absolute level of 70dB is usually interpreted as a minimum design target.

To improve the phase margin to within 10° of that using an ideal EA, it is proposed that the EA GBW should at least equal the unity gain frequency, denoted as $f_c$ in Figure 5, of the necessary compensator characteristic $G_c(s)$. For example, the compensator required for a 200 kHz overall loop crossover has a unity gain frequency $f_c$ of 45 MHz in Figure 5. Employing an EA with a 45 MHz GBW and recalculating, the phase margin is restored from its original low level of 14° to a quite acceptable 52° (i.e. the EA induced phase margin erosion improves from 46° to 10°). Of course, operation with a somewhat lower EA GBW is feasible if the designer is aware that an initial phase margin specification greater than normal is a necessary starting point. The open-loop EA phase margin has little impact in this instance – altering the EA high frequency pole location does not appreciably change the overall loop response or phase margin since the EA high frequency pole is positioned well above the overall loop crossover frequency. An open loop EA phase margin of 45° to 80° is commonplace, although this parameter is often not explicitly specified in a controller or regulator IC data sheet. However, the amplifier large-signal slew-rate (SR) is usually provided and indicates the amplifier output drive current capability through a specified feedback capacitor to effect a large change in COMP voltage. For example, the Texas Instruments LM3743 PWM controller error amplifier provides a slew-rate of 0.5 V/µs with 2.2 nF capacitance. Its GBW and DC gain are 30 MHz and 90 dB, respectively.

## 9 References

1. ‘Analysis and Design of Analog Integrated Circuits’, P.R. Gray & R.G. Meyer, John Wiley & Sons, 1977

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