AN-1331 LM5033 Evaluation Board

1 Introduction

The LM5033EVAL evaluation board provides the design engineer with a fully functional intermediate bus converter (IBC) employing a half-bridge topology. Configured as an IBC, the circuit operates open loop, resulting in an output voltage which tracks the input voltage. Operating open loop results in very high efficiency (>95%), since the circuit operates at maximum duty cycle, making best use of the transformer with minimal deadtime.

IBCs are used to change a relatively high voltage (e.g., 48V) to a lower voltage (e.g., 9V) to power Point-of-Load (POL) regulators. Since many POLs are buck converters, which have higher efficiency when their input voltage is low, the combination of IBC+POLs provides higher overall system efficiency. Additionally, an IBC provides isolation which buck converters do not.

This board's specifications are:

- Input voltage: 40V to 60V, 48V nominal
- Output voltage: 7.5V to 11.3V, 9.0V nominal
- Output current: 0 to 20A
- Measured efficiency: 95.5% (40V<V_{IN}<60V, Io = 11A)
- Load regulation: ±4% (0-20A)
- Internal oscillator frequency: 315 kHz
- Current limit: ≅23A
- Shutdown input
- Synchronizing input
- Size: 2.3 x 1.45 x 0.43 in. (¼ brick footprint)

The printed circuit board consists of 4 layers of 2 oz copper on FR4 material, with a thickness of 0.050 in. It is designed for continuous operation at rated load with a minimum airflow of 200 LFPM.

2 Theory of Operation

Referring to Figure 8, the circuit is a half-bridge configuration with Q1 and Q2 as the high side and low side switches, respectively. The half supply point is at the junction of C1-C2 and C3-C4, with R1 and R2 ensuring equal voltage division from V_{IN}. The LM5033 controller alternately drives Q1 and Q2 via the LM5100 level shifting gate driver. The power transformer (T1) has a 5-turn primary, and two secondaries of 2 turns each with a common terminal. The secondary side uses synchronous rectifiers Q3 and Q4 to maintain high efficiency. The 4-turn auxiliary winding powers the V_{CC} line to reduce power dissipation within the LM5033.

Current sensing transformer T2 provides primary side current information to the LM5033 (pin 8) for over-current detection.

Comparators U2A, U2B, and U3A provide under-voltage (UVLO) and over-voltage (OVLO) sensing of V_{IN}. If V_{IN} is outside the range of 40-60V, the circuit shuts down.

This evaluation board can be synchronized to an external clock. A shutdown pin permits shutting down the output voltage by using an external switch to ground.

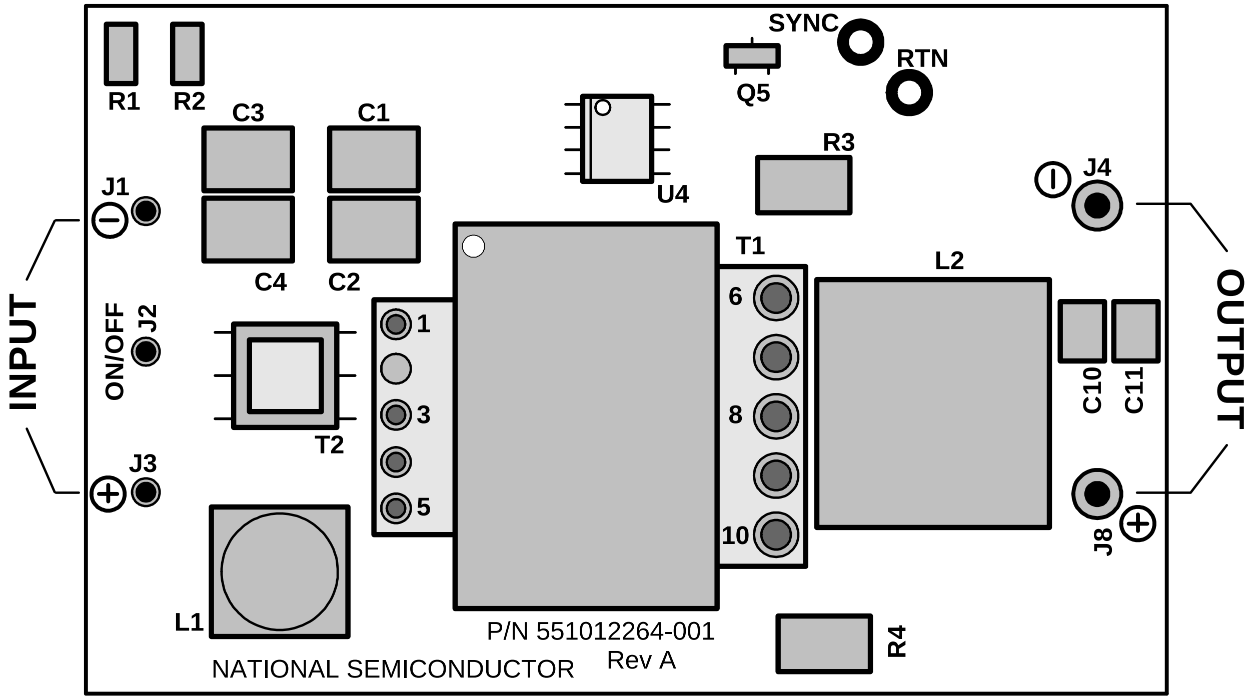


Figure 1. Evaluation Board - Top Side

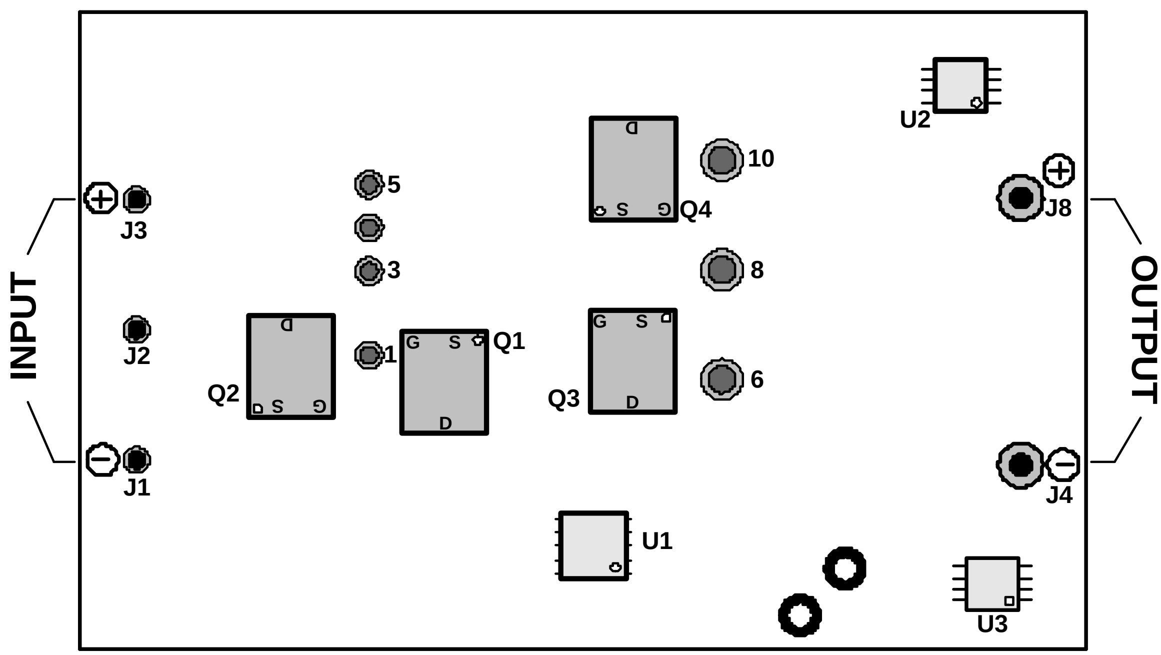


Figure 2. Evaluation Board - Bottom Side

3 Board Layout and Probing

The pictorial in Figure 1 and Figure 2 shows the placement of the significant components which may be probed in evaluating the circuit's operation. The following should be kept in mind when the board is powered:

1. The board has two circuit grounds - one associated with the input power, and one associated with the output power. The grounds are DC isolated.
2. The main current carrying components (L1, T1, T2, Q1, Q2, L2, Q3 and Q4) will be hot to the touch at maximum load current. USE CAUTION. When operating at load currents in excess of 5A the use of a fan to provide forced air flow IS NECESSARY.
3. Use care when probing the primary side at maximum input voltage. 60 volts is enough to produce shocks and sparks
4. At maximum load current (20A), the wire size and length used to connect the load becomes important. Ensure there is not a significant voltage drop in the wires. A minimum of 14 gauge wire is recommended.
5. The input wires will carry an average of 4A at maximum load current. Ensure these wires are adequately sized.

4 Board Connections/Start-Up

When operating at load currents in excess of 5A forced air flow across the board IS NECESSARY. The input connections are made to terminals J3 (+) and J1 (-). The source must be capable of supplying the input current shown in Figure 5. Upon turn-on the input current increases linearly, without overshoot, due to the LM5033's softstart function .

The load is connected to terminals J8 (+) and J4 (-). A minimum of 14 gauge wire should be used for the 20A load current.

Before start-up a voltmeter should be connected to the input terminals, and one to the output terminals. The input current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually until the under-voltage lockout threshold (UVLO, ≅37V) is reached, at which time the output becomes active. At this point the three meters should be checked immediately to ensure they indicate nominal values.

5 Performance

Once the circuit is powered up and operating normally, the output voltage follows the input voltage as shown in Figure 6. The load regulation is ≅ ±350 mV (±4%), due to an output impedance of ≅30 mΩ. The power conversion efficiency, which exceeds 95%, is shown in Figure 7.

6 Waveforms

Figure 4 shows some of the significant waveforms for various input/output combinations. REMEMBER there are two circuit grounds, and scope probe grounds must be connected appropriately. When viewing the signal at the CS pin the scope probe and its ground lead must be directly across C13.

7 Primary Side Operation

With V_{IN} within the normal operating range (40V to 60V) the LM5033 alternating outputs drive the LM5100 Gate Driver. The LM5100's LO output drives Q2's gate with a 0V to 10V signal, and the HO output drives Q1's gate with a voltage which switches between ground and 9V above V_{IN}. When Q1 is on current flows from L1 and out of C1/C2 through Q1, T1's primary, T2, and into C3/C4. When Q2 is on current flows out of C3/C4 through T2, T1's primary, and Q2 to ground. The LM5033's ensured deadtime ensures Q1 and Q2 are never on simultaneously.

8 Secondary Side Operation

When Q1 is on, T1's pin 6 is high relative to pins 8 and 10. Q3 is on since its gate is pulled up to between 6V and 9.5V (depending on V_{IN} and the load current) through Q6, causing pin 10 to be within 60 mV of ground. The load current flows from T1's pin 8 through L2, the load, and through Q3 to pin 10. Since pin 10 is effectively at ground Q4 is off, and no current flows out of T1's pin 6 (except for a small amount through Q6 and R18). During the next half cycle, when Q2 is on, T1's pin 10 is high relative to pins 8 and 6, Q4 provides the return path for the load current, and Q3 is off.

During the deadtime when both Q3 and Q4 are off, the load current's return path is through their body diodes. The gate voltage at Q3 and Q4 is limited by Q6 and Q7, respectively, to ≅1.5V below that at Z2's cathode.

9 UVLO/OVLO Operation

When V_{IN} exceeds 13V the LM5033 is fully biased, providing 9.6V at V_{CC} and 2.5V at the REF pin. V_{CC} powers comparators U2 and U3 which have open collector outputs. With V_{IN} below the UVLO threshold U2A and U3A outputs are low, grounding the Softstart pin and disabling the LM5033 outputs. When V_{IN} is increased past 37V both U2A and U3A outputs open, releasing the Softstart pin and allowing the voltage across C14 to ramp up. When the Softstart pin voltage exceeds 1.0V the LM5033 outputs become active. When V_{IN} is reduced below 33V U2A and U3A outputs switch low, disabling the LM5033 outputs.

When V_{IN} exceeds the over-voltage lockout threshold (OVLO) at 63V both U2B and U3A outputs switch low, grounding the Softstart pin and disabling the LM5033 outputs. As V_{IN} is reduced below 61.5V both U2B and U3A outputs open releasing the Softstart pin. When the Softstart pin voltage exceeds 1.0V the LM5033 outputs become active.

10 V_{CC}

While the LM5033 internally generates 9.6V at V_{CC}, the internal regulator is used only during start-up and when the LM5033 is shut down by the On/Off input or the UVLO/OVLO circuit. When the LM5033 outputs are enabled, the voltage from T1's auxiliary winding (Pins 1, 5) is regulated to 10.3V by Z1 and Q5. This voltage powers the V_{CC} requirements within the LM5033, the reference voltage at pin 2, the LM5100's V+ pin, and the two dual comparators (U2, U3). The LM5033's internal V_{CC} regulator is shut off, reducing its power dissipation.

11 Current Limit Operation

The current out of T2's secondary is 1% of the primary current. The voltage across R7 is therefore proportional to the load current reflected through T1, and is provided to the LM5033's CS pin via the R8/C13 filter. When the load current exceeds ≅23A the voltage at CS will exceed 0.5V causing the LM5033 to disable its outputs, and internally ground the Softstart pin. When the softstart capacitor is fully discharged and the voltage at CS has fallen below 0.5V the Softstart pin is internally released. The Softstart voltage initially rises slowly due to the parallel combination of C14 and C20 (U3B's output is low). After ≅10 ms, when the softstart voltage reaches 1.0V, the LM5033 outputs become active and C20 is effectively removed (U3B's open collector output opens). The Softstart voltage then rises rapidly, determined by C14. If the overload condition is still present the above sequence repeats when the current limit threshold is again reached. See Figure 3.

The addition of C20 and U3B lengthens the off-time between retries in a current limit situation, reducing the on-time/off-time ratio. The result is lower average input current and a lower temperature rise in the circuit components

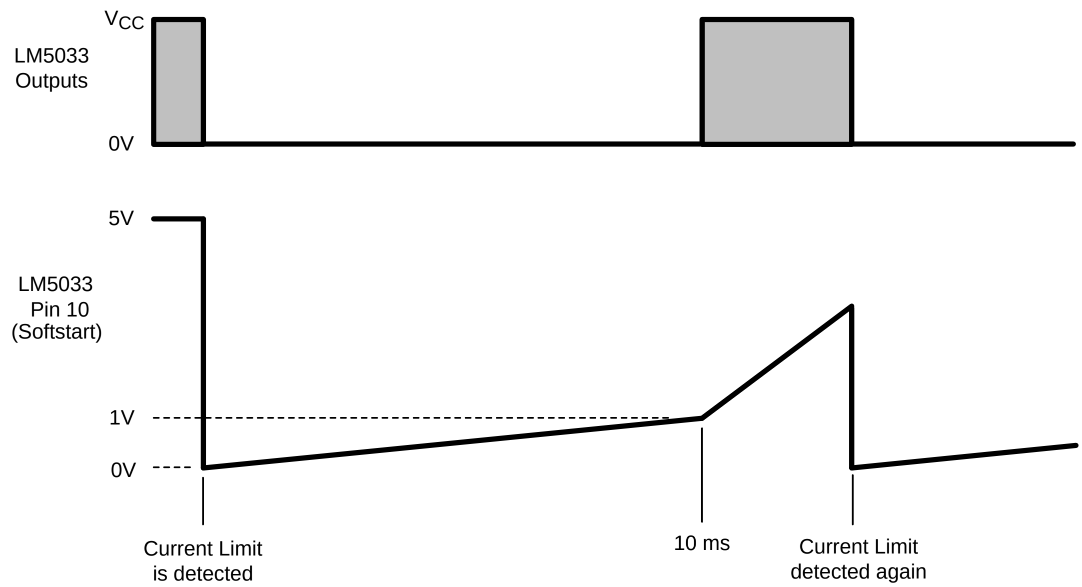


Figure 3. Current Limit Operation

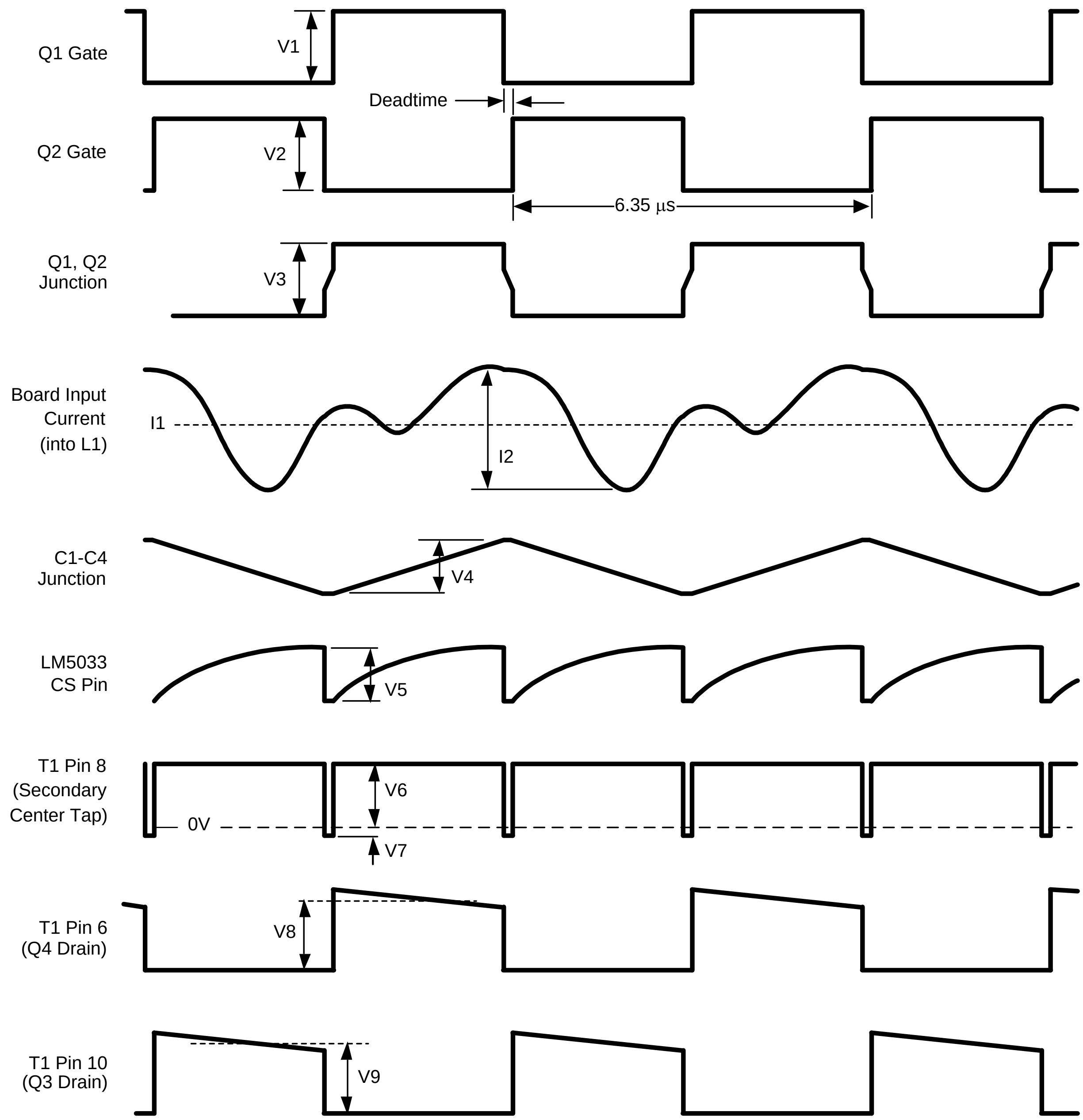
12 Shutdown

The On/Off pin (J2) permits shutting off the converter by an external switch. J2 must be taken below 0.8V with an open collector or open drain device to disable the LM5033 outputs. Releasing the pin allows the circuit to resume normal operation.

13 External Sync

The LM5033's internal oscillator can be synchronized to an external signal applied to the SYNC input pad. The external frequency must be higher than the free running frequency set with the R_T resistor (315 kHz with R_T = 16.5 kΩ). The sync input pulse width must be between 15 ns and 150 ns, with an amplitude of 1.8V - 3.0V at the SYNC pad. The pulses are coupled to the LM5033 through a 100 pF capacitor (C15).

The ground side of the external signal source must be connected to the RTN pad which is adjacent to the SYNC pad. Do not use the ground input pin (J1) for this signal's ground.



V_{IN}, I_O	V1	V2	V3	V4	V5	V6	V7	V8	V9	I1	I2
40V, 2A	49V	9.8V	40V	0.2V	60 mV	7.9V	-1.0V	16.1V	16.1V	0.42A	12 mA
40V, 20A	48V	9.8V	40V	1.7V	430 mV	7.6V	-1.4V	15.4V	15.4V	3.88A	35 mA
60V, 2A	69V	10V	60V	0.25V	60 mV	12.1V	-1.0V	23.7V	23.7V	0.43A	19 mA
60V, 20A	68V	10V	60V	2.1V	430 mV	11.7V	-1.4V	23.2V	23.2V	3.93A	50 mA

Figure 4. Representative Waveforms

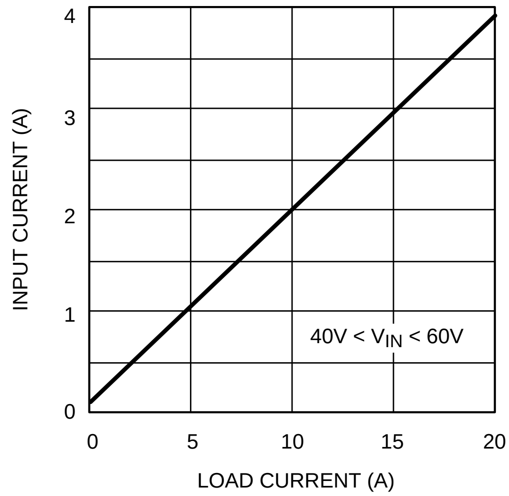


Figure 5. Input Current vs Load Current

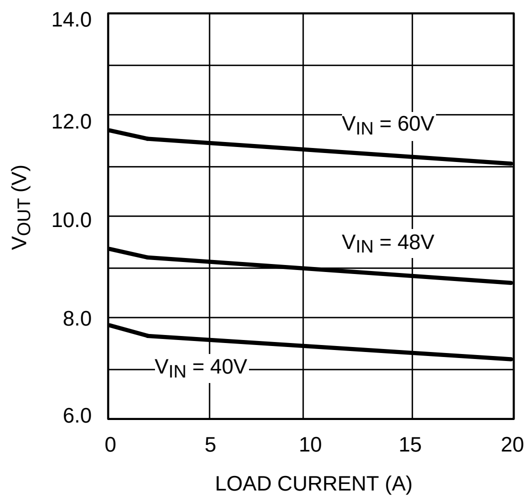


Figure 6. V_{OUT} vs Load Current and V_{IN}

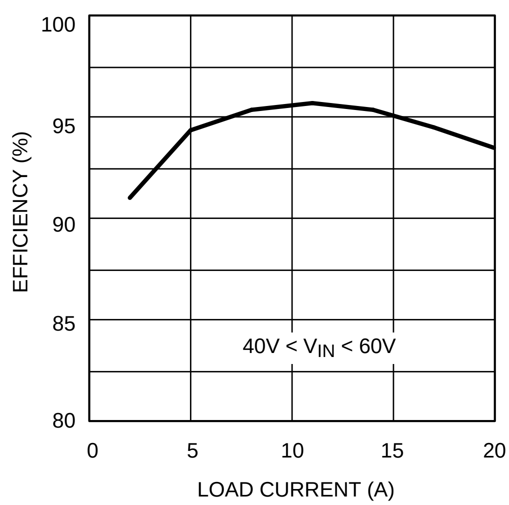


Figure 7. Efficiency vs Load Current

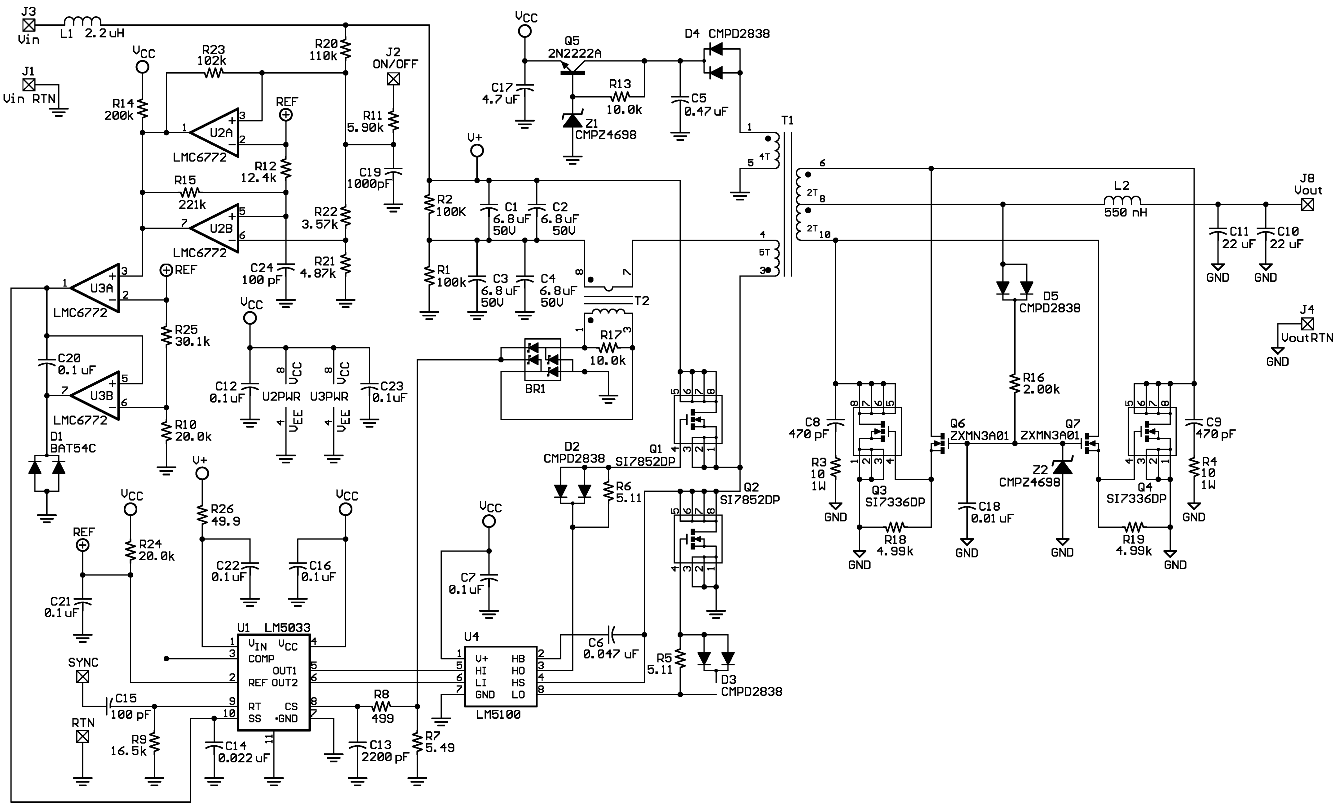


Figure 8. Eval Board Schematic

Table 1. Bill of Materials

Item	Item	Mfg., Part No.	Package	Value
BR1	Schottky diode bridge	Diodes, Inc. BAT54BRW	SOT-363	30V, 0.2A
C1-4	Capacitor	TDK, C4532X7R1H685M	1812	6.8 µF, 50V
C5	Capacitor	TDK, C2012X7R1E474M	0805	0.47 µF, 25V
C6	Capacitor	Kemet, C0805C473M3RAC	0805	0.047 µF, 25V
C7, 12, 16, 20-23	Capacitor	Kemet, C0805C104M4RAC	0805	0.1 µF, 16V
C8, 9	Capacitor	Kemet, C0805C471M5RAC	0805	470 pF, 50V
C10, 11	Capacitor	TDK, C3225X7R1C226M	1210	22 µF, 16V
C13	Capacitor	Kemet, C0805C222K4RAC	0805	2200 pF, 16V
C14	Capacitor	Kemet, C0805C223K4RAC	0805	0.022 µF. 16V
C15, 24	Capacitor	Kemet, C0805C101K4GAC	0805	100 pF, 16V
C17	Capacitor	TDK, C3216X7R1C475M	1206	4.7 µF, 16V
C18	Capacitor	Kemet, C0805C103M4RAC	0805	0.01 µF, 16V
C19	Capacitor	Kemet, C0805C102M4RAC	0805	1000 pF, 16V
D1	Dual Schottky diode	Vishay BAT54C	SOT-23	30V, 0.2A
D2-5	Dual diode	Central Semi CMPD2838	SOT-23	75V, 0.2A
L1	Inductor	TDK RLF7030T-2R2M5R4	SMD	2.2 µH, 5.5A
L2	Inductor	TDK SPM12535T-R60M220	SMD	550 nH, 22A
Q1, 2	N Channel MOSFET	Vishay Si7852DP	PowerPAK SO-8	80V, 12.5A
Q3, 4	N Channel MOSFET	Vishay Si7336DP	PowerPAK SO-8	30V, 30A
Q5	NPN Transistor	Central Semi., CMPT2222A	SOT-23	75V, 0.6A

Table 1. Bill of Materials (continued)

Item	Item	Mfg., Part No.	Package	Value
Q6, 7	N Channel MOSFET	Zetex, ZXMN3A01F	SOT-23	30V, 2 A
R1, 2	Resistor	Vishay, CRCW12061003F	1206	100 kΩ, ¼ W
R3, 4	Resistor	Vishay, CRCW251210R0F	2512	10Ω, 1W
R5, 6	Resistor	Vishay, CRCW08055R11F	0805	5.11Ω
R7	Resistor	Vishay, CRCW08055R49F	0805	5.49Ω
R8	Resistor	Vishay, CRCW08054990F	0805	499Ω
R9	Resistor	Vishay, CRCW08051652F	0805	16.5 kΩ
R10, 24	Resistor	Vishay, CRCW08052002F	0805	20 kΩ
R11	Resistor	Vishay, CRCW08055901F	0805	5.9 kΩ
R12	Resistor	Vishay, CRCW08051242F	0805	12.4 kΩ
R13, 17	Resistor	Vishay, CRCW08051002F	0805	10 kΩ
R14	Resistor	Vishay, CRCW08052003F	0805	200 kΩ
R15	Resistor	Vishay, CRCW08052213F	0805	221 kΩ
R16	Resistor	Vishay, CRCW08052001F	0805	2.0 kΩ
R18, 19	Resistor	Vishay, CRCW08054991F	0805	4.99 kΩ
R20	Resistor	Vishay, CRCW12061103F	1206	110 kΩ, ¼ W
R21	Resistor	Vishay, CRCW08054871F	0805	4.87 kΩ
R22	Resistor	Vishay, CRCW08053571F	0805	3.57 kΩ
R23	Resistor	Vishay, CRCW08051023F	0805	102 kΩ
R25	Resistor	Vishay, CRCW08053012F	0805	30.1 kΩ
R26	Resistor	Vishay, CRCW080549R9F	0805	49.9Ω
T1	Power Transformer	Coilcraft B0853-A	Planar	
T2	Current Sense Transformer	Pulse Eng. P8208	SMD	100:1, 10A
U1	PWM Controller	Texas Instruments LM5033	WSON-10	
U2, 3	Dual Micropower Comparator	TI LMC6772	VSSOP-8	
U4	Gate Driver	Texas Instruments LM5100	SOIC-8	
Z1, 2	Zener diode	Central Semi CMPZ4698	SOT-23	11V, 350 mW

14 PCB Layouts

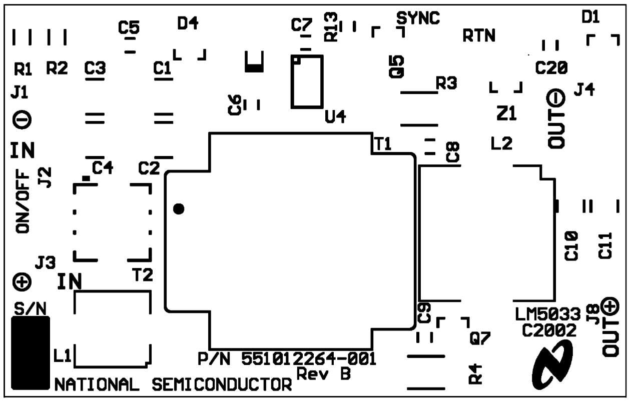


Figure 9. Top Silk Screen

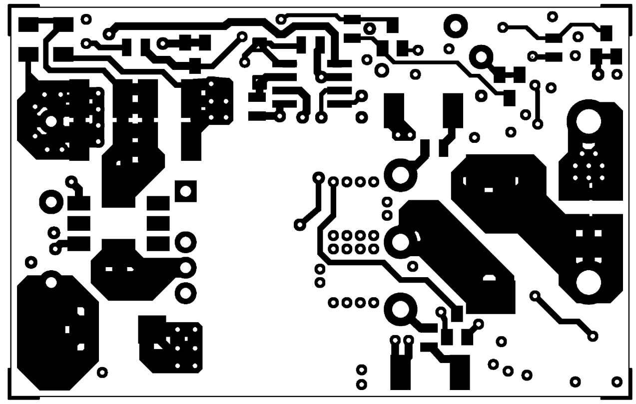


Figure 10. Top Layer

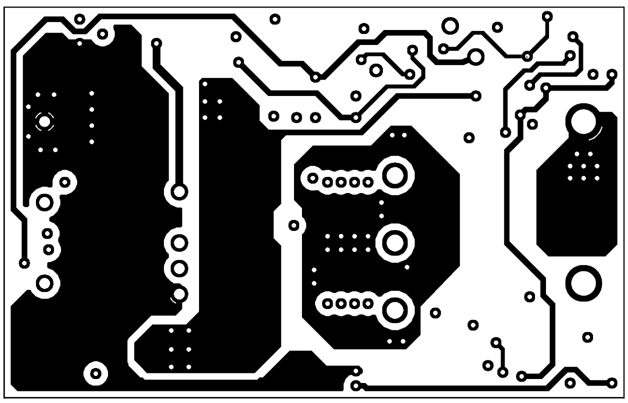


Figure 11. Layer 2

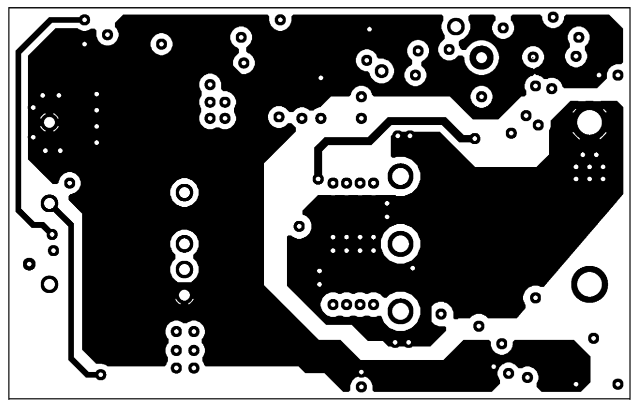


Figure 12. Layer 3

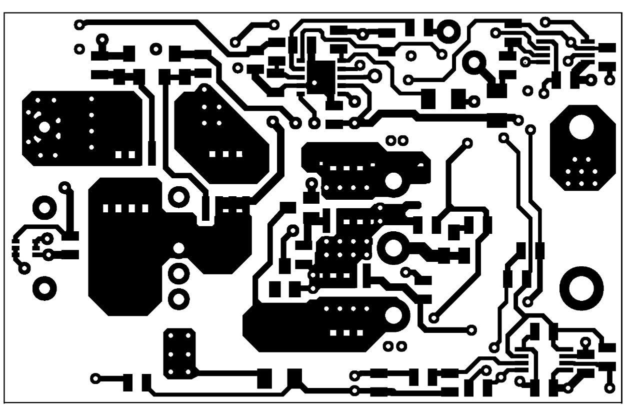


Figure 13. Bottom Layer, as viewed from the Top

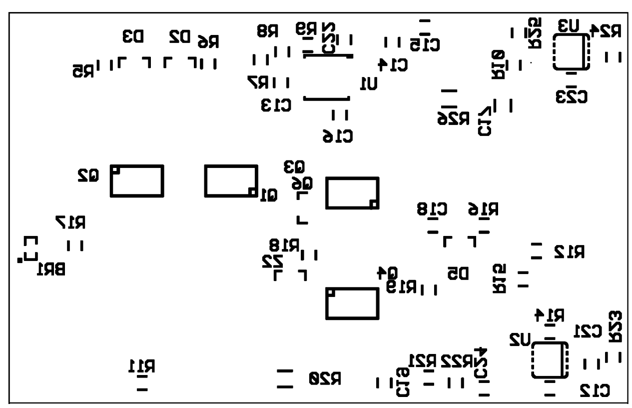


Figure 14. Bottom Silk Screen, as viewed from the Top

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