LMK00804BEVM User’s Guide

User's Guide

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LMK00804BEVM User's Guide

1 Introduction

The LMK00804B is a low skew, high performance clock fanout buffer, which distributes up to four LVCMOS/LVTTL outputs (3.3 V, 2.5 V, 1.8 V, or 1.5 V levels). The clocks are derived from one of two selectable inputs, which can accept differential or single-ended input signals.

This evaluation module (EVM) is designed to demonstrate the functionality and electrical performance of the LMK00804B device. For optimum performance, the board is equipped with 50-ohm SMA connectors and 50-ohm controlled impedance traces.

Table 1. Device and Package Configurations

DESIGNATOR	IC	PACKAGE
U1	LMK00804B	PW-16 (TSSOP 16 pin)

2 Features

- Easy to use evaluation board to fan-out up to four LVCMOS clocks with low phase noise/jitter
- Accepts differential or single-ended/LVCMOS input clock
- Device control pins configurable through jumpers
- Board power at 3.3-V for VDD and VDDO (single supply) or 2.5-/1.8-/1.5-V for VDDO (dual supply)

3 Setup

This section describes the jumpers and connectors on the EVM as well and how to properly connect, set up and use the LMK00804BEVM.

3.1 Input/ Output Connector Description

Connectors:

- **LVCMOS_CLK** SMA connector is used to interface an external single-ended clock input (50Ω source impedance) to the LVCMOS_CLK input of the device.
- **CLK and nCLK** SMA connectors are used to interface an external AC-coupled clock input to the second of the two differential input pairs (CLK1, nCLK1) of the device.
- **Q0 and Q3** SMA connectors are used to distribute two of the four LVCMOS clock outputs. The other two clock outputs are not connected to the traces, so their SMA connectors are not populated by default.

Power Supply Test Points:

- **Vdd** test point is used to connect 3.3-V power to the VDD supply of the board/device.
- **Vddo** test point is used to connect 3.3-/2.5-/1.8-/1.5-V power to the VDDO supply of the board/device.
- **GND** test point is used to connect the power supply ground to GND of the board/device.

Jumpers:

- **CLK_SEL** selects between one of the two selectable inputs.
  - 0 (position 1-2) = Select LVCMOS_CLK input
  - 1 (position 2-3) = Select CLK/nCLK input

- **CLK_EN** selects between U1 clock enabled or disabled modes.
  - 0 (position 1-2) = Clock Disabled (output drivers still enabled)
  - 1 (position 2-3) = Clock Enabled (normal operation)
- **OUT_EN** selects between U1 output enable or disable modes.
  - 0 (position 1-2) = Outputs Disabled (Hi-Z)
  - 1 (position 2-3) = Outputs Enabled

3.2 Equipment

With this EVM, one could distribute any one of two clocks to up to 4 LVCMOS outputs. Therefore, a minimum of one clock source is needed and appropriate test equipment to observe or measure the outputs.

3.3 Operation

Power with Single Supply (Vdd = Vddo = 3.3 V):

Before applying any clock inputs, short Vddo_SEL jumper pins 1-2 to set Vdd=Vddo and supply the board with 3.3V and ground at Vdd and GND test points. Make sure the total supply current (Idd+Iddo) being drawn is less than 26 mA without any output loading.

Alternative Power with Separate Core and Output Supplies (Vdd = 3.3 V, Vddo = 3.3-/2.5-/1.8-/1.5-V):

Before applying any clock inputs, short Vddo_SEL jumper pins 2-3 to allow Vdd & Vddo to be powered separately and supply the board with Vdd=3.3V, Vddo=3.3-/2.5-/1.8-/1.5-V, and GND. Make sure the Idd current is less than 21 mA and Iddo current is less than 5 mA without any output loading.

Inputs:

Figure 1 shows the LMK00804B input structure and default on-board input termination. The internal 51kΩ pull-up and pull-down resistors on CLK/nCLK work with the external 50Ω termination resistors, which causes the device inputs to be biased to about 1.1V. Therefore, AC-coupled clock sources from 0.15Vpp-1.3Vpp (50Ω terminated) can be tied to CLK/nCLK clock inputs directly. The input SMAs expect a 100Ω differential clock source. Note that with the default input configuration, the differential input has only very small offset voltage (~3.2mV) so that when the selected clock inputs are left open/floating, the outputs could have the tendency to chatter.

With DC-coupled clock sources, use a “DC-block” at the input SMAs to ensure DUT input voltage range compliance. Alternatively, adjust the clock source DC bias (if available) to make sure the LMK00804B input voltage range is not violated.

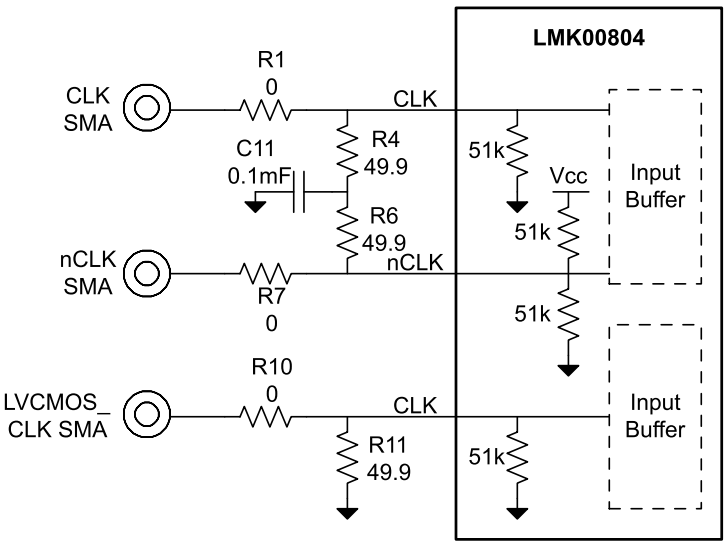


Figure 1. On-board Input Termination with Internal Pull-up/Pull-down Resistors

The clock inputs can accommodate a differential input or single-ended input signal with the proper external input termination using the various component options on the board. Refer to the datasheet for input interface application circuits.

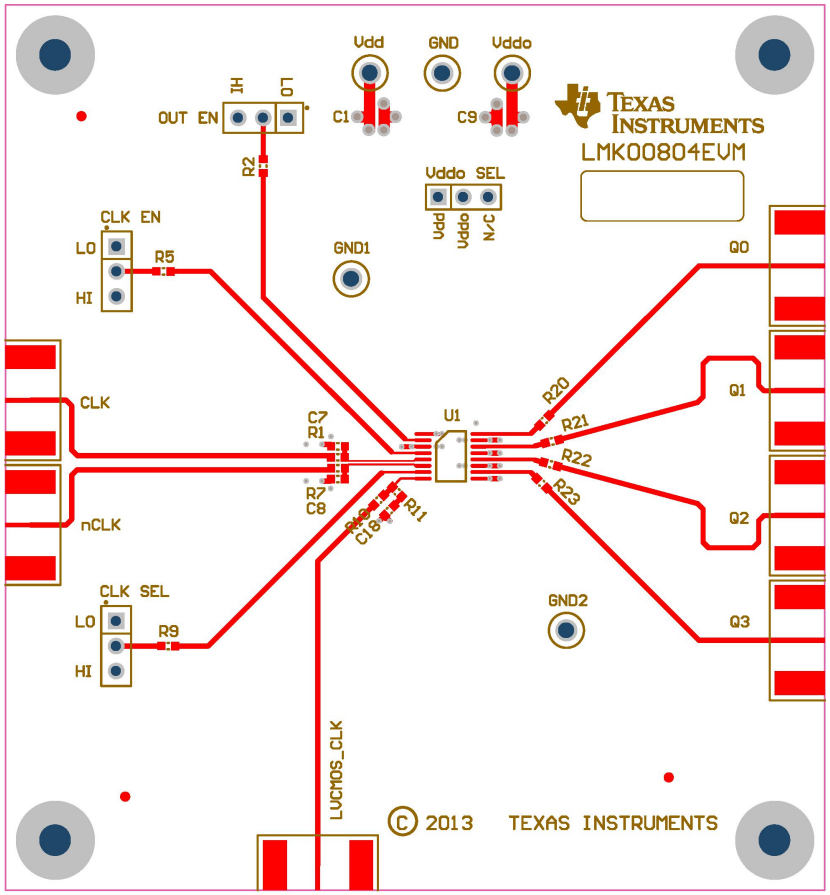
To achieve the best possible additive jitter and noise floor performance, it is recommended to drive the CLK/nCLK pair using an input signal with fast slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate can degrade the additive jitter and noise floor performance. For this reason, a differential input signal (e.g. LVPECL), is recommended because it typically provides higher slew rate and common-mode noise rejection compared to a single-ended input (e.g. LVCMOS/LVTTL or sine-wave).

The LVCMOS_CLK input is terminated on-board with 50 Ω to ground (R11), and can accommodate a single-ended input source expecting a 50 Ω load. When connecting a source-terminated LVCMOS input that expects a high-impedance input, remove R11 to disconnect the 50 Ω termination.

Outputs:

All four LVCMOS outputs (Rout = 7 Ω typ) are configured with 43Ω series resistors for source termination (Ro + Rs = 50 Ω) and routed via 50 Ω traces. By default, two of the four output traces are configured with SMA connectors, which can be connected through a 50Ω coax cable to a high-impedance load/receiver, such as a 1-MΩ scope input. When driving a high-impedance load, the output voltage swing measured at the load should be nearly rail-to-rail (GND to Vddo) over the specified operating frequency. When driving a 50-ohm load, the output voltage swing will be attenuated by about 50% (GND to Vddo/2) due to the divider formed source and load resistors.

4 PCB Layout



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LAYER NAME = Top Overlay			
PLOT NAME = Top Layer	GENERATED : 8/29/2013 12:57:54 PM		TEXAS INSTRUMENTS

Figure 2. Top Layer

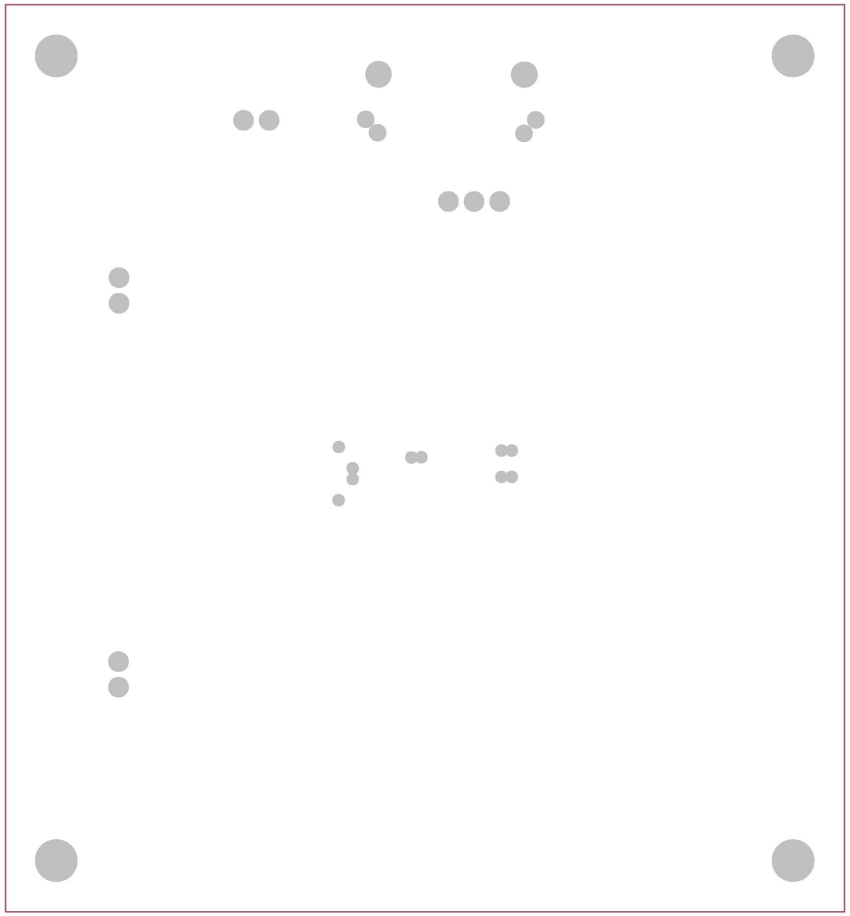

Figure 3. Inner Layer 2 (Ground Plane, Inverted)

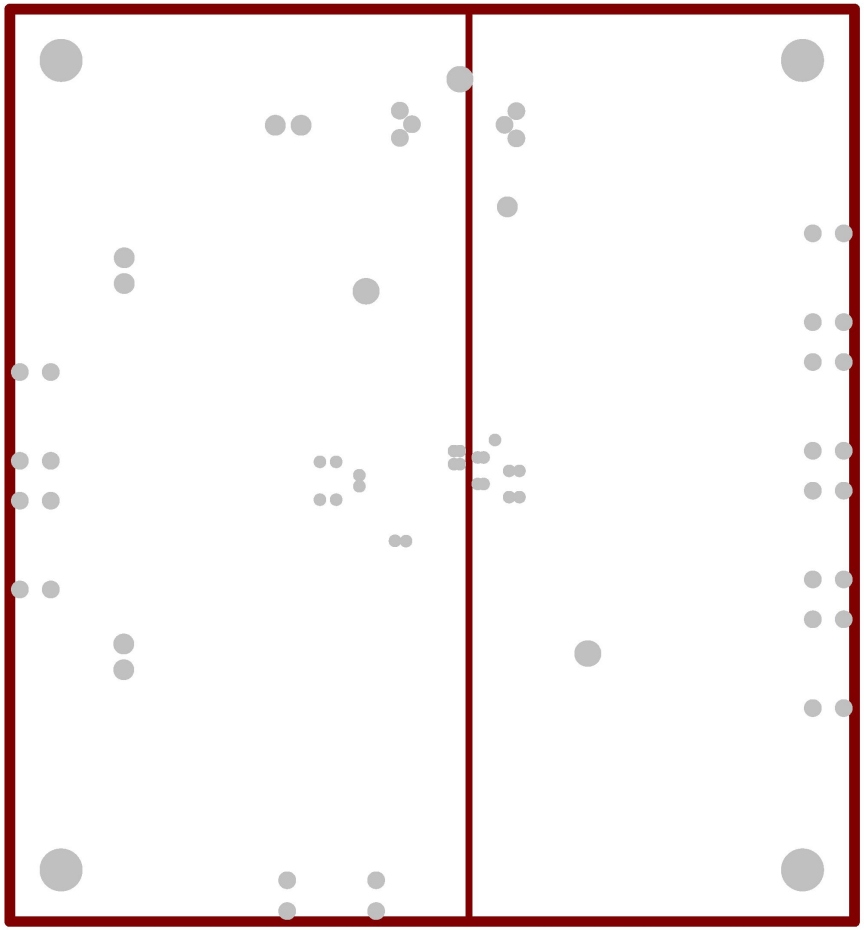

Figure 4. Inner Layer 3 (Vdd (Left) and Vddo (Right) Power Planes, Inverted)

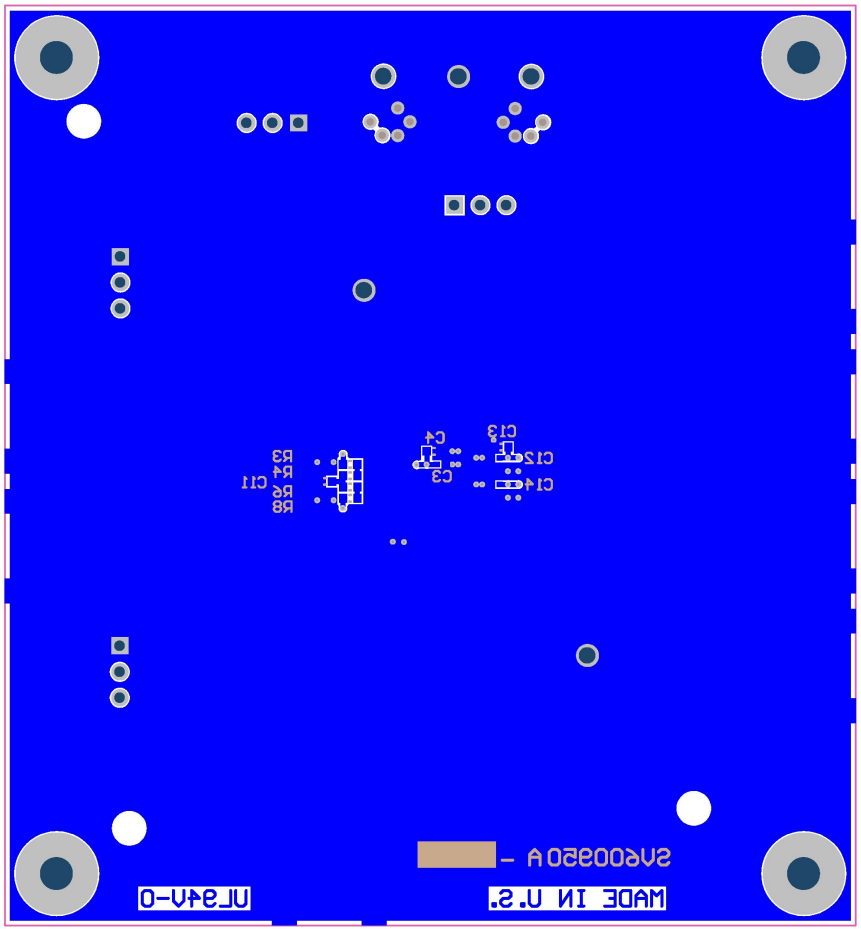

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Figure 5. Bottom Layer

5 Schematic

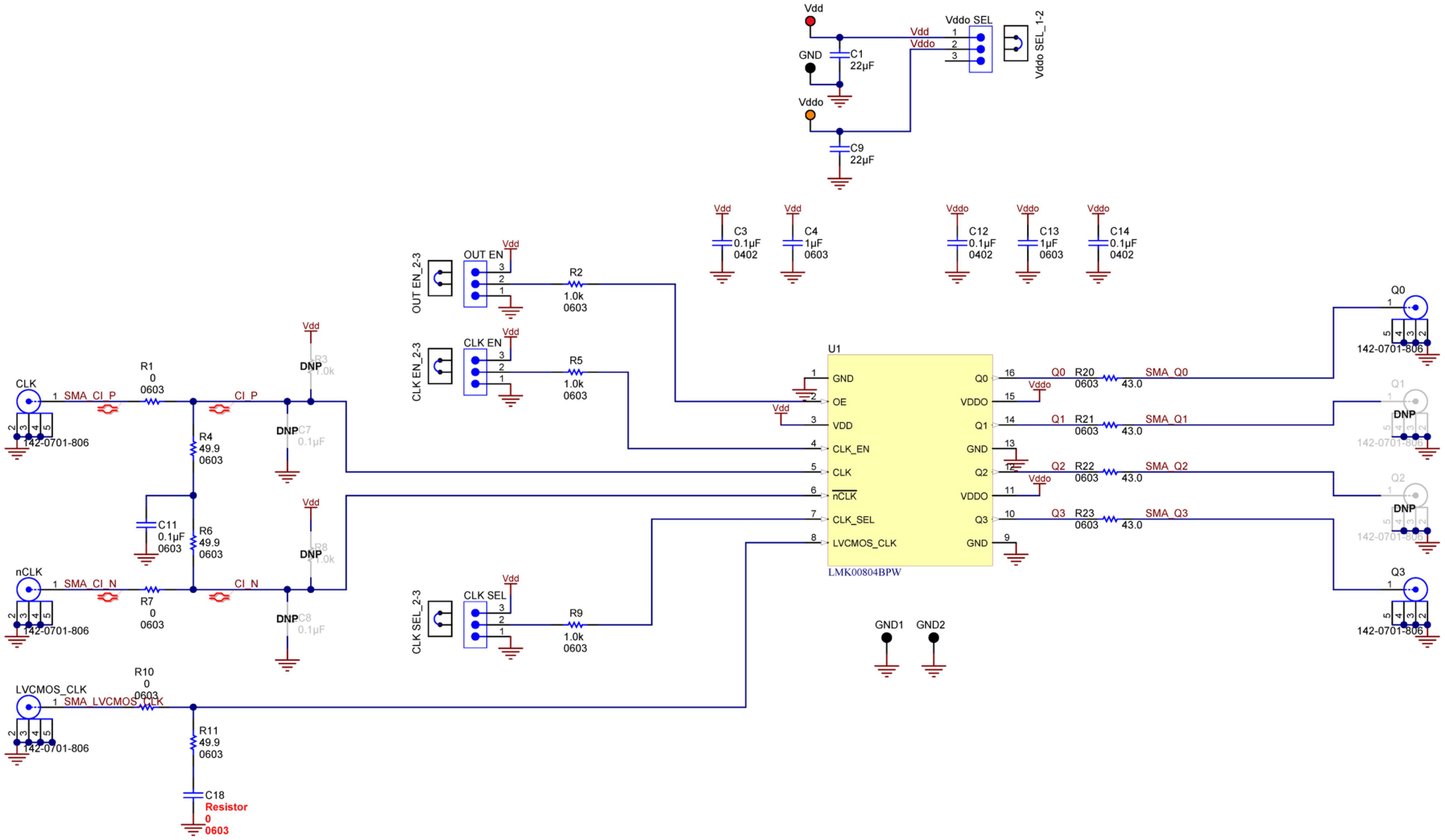

Figure 6. LMK00804BEVM Schematic

6 Bill of Materials

Table 2. LMK00804BEVM Bill of Materials

Designator	Qty	Value	Description	Pkg Ref	Part Number	Manufacturer
!PCB	1		Printed Circuit Board		SV600950	Any
C1, C9	2	22uF	CAP, CERM, 22uF, 16V, +/-10%, X5R, 0805	0805	C2012X5R1C226K125AC	TDK
C3, C12, C14	3	0.1uF	CAP, CERM, 0.1uF, 10V, +/-10%, X5R, 0402	0402	C1005X5R1A104K	TDK
C4, C13	2	1uF	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	0603	C1608X5R1A105K	TDK
C11	1	0.1uF	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	0603	0603YC104JAT2A	AVX
C18, R1, R7, R10	4	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
CLKEN, CLKSEL, OUTEN, VddoSEL	4	1x3	Header, TH, 100mil, 1x3, Gold plated, 230 mil above insulator	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
CLK, LVCMOS_CLK, nCLK, Q0, Q3	5	50 Ohm	Connector, SMT, End launch SMA 50 ohm	SMA	142-0701-806	Emerson Network Power
CLKEN_2-3, CLKSEL_2-3, OUTEN_2-3, VddoSEL_1-2	4	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
GND, GND1, GND2	3	Black	Test Point, Compact, Black, TH	Black Compact Testpoint	5006	Keystone
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NYPMS4400025PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650"H x 0.200"W	THT-14-423-10	Brady
R2, R5, R9	3	1.0k	RES, 1.0k ohm, 5%, 0.1W, 0603	0603	CRCW06031K00JNEA	Vishy-Dale
R4, R6, R11	3	49.9	RES, 49.9 ohm, 1%, 0.1W, 0603	0603	CRCW060349R9FKEA	Vishy-Dale
R20, R21, R22, R23	4	43.0	RES, 43.0 ohm, 1%, 0.1W, 0603	0603	RC0603FR-0743RL	Yageo America
U1	1		Low Skew, 1-to-4, Differential/LVCMOS-to-LVCMOS/LVTTL Fanout Buffer, PW0016A	PW0016A	LMK00804BPW	Texas Instruments
Vdd	1	Red	Test Point, TH, Compact, Red	Keystone5005	5005	Keystone
Vddo	1	Orange	Test Point, TH, Compact, Orange	Keystone5008	5008	Keystone
C7, C8	0	0.1uF	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	0603	0603YC104JAT2A	AVX
Q1, Q2	0	50 Ohm	Connector, SMT, End launch SMA 50 ohm	SMA	142-0701-806	Emerson Network Power
R3, R8	0	1.0k	RES, 1.0k ohm, 5%, 0.1W, 0603	0603	CRCW06031K00JNEA	Vishy-Dale

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

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This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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