Application Brief

Space-Grade, 100-krad, 100-V, High-Side Current Sensing Circuit

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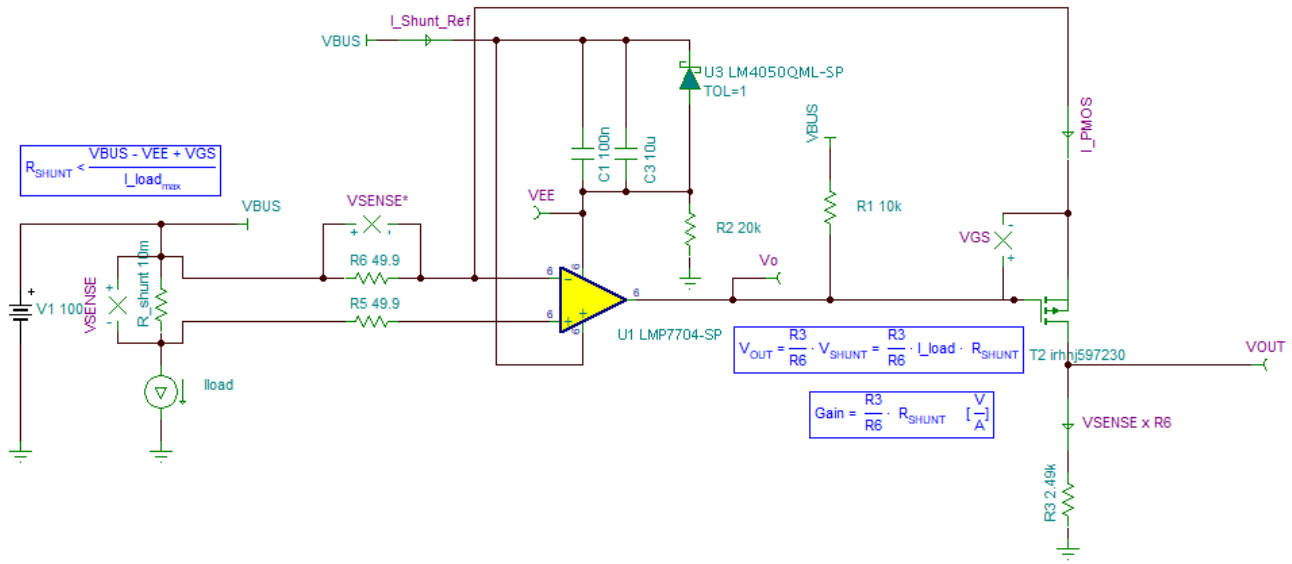
Design Goals

Parameter	Value
Common-Mode Voltage (VCM)	100 V
Load Current (I_{load} or I_{shunt})	1 A to 10A
Output Voltage (V_{out})	0.5 V to 5 V
Output Voltage Error	< 0.7%
Power Consumption	< 700 mW
Total Ionizing Dose (TID)	100-krad (Si)
Single Event Latch-up (SEL) Immunity	85 MeV·cm^2/mg

Design Description

To measure the current in power system health monitoring systems, a shunt resistor is placed either at the high side or the low side of the load. However, placing it at the low side could disturb the load ground. Measuring current at the high side is more preferable in most applications. The following figure shows a high-side current sensing circuit with power supply equal to 100 V and load current varying from 1 A to 10 A. The output of this circuit ranges from 0.5 V to 5 V.

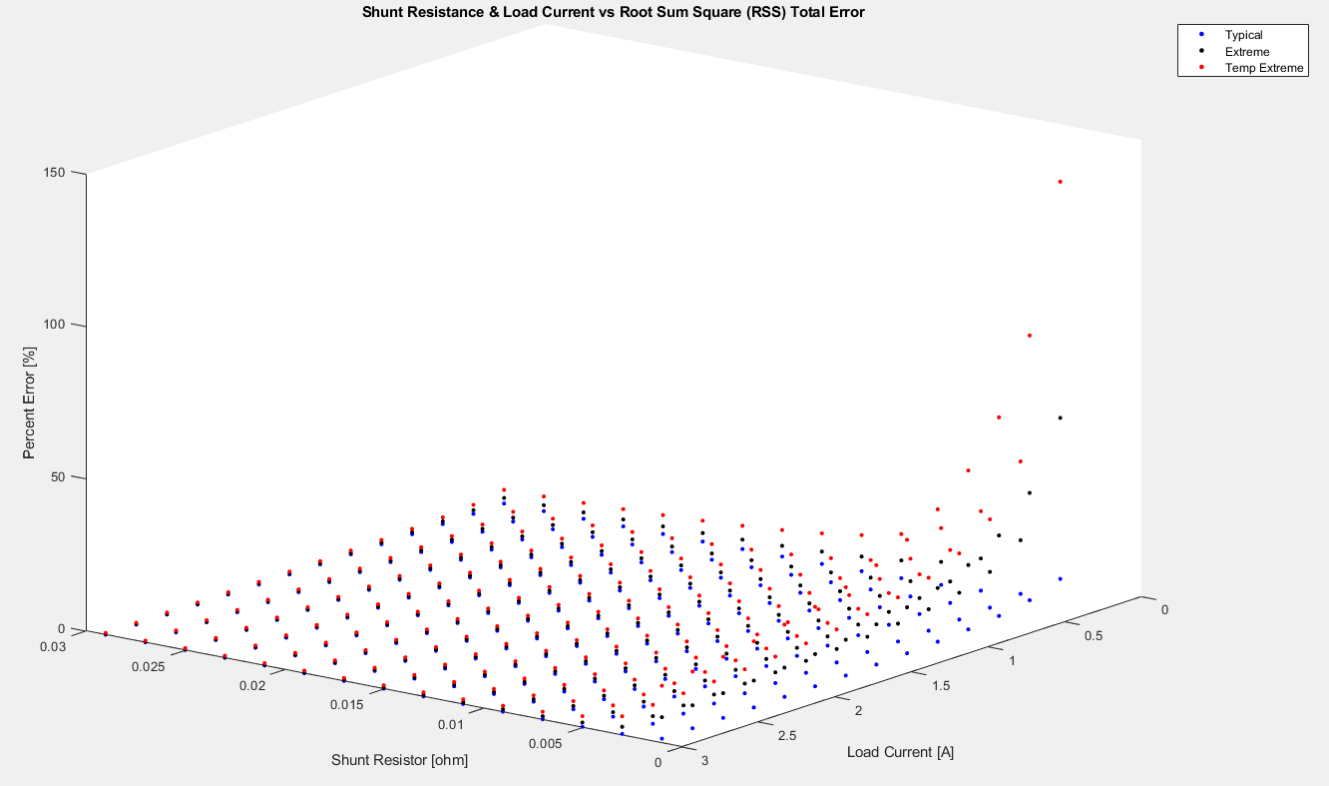


Design Notes

- The Vos of the op amp dominates the error when the load current is low. The tolerance of the shunt resistor dominates the error when the load current is high.
- Increasing R3, R5, and R6 values decreases PMOS power consumption but decreases output (V_{OUT}) range.
- R2 dominates the power consumption in the system

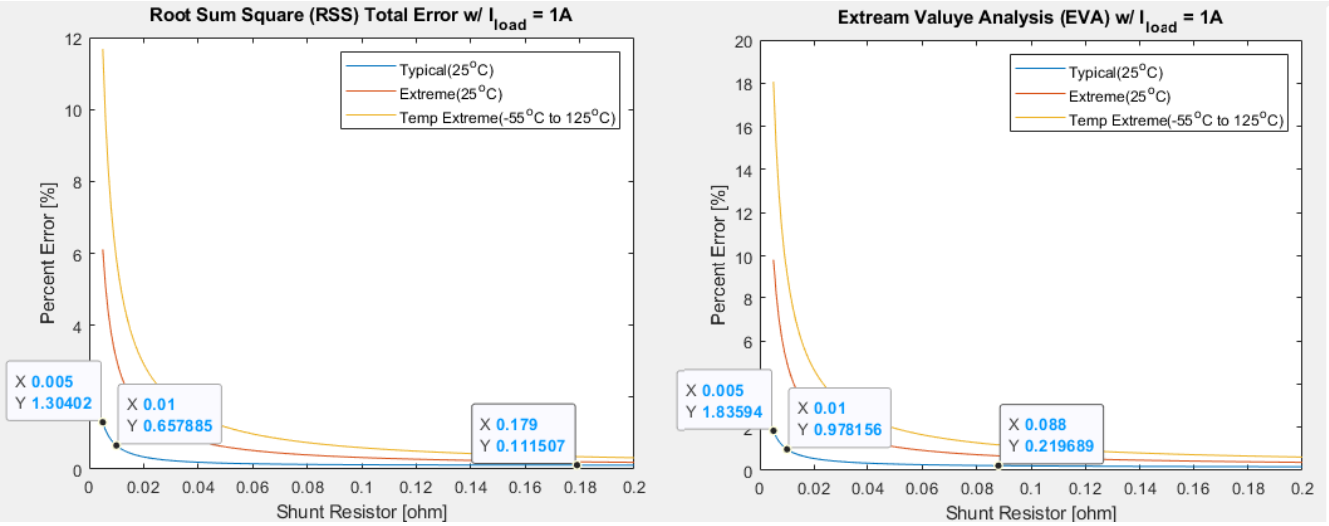
Design Steps

- **Circuit Specification**
  - Load power supply (V_{bus}): 100 V
  - Load current (IS1): 1 A to 10 A
  - Output voltage (V_{out}): 0.5 V to 5 V
- **Op Amp Selection**
  - The Op-amp common mode voltage (Vcm) needs to be equal to or greater than the bus voltage (V_{bus})
  - To minimize DC error, an op amp with small offset voltage, offset drift, bias current, and larger CMRR and PSRR are preferred
  - Since both input voltages of the op amp are close to V_{bus}, the maximum common-mode voltage range (CMVR) of the op amp must be equal to or greater than the positive power supply V_+ of the op amp
  - The LMP7704-SP is selected in this application. This device supports rail to rail input. It has a typical offset voltage of 60 µV, offset drift of 1 µV/°C, bias current of 1 pA, and CMRR of 130 dB. It also has rail-to-rail input and output.
- **Shunt Resistor Selection**
  - Consideration:
    1. Increasing the shunt resistor value could reduce error but increase power consumption and reduce load supply voltage
    2. To select a shunt resistor value, the CSM3637 series shunt resistor (data sheet is referenced in the *Design References* section) is selected to run a simulation in MATLAB®. The tolerance and temperature coefficient of this series of shunt resistors could be down to 0.1% and 10 ppm/°C. *Error Calculation* shows all equations used for calculating the output error in MATLAB.



As shown in the previous image, the shunt resistor (R_{shunt}) and load current (I_{load}) are used as the inputs for calculating the output percent error. The result shows that the output percent error increases as I_load decreases or R_shunt decreases. Hence, the load current is set to its minimum value (1 A) when picking the R_shunt value to satisfy the minimum requirement in the specification.

In the following curve, to obtain a root sum square (RSS) error less than 0.7%, a 10-mΩ shunt resistor is selected. Even though increasing R_shunt could further increase accuracy, it also increases power dissipation. The part number of the 10-mΩ CSM series shunt resistor selected is Y14870R00100B9W. The resistor has a power rating up to 3 W. With a derating factor of 0.6 (based on EEE-INST-002), the designed shunt resistor power should be less than 1.8 W. With a maximum load current designed to be 10 A, the maximum power consumed by R_shunt is 1 W, which satisfies the requirement.



– Load voltage supply calculation:

$$V_{load} = V_{BUS} - I_{load} \times R_{shunt}$$

According to the previous equation, with the 10-mΩ (R_{shunt}) selected, V_{load} drops from 100 V to 99.9 V.

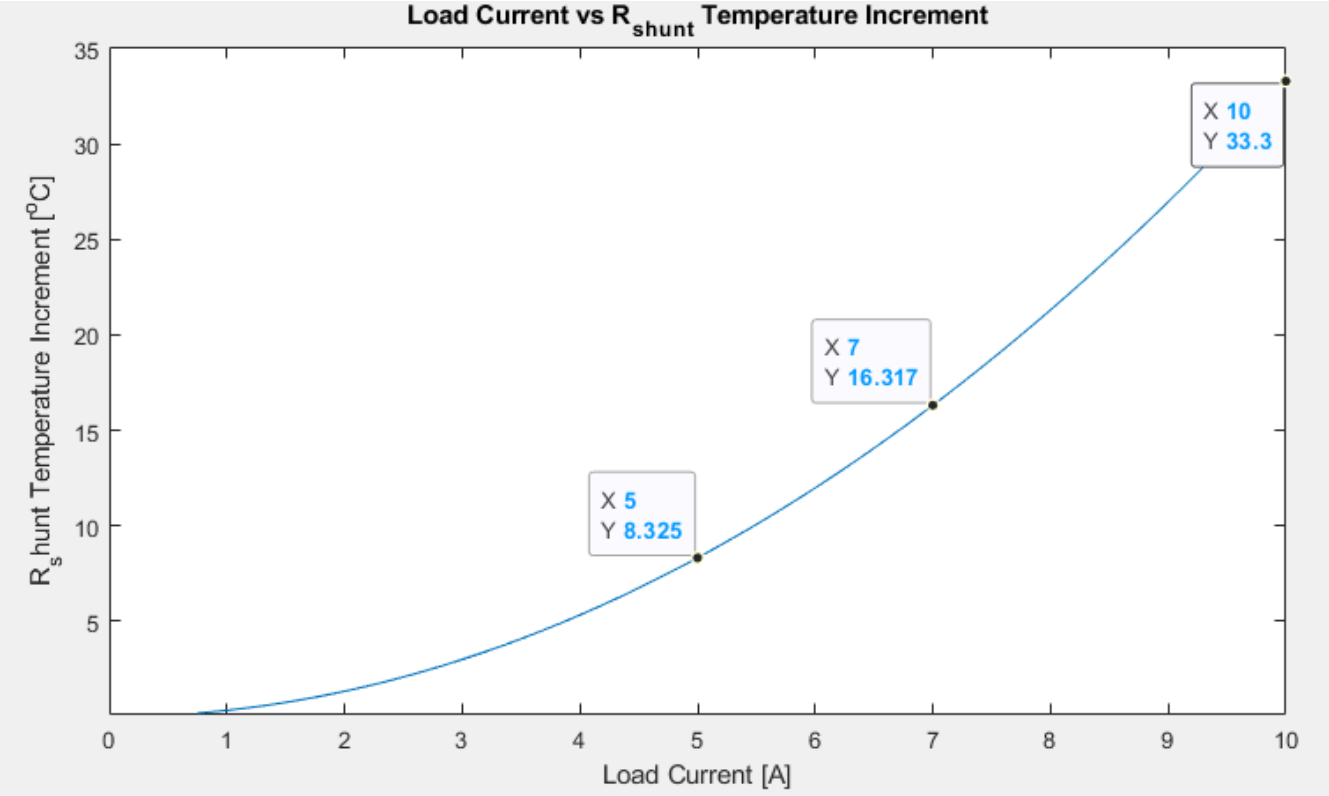
– Shunt resistor self-heating:

With the derating curve found in the shunt resistor data sheet, the self-heating coefficient (θ_{SH}) and shunt resistor temperature change (ΔT) are calculated using the following equations.

$$\theta_{SH} = \frac{T_{max} - T_{\max\_pwr100\%}}{PowerRating} = \frac{170°C - 70°C}{3\,W} = 33.3\,°C/W$$

$$\Delta T = \theta_{SH} \times P = \theta_{SH} \times I_{load}^2 \times R_{shunt} = 33.3\,\frac{°C}{W} \times I_{load}^2 \times 10\,m\Omega$$

Plugging the previous equations into the MATLAB tool, the relationship between the load current and temperature change is plotted in the following image. From the curve, the shunt resistor temperature is approximately 33.3°C higher than the surrounding temperature with a full load current of 10 A.



- **R_5, R_6, and R_3 Selection**
  - R_6 and R_3 calculation

$$V_{out} = \frac{R_3}{R_6} \times V_{sense} = \frac{R_3}{R_6} \times I_{load} \times R_{shunt}$$

$$Gain = \frac{V_{out}}{I_{load}} = \frac{R_3}{R_6} \times R_{shunt} = \frac{5\ V}{10\ A} = 0.5\ [V/A]$$

Based on the previous equations, to obtain a V_{out} range from 0 V to 5 V, with R_{shunt} equal to 10 mΩ, the ratio of R_3 to R_6 is calculated to be 50. There are 2 aspects to consider when picking values for R_5, R_6, and R_3:

1. To minimize the effect of op amp bias current, R_5 is chosen to be the same as R_6.
2. Increasing R_3 and R_6 could reduce power consumption but increase minimum V_{out} due to the effect of Zero Gate Voltage Drain Current (I_{DSS}) of the PMOS.

R_6 is set to be 49.9 Ω, and R_3 is determined to be 2.49 kΩ for the rest of the calculation. In this application, the Vishay® foil resistor models 303133 to 303138 are selected as a reference for simulation and error calculations. (See the *Design References* section.)

- **PMOS Selection**
  1. The absolute value of the threshold voltage $|V_{th}|$ of the PMOS needs to be small enough for the op amp to turn the PMOS gate on and off.
  2. The Zero Gate Voltage Drain Current (I_{DSS}) of the PMOS defines the leakage current when the gate voltage is equal to V_{bus}. I_{DSS} sets the lower V_{out} range.
  3. The PMOS gate capacitance could affect stability if wire resistance from the op amp output (V_o) to the gate is too large. This capacitance adds a zero in the 1/β curves. If the zero is located on the left of the point where 1/β and AoI intercept, the phase margin decreases. Hence, a small gate capacitance is preferred.
  4. Based on military standards, the drain-to-source breakdown voltage must be two times larger than the V_{bus}, a minimum of 200-V breakdown voltage is required.

PMOS Comparison

Parameter	IRF9230	IRHE9230	IRHN9250	IRHNJ597230
D-S Breakdown [V]	–200	–200	–200	–200
Vgs [V]	–2 to –4	–2 to –4	–2 to –4	–2 to –4
Zero Gate Voltage Drain Current [µA]	–25 to –250	–25 to –250	–25 to –250	–10 to –25
Input Capacitance [pF]	700	1200	4200	1344
Mounting Type	TH	SMT	SMT	SMT
Size [mm]	39.37 × 25.53	7.94 × 9.41	16 × 11.55	10.28 × 7.64

As shown in the PMOS *Comparison* table, IRHNJ597230 is selected because it has the smallest I_{DSS} and has relatively small package size and input capacitance.

- **Shunt Reference and R2 Selection**

  The shunt reference in the design is to create a virtual voltage supply of 95 V for the LMP7704-SP op amp. The maximum supply current for LMP7704 is 4.5 mA. Hence, the current range of the shunt reference selected must be greater than 4.5 mA.

  Shunt Reference Options lists the two shunt reference options for comparison. Both shunt references have a current range greater than 4.5 mA. The reverse breakdown voltage tolerance is not critical in this case, as long as the V_{EE} is around 95 V. Hence, even though the TL1431 has better performance in general, the LM4050QML is preferable because it has a smaller size and requires less components.

Shunt Reference Options

Parameter	TL1431-SP	LM4050QML-SP
Reverse Breakdown Voltage tolerance (%)	0.4	1.75
TID (krad)	100	100
Component Needed	5	3
Current Range (mA)	1 to 100	0.06 to 15
Mounting Type	SMT	SMT
Size (mm)	10.16 × 7.11	6.86 × 10.41

Since the LMP7704 drains a maximum of 4.5 mA, and the shunt reference selected requires at least 0.06 mA, the current through R2 is designed to be 4.75 mA. R2 is calculated with the following formula:

$$R2 = \frac{95\ V}{4.75\ mA} = 20\ k\Omega$$

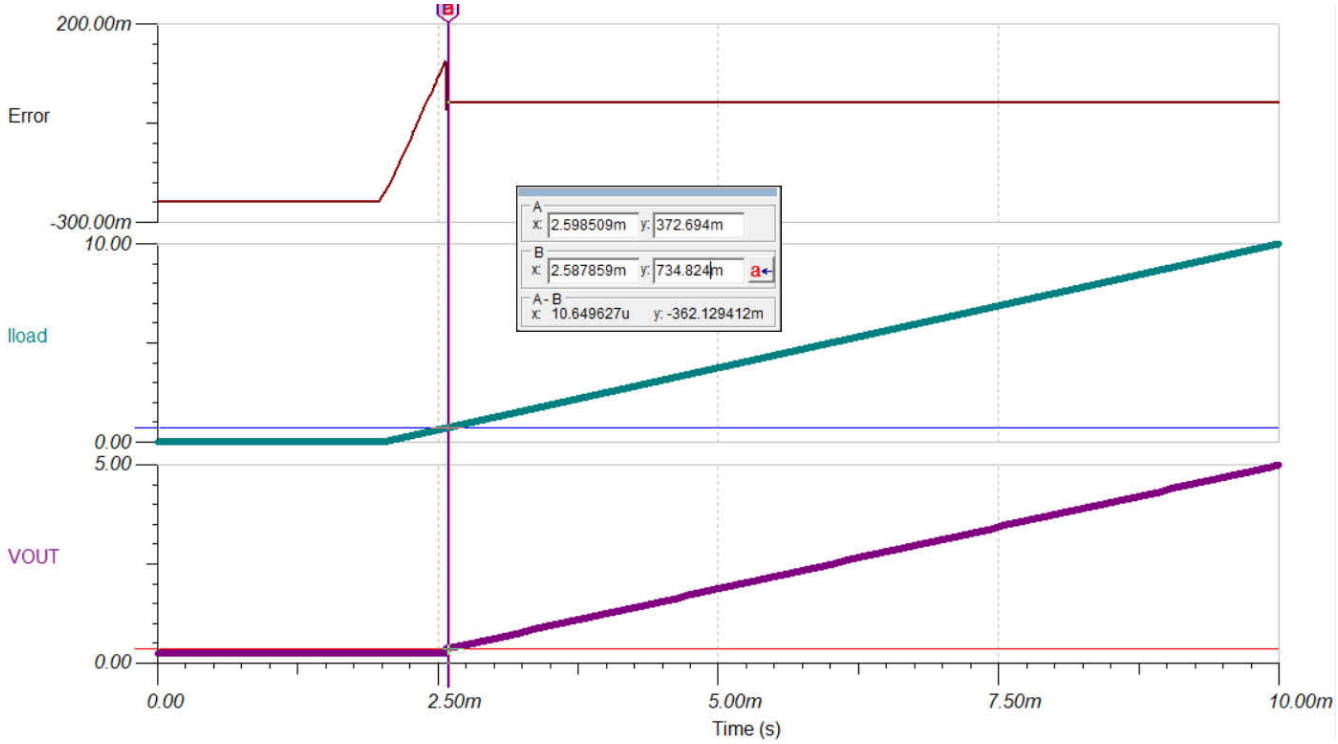
Design Simulations

- **Input and Output Ranges**

  The following plots show the output voltage across the 2.49-kΩ (R3) resistor. The error is calculated based on the following equation:

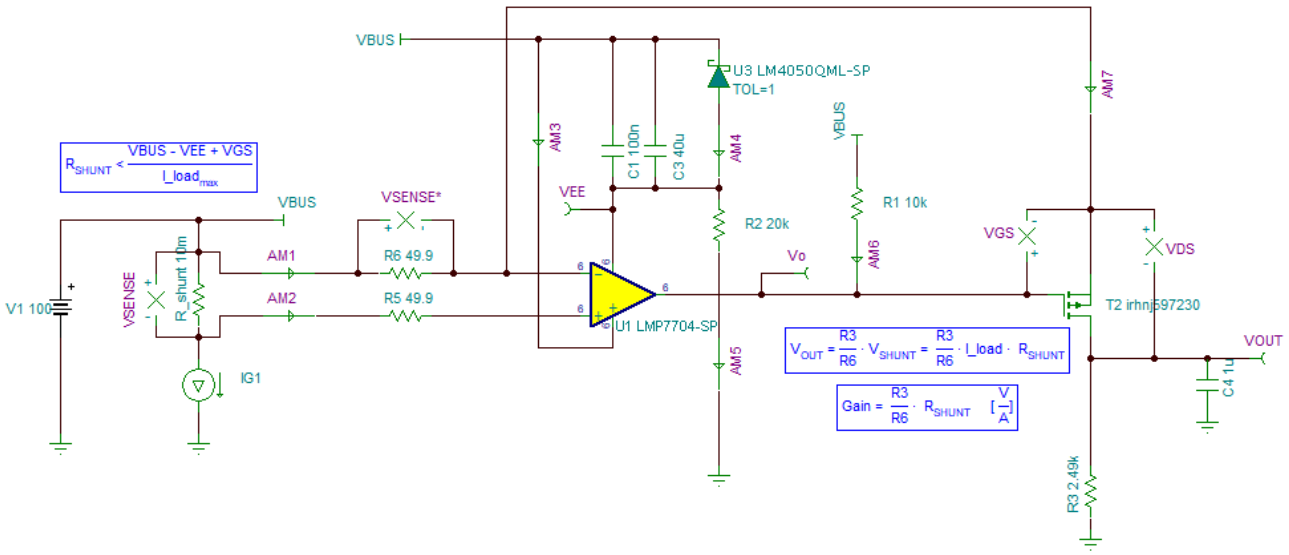
$$Error = \frac{I_{load} \times R_{shunt} \times R3}{R6} - Vout = \frac{I_{load} \times 0.01\ \Omega \times 2490\ \Omega}{49.9\ \Omega} - Vout$$

  Ideally, V_{out} swings from 0 V to 5 V as the load current (I_{load}) swings from 0 A to 10 A. However, the minimum of V_{out} is 373 mV and is non-linear before the load current (I_{load}) gets up to 735 mV.



- **Power Consumption**

  The following simulation and calculations show the power consumption of each component in the circuit with different load currents. Without considering the power consumption on the R_shunt, the overall power rate is from 471.4 mW to 651.3 mW. R2 dominates the power consumption.



P_PMOS	0.0199
P_R1	1.0201e-04
P_R2	0.4513
P_R3	9.9600e-05
P_R5	1.2144e-20
P_R6	1.9960e-06
P_Rshunt	0.0100
P_total_wo_Rshunt	0.4714

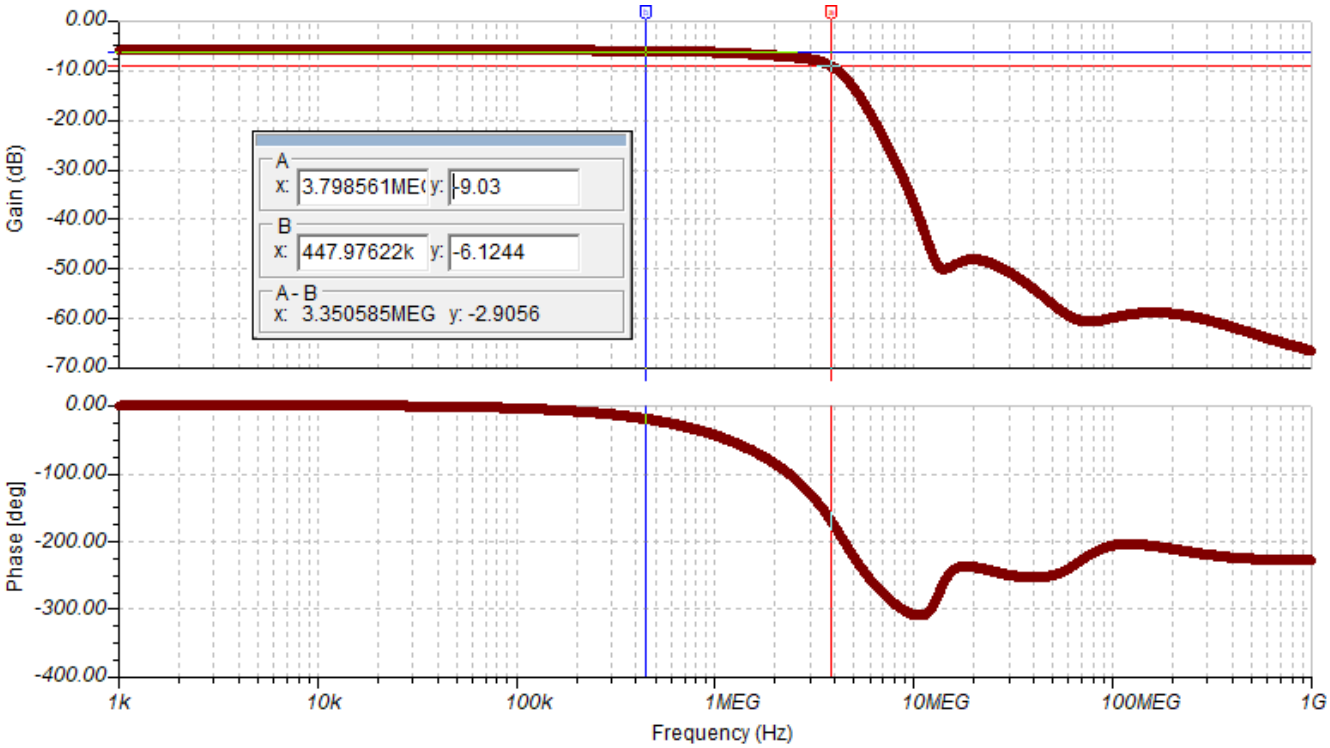
a) Power [W] Calculation with I_{load} = 1A

P_PMOS	0.1898
P_R1	1.2100e-04
P_R2	0.4513
P_R3	0.0100
P_R5	1.1834e-20
P_R6	1.9960e-04
P_Rshunt	1
P_total_wo_Rshunt	0.6513

b) Power [W] Calculation with I_{load} = 10A

- **Bandwidth**

  The following figure shows the gain of the circuit, where Gain = V_{out} (V) / I_{load} (A). With a load capacitance of 15 pF, the 1% full power bandwidth and the 3-dB bandwidth is found to be 478 kHz and 3.8 MHz.

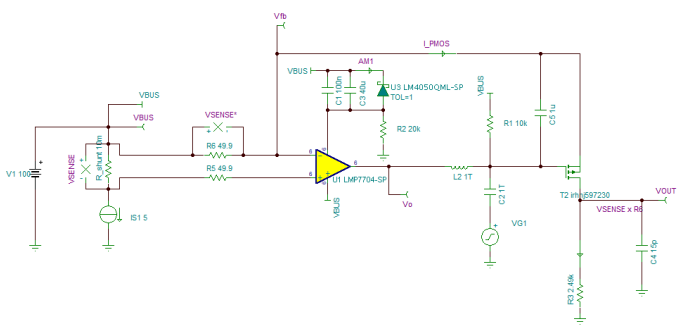


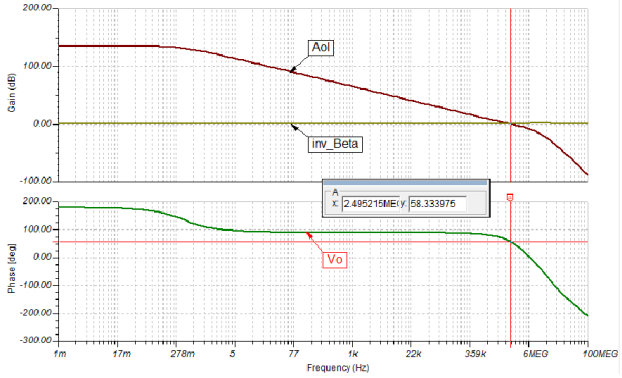
- **Stability Analysis**

  The stability of the system is verified by measuring its phase margin and applying a small signal-transient step response. To ensure stability, the phase margin, which is measured at a point where the Aol curve intersects 1/β, needs to be at least 45 degrees.

  As shown in the following schematic, a 1-µF capacitor is added in the feedback loop to increase stability. The following open-loop AC simulation breaks the loop at the input and the following equations are used to plot the relevant curves:

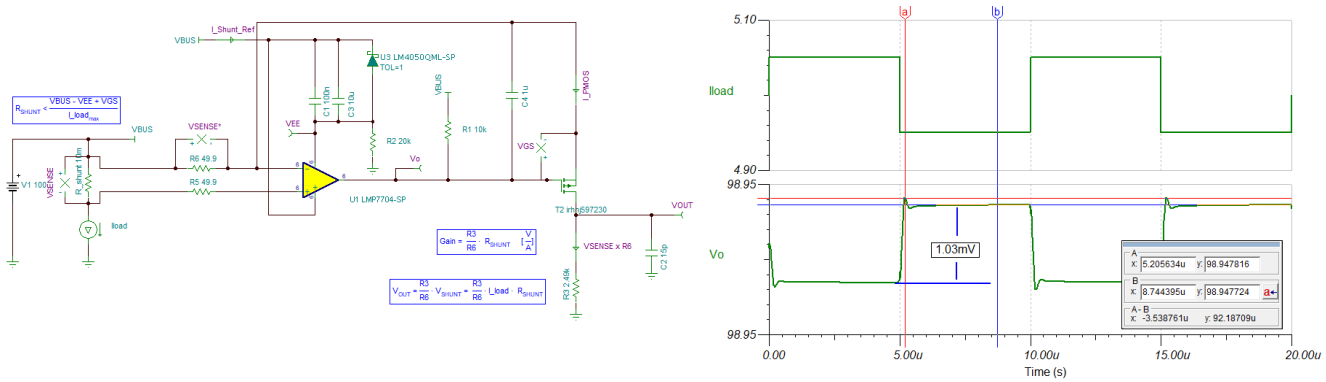
$$Aol = \frac{Vo}{Vfb} \qquad \frac{1}{\beta} = \frac{1}{Vfb} \qquad Aol \times \beta = Vo$$

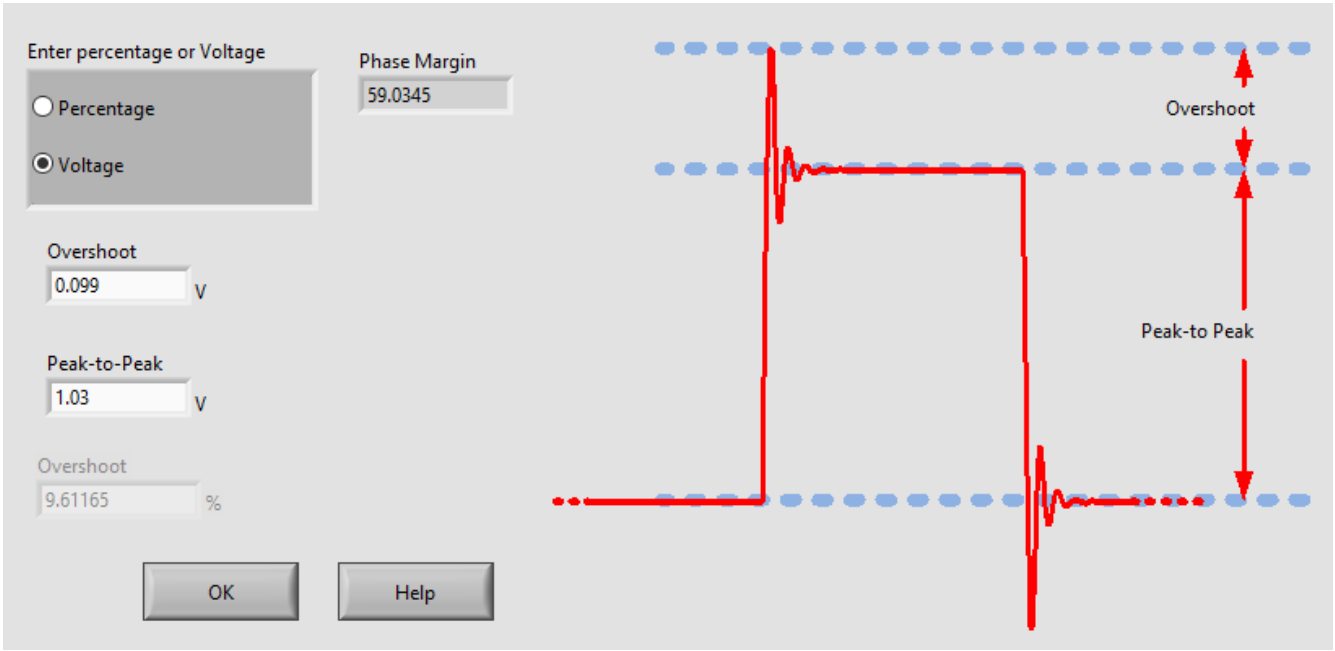




  The previous image shows the frequency domain simulation result. The phase margin is measured at a point where 1/β and Aol intercept, and it is 58.3 degrees, indicating the system is stable.

To further ensure stability, a small signal transient step response is applied at the input (IG1) of the circuit and percent overshoot is measured at Vo. The overshoot in the following image indicates a phase margin of 59 degrees, further confirming the stability of the system.



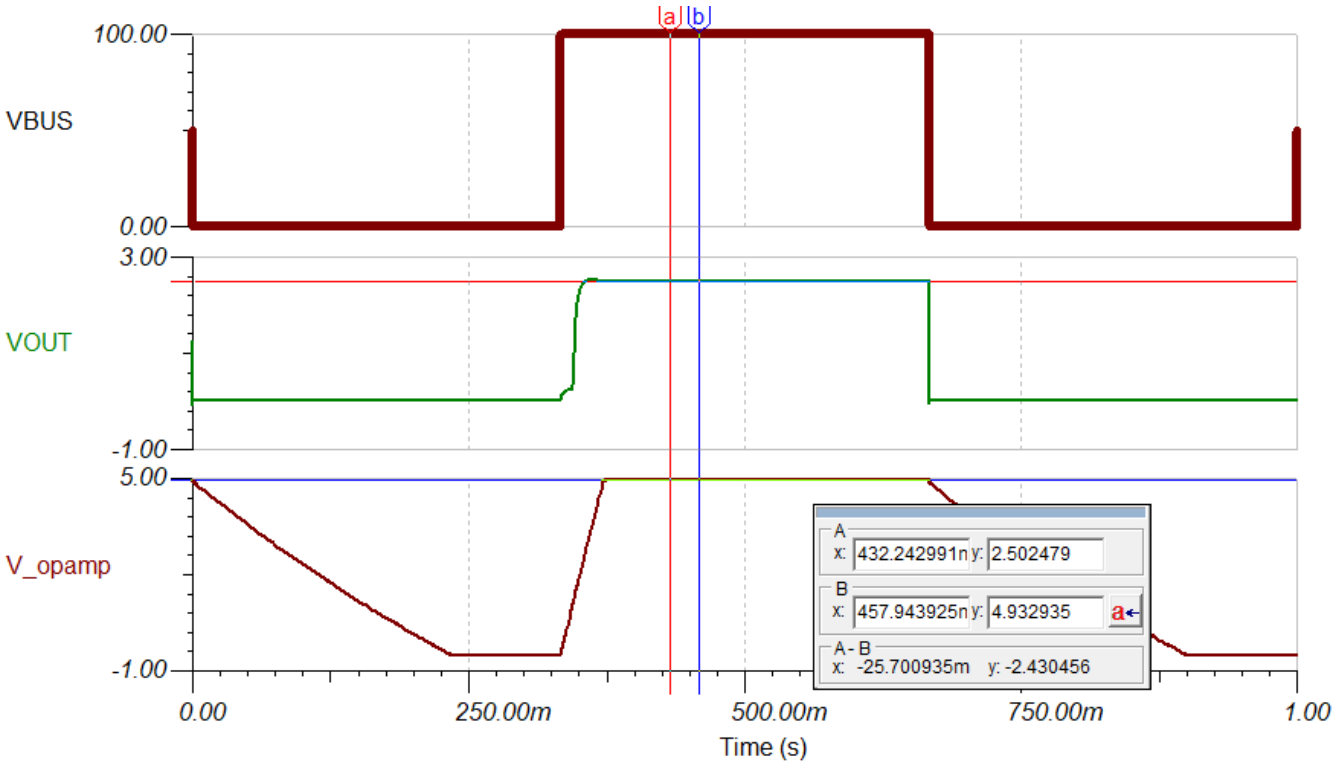


- **Fault Analysis**

> **CAUTION**
> If the LMP7704-SP op amp is damaged and the PMOS gate is left floating, this might destroy the microcontroller or ADC.

It is necessary to put a 10-kΩ pullup resistor (R1) in front of the PMOS gate to pull up the PMOS gate and protect the ADC or microcontroller.

Another fault consideration is whether the op amp (LMP7704-sp) will get damaged by the 100-V V_{bus}. To simulate it, a 100-V peak-to-peak square wave is applied to the V_{bus}. See the simulation results in the following image.



V_opamp, which is the difference between V_{bus} and VEE, is always below 4.933 V. LMP7704 is designed for a power supply up to 12 V, so it will not be damaged. Load current is set to 5 A in the simulation. As expected, V_{out} is simulated to be around 2.5 V.

- **Error Calculation**

  To analysis the output error of the circuit, the following parameters are needed

  - Vos: Op amp offset error (V)
  - Vos_drift: Offset drift (V/°C)
  - CMRR: Common-mode rejection ratio (dB)
  - PSRR: Power supply rejection ratio (dB)
  - temp: temperature (°C)
  - Vcm_sys: common-mode voltage (V), 5 V in this application
  - Vcm_ds: common-mode voltage used for testing in the data sheet (V).
  - R1: R6 resistor value (Ω)
  - R_shunt: Shunt resistor value (Ω)
  - Rshunt_tol: Shunt resistor tolerance (%)
  - TC_shunt: Shunt resistor temperature coefficient (ppm/°C)
  - I_{load}: Load current (A)
  - I_b: Input bias current (A)
  - R1_tol: R6 resistor tolerance (%)
  - TC1: R6 resistor temperature coefficient (ppm/°C)
  - R2_tol: R3 resistor tolerance (%)
  - TC2: R3 resistor temperature coefficient (ppm/°C)

Offset error:

$$V_{sense} = R\_shunt \times I_{load}$$

$$e_{Vos} = \frac{(Vos + Vos\_drift \times (temp - 25))}{V_{sense}} \times 100\%$$

CMRR error:

$$CMRR\_ = 10^{-\frac{CMRR}{20}}$$

$$e_{CMRR} = \frac{abs(Vcm\_sys - Vcm\_ds) \times CMRR\_}{V_{sense}} \times 100\%$$

PSRR error:

$$PSRR\_ = 10^{-\frac{PSRR}{20}}$$

$$e_{PSRR} = \frac{abs(Vcm\_sys - Vcm\_ds) \times PSRR\_}{V_{sense}} \times 100\%$$

Shunt resistor error:

$$e_{shunt} = \frac{Rshunt\_tol \ + \ TC\_shunt}{10000} \times (temp - 25)$$

Resistor (R3 and R6) error:

$$e_{R1} = \frac{R1\_tol \ + \ TC1}{10000} \times (temp - 25)$$

$$e_{R2} = \frac{R2\_tol \ + \ TC2}{10000} \times (temp - 25)$$

Bias current error:

$$e_{biasCurr} = \frac{I\_b \times R1}{V_{sense}} \times 100\%$$

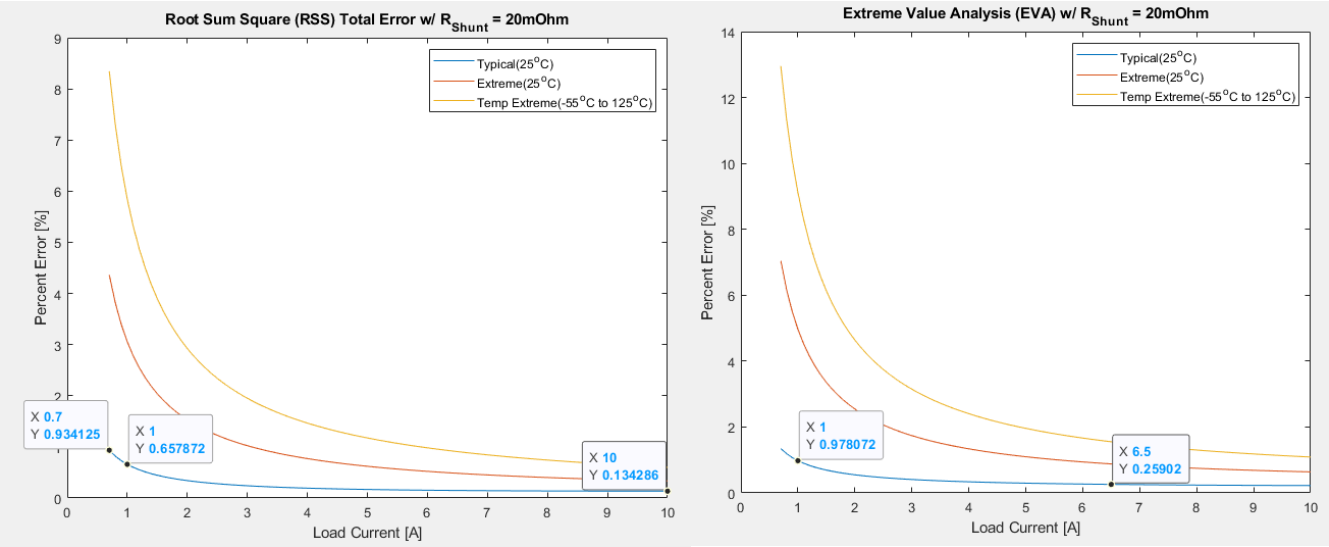
Root Sum Square (RSS) total error:

$$RSS \ = \sqrt{e_{Vos}^2 + e_{CMRR}^2 \ + e_{PSRR}^2 + e_{shunt}^2 \ + e_{R1}^2 + e_{R2}^2 + e_{biasCurr}^2}$$

Extreme Value Analysis (EVA):

$$EVA = e_{Vos} + e_{CMRR} + e_{PSRR} + e_{shunt} + e_{R1} + e_{R2} + e_{biasCurr}$$

The previous error equations are implemented in MATLAB, and the simulation result is shown in the following image.



The RSS is 0.658% when the load current is 1 A. This RSS satisfies the 0.7% error requirement. The EVA plot is also provided on the right as a reference.

e_bias_curr	1.5000e-07
e_CMRR	0.0079
e_PSRR	0.2500
e_R1	0.0100
e_R2	0.0100
e_shunt	0.1002
e_Vos	0.6000

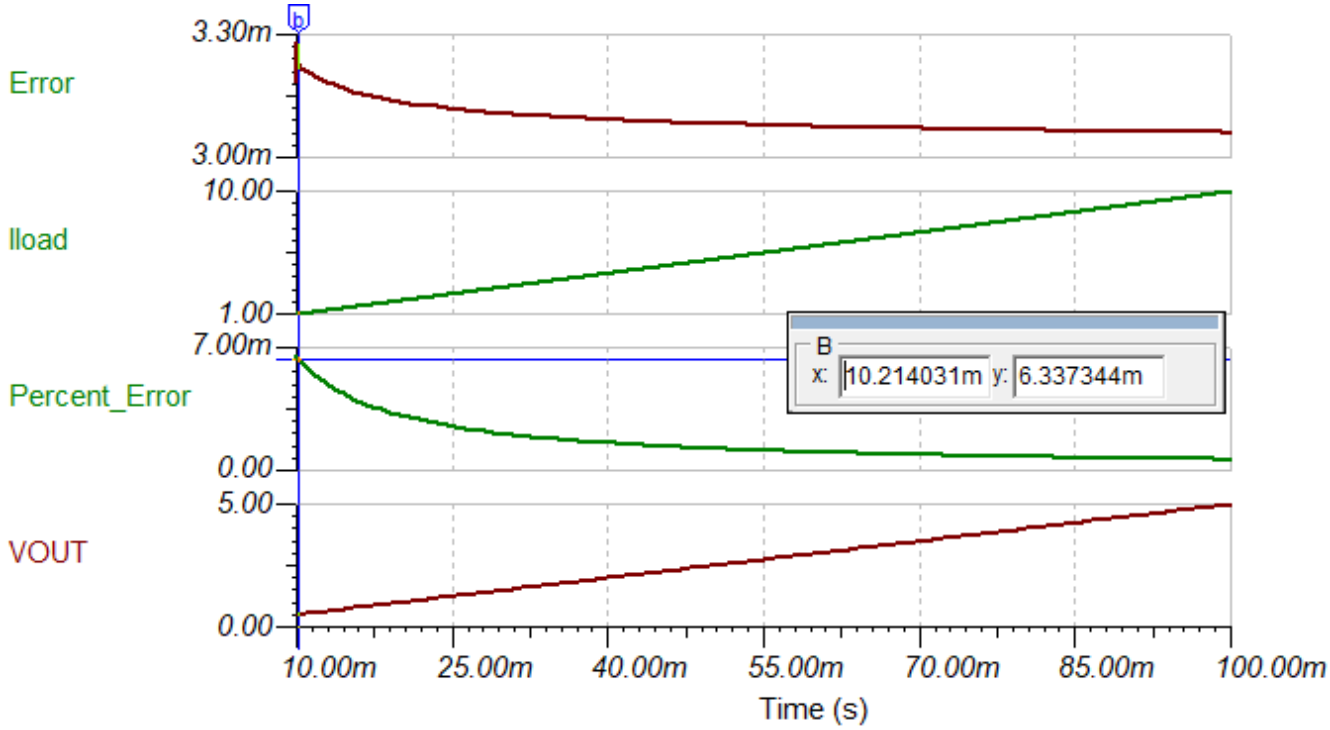
a) Error with I_{load} = 1A, unit in [%]

e_bias_curr	1.5000e-08
e_CMRR	7.9057e-04
e_PSRR	0.0250
e_R1	0.0100
e_R2	0.0100
e_shunt	0.1167
e_Vos	0.0600

b) Error with I_{load} = 10A, unit in [%]

The previous result is calculated with R_shunt set to 10 mΩ. When the load current is 1 A, the op amp Vos dominates the error. When load current is 10 A, the shunt resistor tolerance dominates the error.

The previous error calculation is verified again with TINA-TI™ simulation, and the result is shown in the following image.



The percent error is calculated with the following equation.

$$Percent\_Error = \frac{I_{load} \times 10\ m\Omega \times \frac{2.49\ k\Omega}{49.9\ \Omega} - Vout}{I_{load} \times 10\ m\Omega \times \frac{2.49\ k\Omega}{49.9\ \Omega}} \times 100\%$$

As shown in the simulation, when the load current is 1 A, the error is 0.63%. This error is consistent with the 0.6% Vos error in the previous MATLAB calculation. TINA-TI™ does not simulate the error caused by resistor tolerance and changing temperature on the shunt resistor.

Design References

1. Aaron Schultz, “High-Side Current Sensing,” analog.com, Mar, 2018. [Online]. Available: https://www.analog.com/en/analog-dialogue/raqs/raq-issue-151.html. [Accessed Sept. 9, 2021].
2. Sahu, K., and Leidecker, H. (April 2008). EEE-INST-002: Instructions for EEE Parts Selection, Screening,Qualification, and Derating. Retrieved from https://nepp.nasa.gov/DocUploads/FFB52B88-36AE-4378-A05B2C084B5EE2CC/EEE-INST-002_add1.pdf
3. Texas Instruments, *Space-Grade, 100-krad, Voltage-Controlled Current Sink (0–200 mA) Circuit* application note
4. VISHAY, “Model 303337 Bulk Metal® Foil Technology CSM3637F, with Screen/Test Flow in Compliance with EEE-INST-002,” Model 303337 data sheet [Revised Jul. 2020].
5. Texas Instruments, *LM4050QML Precision Micropower Shunt Voltage Reference* data sheet
6. IR HiRel, “RADIATION HARDENED POWER MOSFET SURFACE MOUNT (SMD-0.5),” IRHNJ597230 data sheet, Dec 2018.
7. VISHAY, “Bulk Metal® Technology High Precision, Current Sensing, Power Surface Mount, Metal Strip Resistor,” CMS Series data sheet. [Revised Jan. 2021].

Design Featured Op Amp

LMP7704-SP	
V_{ss}	2.7 V to 12 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	±60 µV
I_q	2.9 mA
I_b	±1 pA
UGBW	2.5 MHz
SR	1 V/µs
#Channels	4
Total Ionizing Dose (TID)	100 krad (Si)
Single Event Latch-up (SEL) Immunity	85 MeV·cm^2/mg
LMP7704-SP	

Design Alternate Op Amp

LM124AQML-SP	
V_{ss}	3 V to 32 V
V_{os}	2 mV
I_b	45 nA
UGBW	1 MHz
SR	0.1 V/µs
#Channels	4
Total Ionizing Dose (TID)	100 krad (Si)
SEL Immunity	SEL Immune (Bipolar process)
LM124AQML-SP	

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