Analog Engineer's Circuit

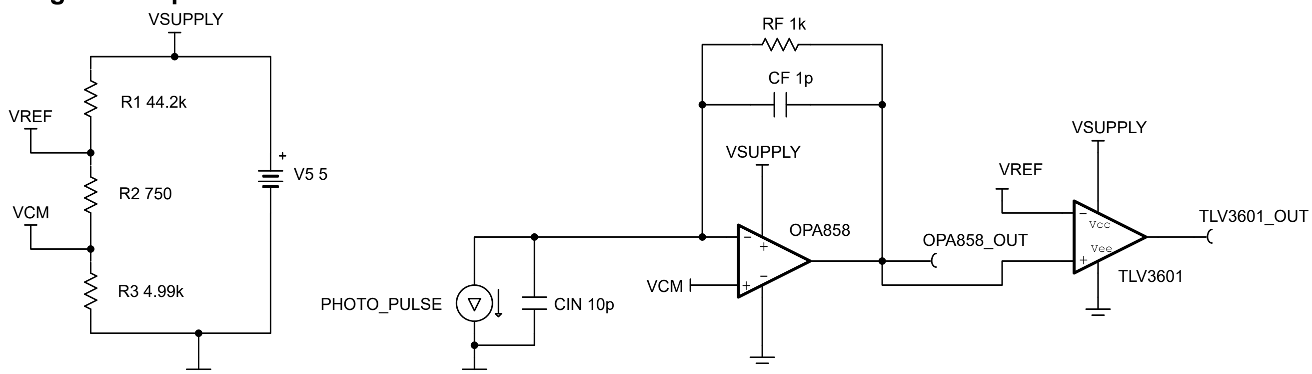
LiDAR Receiver Comparator Circuit

Amplifiers

Design Goals

System Supply	Photodiode Input Current Pulse Width	Transimpedance Amplifier		Output Type	Maximum Propagation Delay
5 V	3 ns	High Bandwidth	100-mV output swing	Single-ended	4 ns

Design Description



LiDAR Receiver Circuit

This circuit must be able to detect a 3-ns pulse received on a photodiode from a light pulse. To do this, a transimpedance amplifier and a high-speed comparator are required. To meet the propagation delay requirement, this design uses the OPA858 5.5-GHz gain bandwidth product, decompensated transimpedance amplifier with FET inputs and the TLV3601 2.5-ns high-speed rail-to-rail comparator with push-pull outputs.

Design Notes

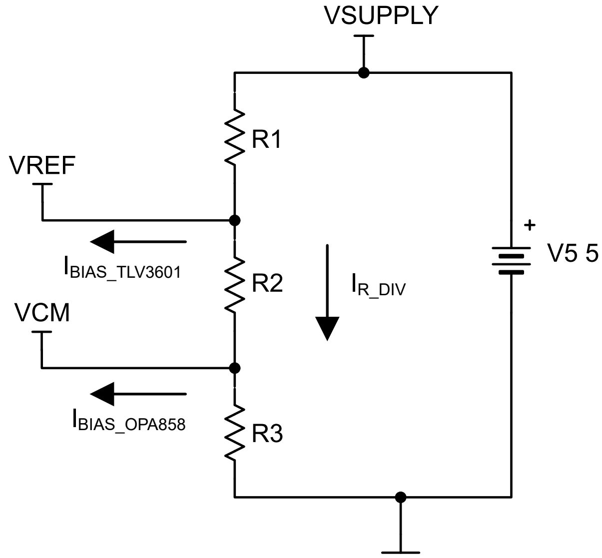
1. Select a high-speed comparator that has narrow pulse width detection capability better than 3 ns
2. Derive the reference for the transimpedance amplifier and comparator from the same voltage source
3. Verify stability of the transimpedance amplifier configuration with selected photodiode

Design Steps

Step 1: Configuring the TIA Common-Mode Voltage and the Comparator Reference Voltage

One of the goals of this design is to operate from a single, 5-V supply. This design uses a three-resistor divider network to establish the common-mode output voltage and the comparator reference voltage.

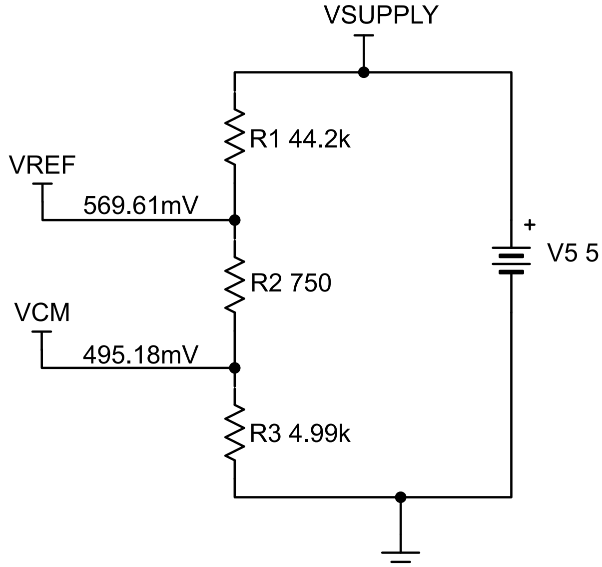
The important thing to note for this resistive divider network is to consider the input bias currents of both the OPA858 and TLV3601 devices. Since the OPA858 has an ultra-low bias current of 10 pA, the largest source of error comes from the TLV3601. The input bias current of the TLV3601 is typically 1 µA which means that the current through the divider network should be at least 100 times larger to maintain the desired reference voltages. With a 5-V supply and a current of 100 µA, the maximum total resistance for this network is 50 kΩ.



Effect of Input Bias Currents on Resistor Divider Network

For this design, the common-mode voltage of the OPA858 is set to 500 mV, a bias voltage within the recommended common-mode range for the OPA858. To do this, divide 500 mV by the 100 µA desired divider current. This gives a value for R3 of 5 kΩ but 4.99 kΩ was used for this design.

To comply with the design requirements, the OPA858 output will swing 100 mV. With the 500-mV output common-mode established, the comparator threshold voltage must be in the range of 500 mV to 600 mV. The TLV3601 threshold is 575 mV for this design. To provide an additional 75 mV from the 500-mV reference, R2 must be 750 Ω with the total branch current still being 100 µA.



Complete Resistor Divider Network With DC Nodal Voltages

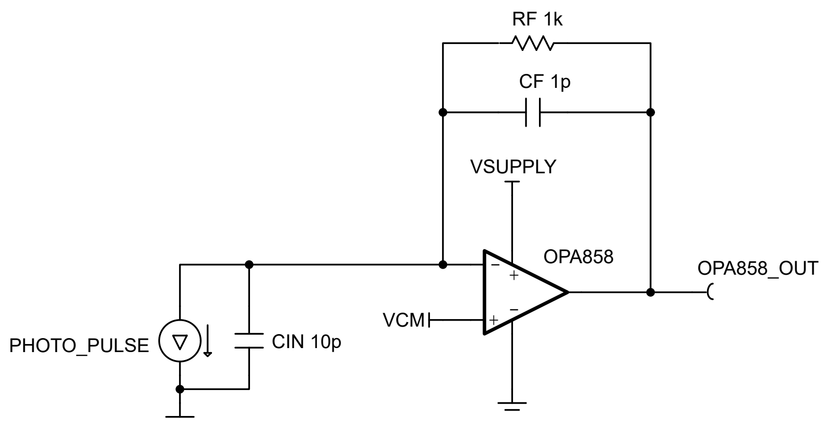
To adhere to the maximum resistance and minimum current requirement, R1 was selected to be 44.2 kΩ. This gives a total resistance of 49.94 kΩ.

Step 2: Configuring the OPA858 Transimpedance Amplifier

With a 100-µA pulse of current through the feedback branch of the OPA858, a 1-kΩ feedback resistance is required to produce a 100-mV swing on the output.

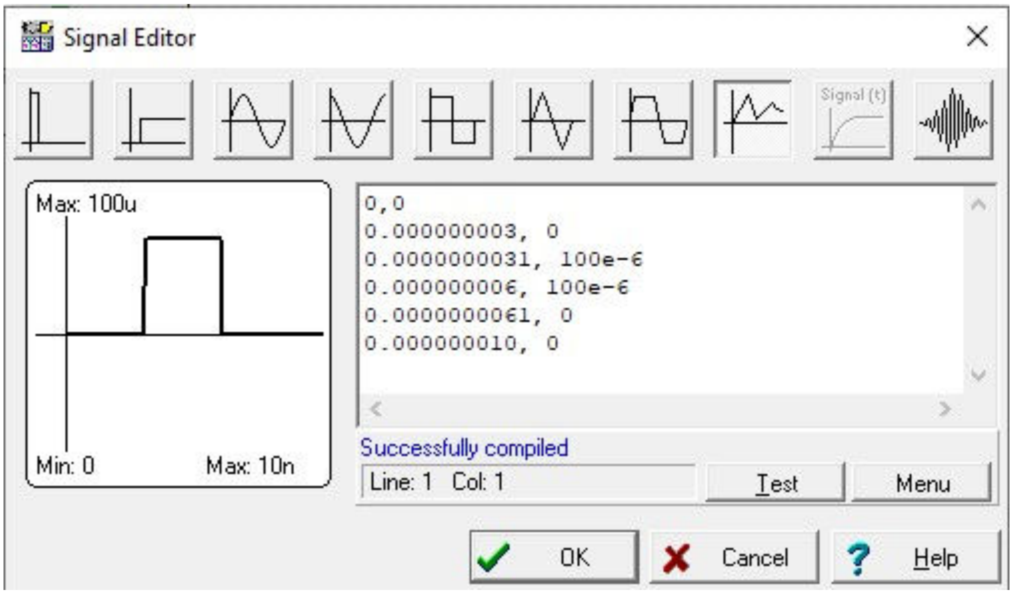
For this application, a 3-ns light pulse is received as a 100-µA current pulse. Assuming at most one, 3-ns pulse in a 10-ns window, the total period of our input is 10 ns. A 10-ns period corresponds to a 100-MHz signal. To select the feedback capacitor, first consider the pole frequency of a feedback network with a capacitor and resistor in parallel. The rough pole frequency is expressed as follows:

$$f_P = \frac{1}{2\pi \times R_F \times C_F}$$



OPA858 and Photodiode Completed Front-End Circuit

With a 1-pF capacitor in the feedback loop and a 1-kΩ feedback resistor, the pole frequency is approximately 159 MHz. The input signal is within the bandwidth of the feedback impedance. Additional stability analysis is also required for the transimpedance amplifier circuit and the metrics used to check for stability were rate of closure (ROC) and phase margin. For further information on stability analysis see the *Op Amps: Stability - Phase Margin* and *Op Amps: Stability - Spice Simulation* TI Precision Labs training videos.

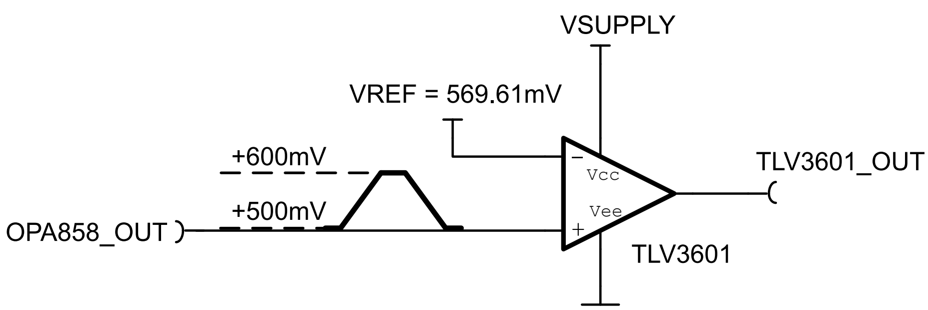


Input Signal Piecewise Configuration for 3-ns, 100-µA Pulse

To mimic the behavior of a photodiode receiving a 3-ns pulse of light, a piecewise current generator is configured to pulse 100 µA for 3 ns in a 10-ns period. The parallel input capacitance is set to 1 pF. For more information on a photodiode equivalent model see the *1 MHz, Single-Supply, Photodiode Amplifier Reference Design*.

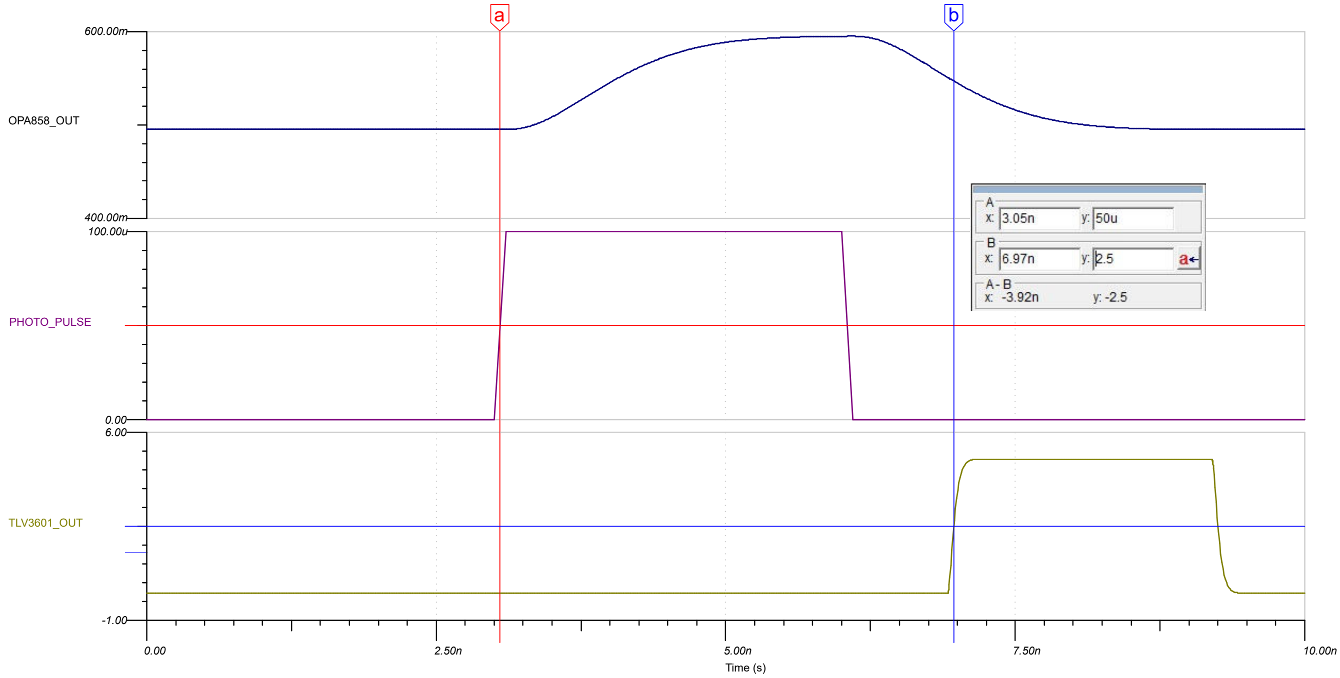
Step 3: Configuring the TLV3601 High-Speed Comparator With Push-Pull Outputs

This design uses the TLV3601 high-speed comparator in a non-inverting configuration. To configure the comparator, connect the voltage node above R2 to the inverting input and designate it VREF. Connect the same 5-V supply used for the OPA858 and connect the VEE pin to ground. The input common-mode range with a 5-V supply is –0.3 V to 5.3 V. With one of the inputs swinging from 500 mV to 600 mV and VREF being 569.6 mV, both inputs adhere to the input common-mode range of the TLV3601. If extra hysteresis is required to avoid output chatter due to noise or input signal conditions, then use the TLV3603. The TLV3603 has an extra hysteresis pin if hysteresis is required for an application.



TLV3601 Inputs and Connections

Simulation Results



Measured Propagation Delay from Input Pulse Measured at 3.92 ns

Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See the *LVDS GaN Driver Transmitter Circuit With High-Speed Comparator*.

See the *Non-inverting comparator with hysteresis circuit*.

Circuit SPICE simulation file: SNOM742.

For more information on many comparator topics including hysteresis, propagation delay, and input common-mode range, see *TI Precision Labs - Op amps*.

Design Featured Comparator

TLV3601	
V_s	2.4 V to 5.5 V
V_{inCM}	V_{EE} – 0.2 V to VCC + 0.2 V
V_{IO} (input offset voltage at 25°C) (maximum)	±0.5 mV
I_q	4.9 mA
T_{PD}	2.5 ns
Input Bias Current (Typical)	1 µA
Output type	Push-Pull
TLV3601	

Design Alternate Comparator

TLV3603	
V_s	2.4 V to 5.5 V
V_{inCM}	V_{EE} – 0.2 V to VCC + 0.2 V
V_{IO} (input offset voltage at 25°C) (maximum)	±0.5 mV
I_q	5.7 mA
T_{PD}	2.5 ns
Input Bias Current (Typical)	1 µA
Output type	Push-Pull
Features	Adjustable Hysteresis and Latch Function
TLV3603-Q1	