Analog Engineer's Circuit

LVDS GaN Driver Transmitter Circuit With High-Speed Comparator

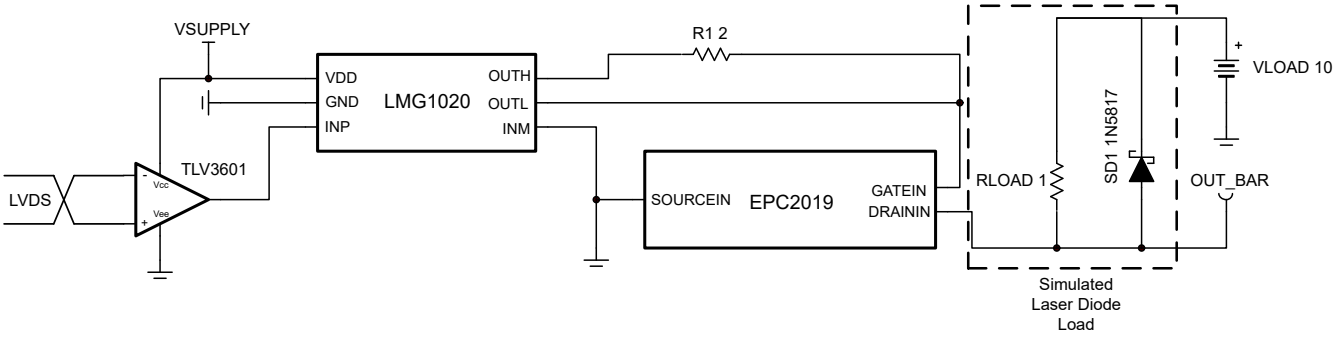
Amplifiers

Design Process

Design Goals

System Supply	Input Type	Output Pulse Width 50% to 50% to Drive LED	FET Switch Type
5 V	LVDS	3 ns ±10%	Low-Side

Design Description



LVDS GaN Driver Transmitter Circuit

For this application, it is crucial to produce as narrow of a pulse as possible when driving a laser diode. For this design, the output of the GaN FET produces a 3-ns wide pulse that can be used to control a low-resistance, 1-Ω load. It is common to use low-voltage differential signal (LVDS) on a long cable or long trace to reduce EMI. The inputs to the GaN FET driver interface circuit must also accept LVDS inputs. To provide speed and accept LVDS input signals, the TLV3601 high-speed comparator is used. The TLV3601 is used to convert an LVDS signal to a single-ended output to drive the input of a GaN FET driver. The EPC2019 GaN FET and the LMG1020 GaN FET driver are also used. The design requirements are reflected in the Design Goals table.

Design Notes

1. Select a high-speed comparator that can be driven differentially by an LVDS signal
2. The low-resistance, 1-Ω load is used in simulation in place of an LED
3. Both the TLV3601 and the LMG1020 devices are powered from a 5-V supply (VSUPPLY)

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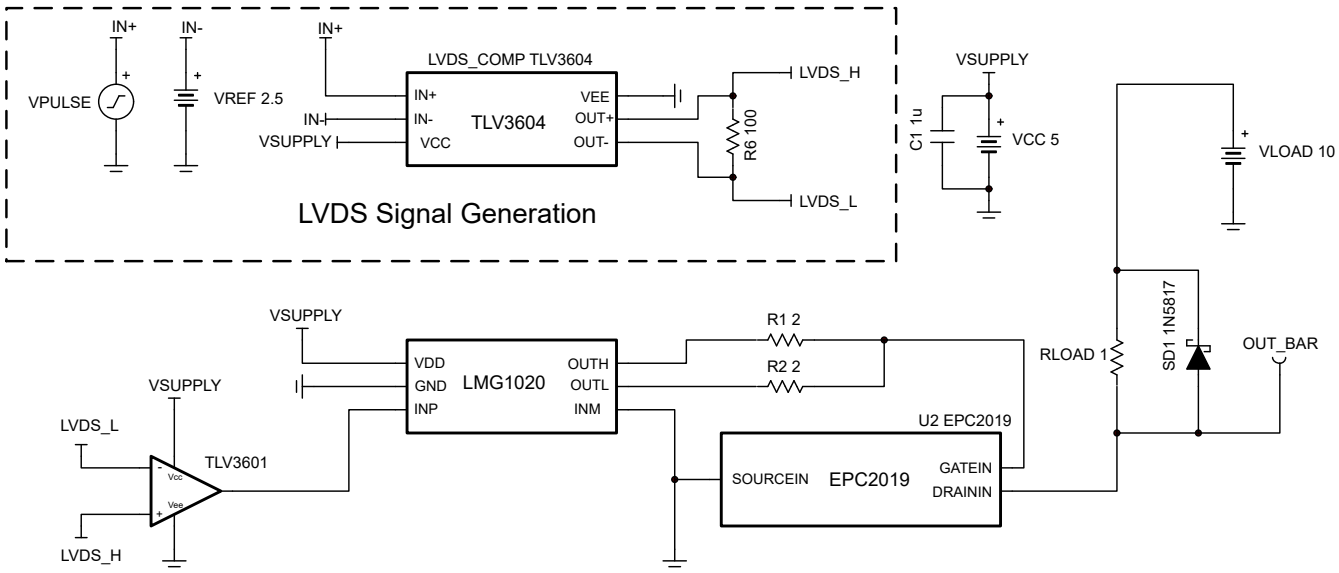
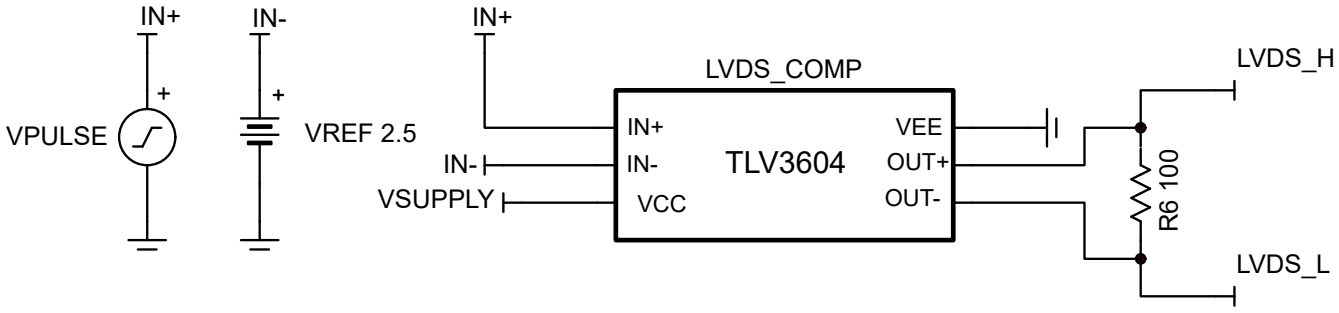
Design Steps



Complete Design Circuit

Step 1: LVDS Generation Using the TLV3604

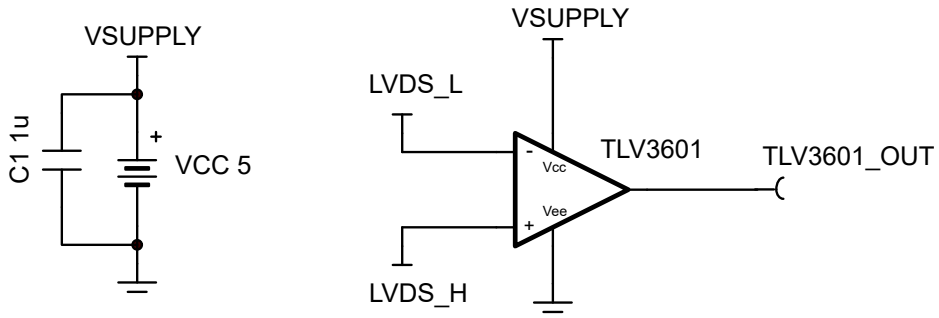
The TLV3604 non-inverting input is driven by a 100-mV, 3-ns pulse with a 2.5-V DC offset (VPULSE).



LVDS Generation Using the TLV3604

Step 2: LVDS to Single-Ended Output Conversion Using the TLV3601

The LVDS outputs of the TLV3604 (LVDS_H and LVDS_L) are used to drive the inputs of the TLV3601. Since the outputs of the TLV3604 are terminated with a 100-Ω load, the voltage across this load can differentially drive the input of the TLV3601.



Connecting the TLV3601

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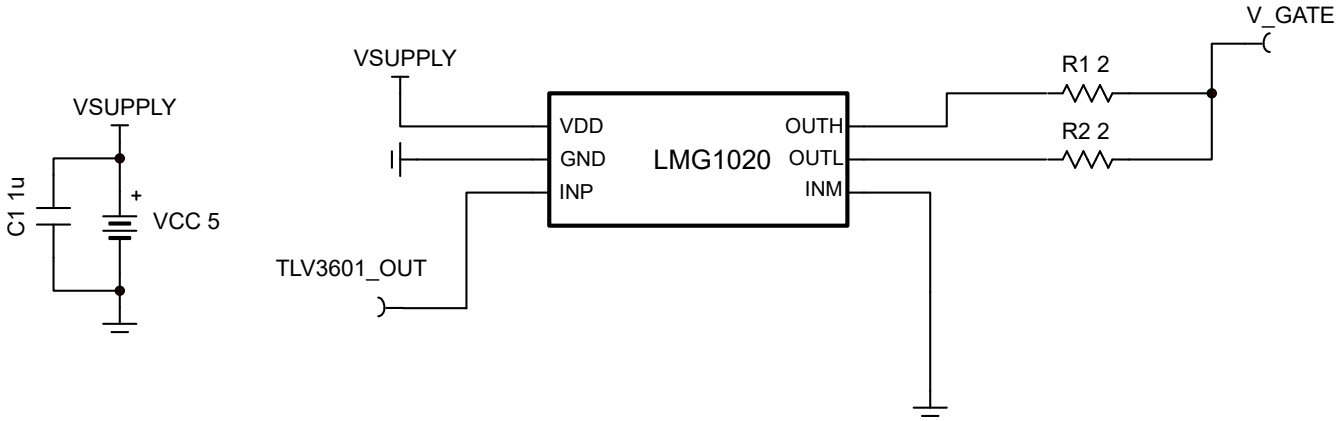
Step 3: Configuring the GaN FET Driver

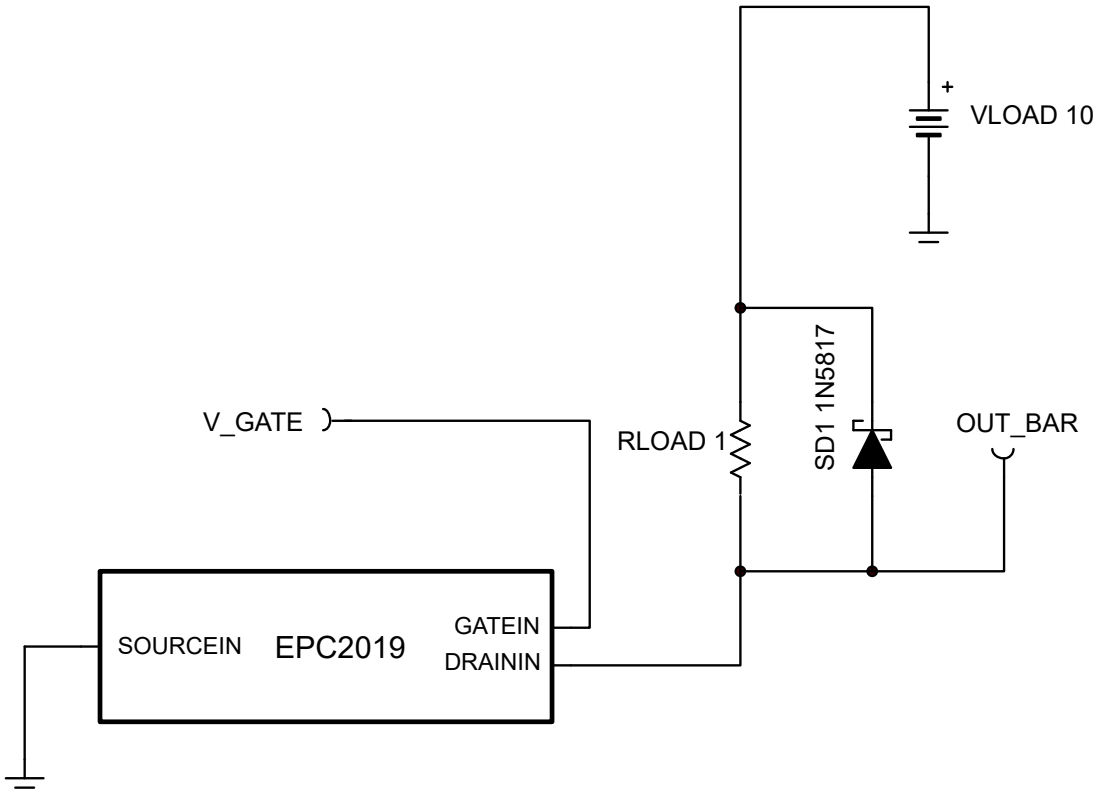
The LMG1020 enable pin (INM in the TINA simulation model) is active low and thus can be left grounded to keep the LMG1020 enabled. The series resistances on the outputs follow the *LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-ns Pulse Width Applications* data sheet recommended minimum value of 2 Ω in the *Typical Applications* section. The shorted outputs then drive the gate of the EPC2019 GaN FET (V_GATE). The LMG1020 input is driven by the output of the TLV3601 (TLV3601_OUT).



LMG1020 Configuration

Step 4: Connecting the EPC2019 GaN FET

The GaN FET controls the 10-V supply current through the 1-Ω load. As a safety feature, a Schottky diode was placed in parallel with the load to ensure that the voltage across the load does not exceed 20 V.



Low-Side GaN FET Connections

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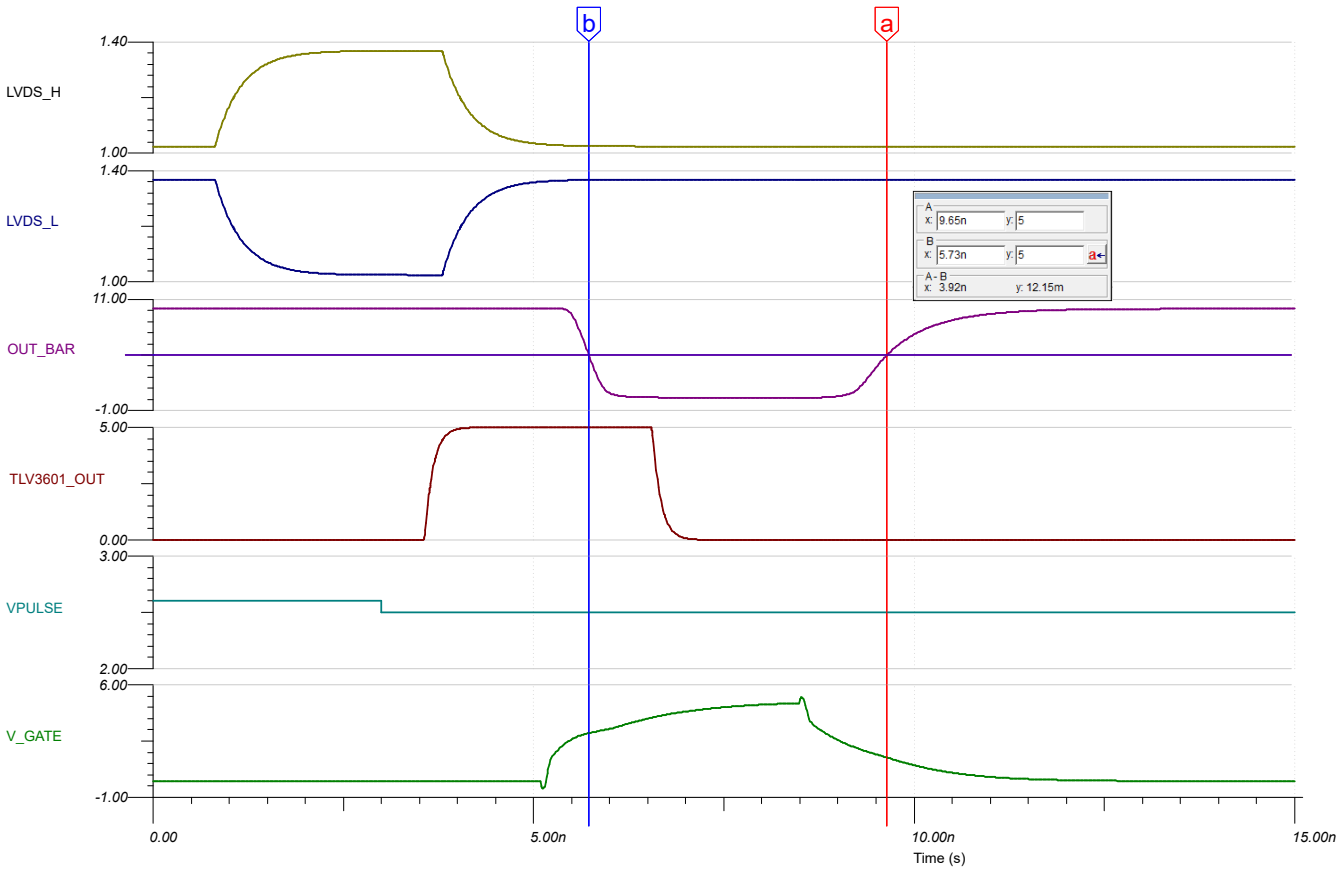
Transient Simulation Results

Using the “VPULSE” pulse waveform generator feeding into the TLV3604, the voltage below the 1-Ω load resistance is monitored as *OUT_BAR*. When the gate of the GaN FET is sufficiently driven, the voltage evident at the drain is approximately 0 V. The following image shows the initial simulation results.



Initial Simulation Results

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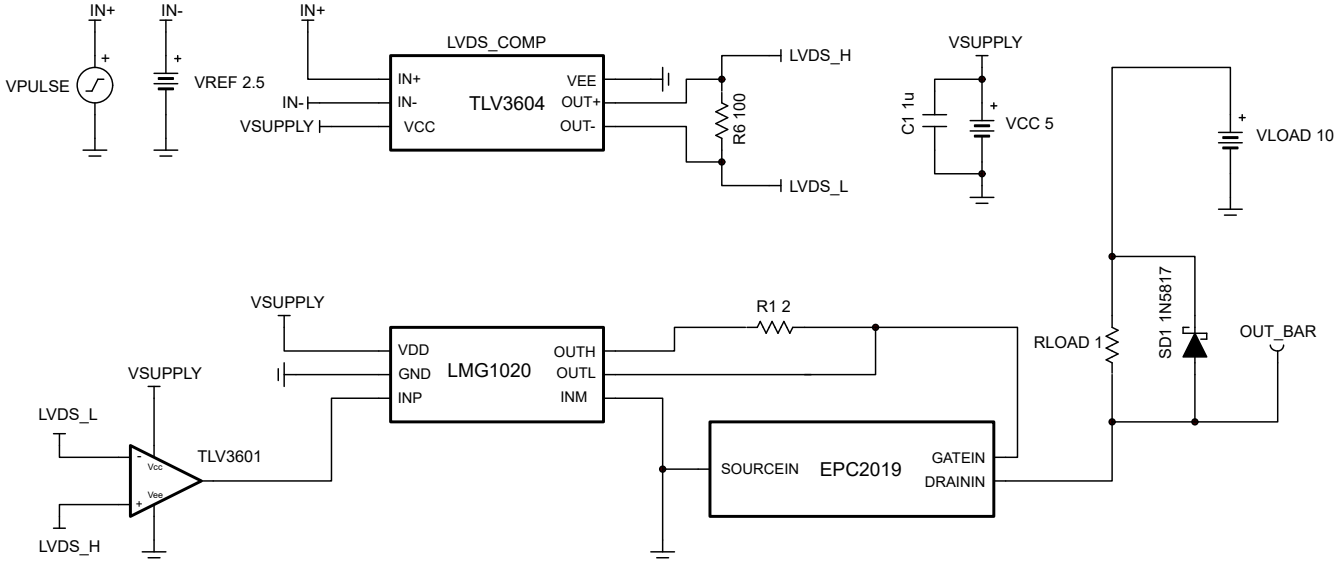
As depicted by Initial Simulation Results, the pulse width is approximately 0.6 ns wider than the design requirement at 3.92 ns. This is partly due to the series resistances on the gate of the EPC2019 that are used to avoid voltage overstress due to inductive ringing. To improve the turn-off time of the GaN FET Driver and GaN FET, the OUTL output of the LMG1020 is shorted to the gate of the EPC2019 as recommended in the *Typical Applications* section of the *LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-ns Pulse Width Applications* data sheet.



Modified Schematic to Improve Pulse Width

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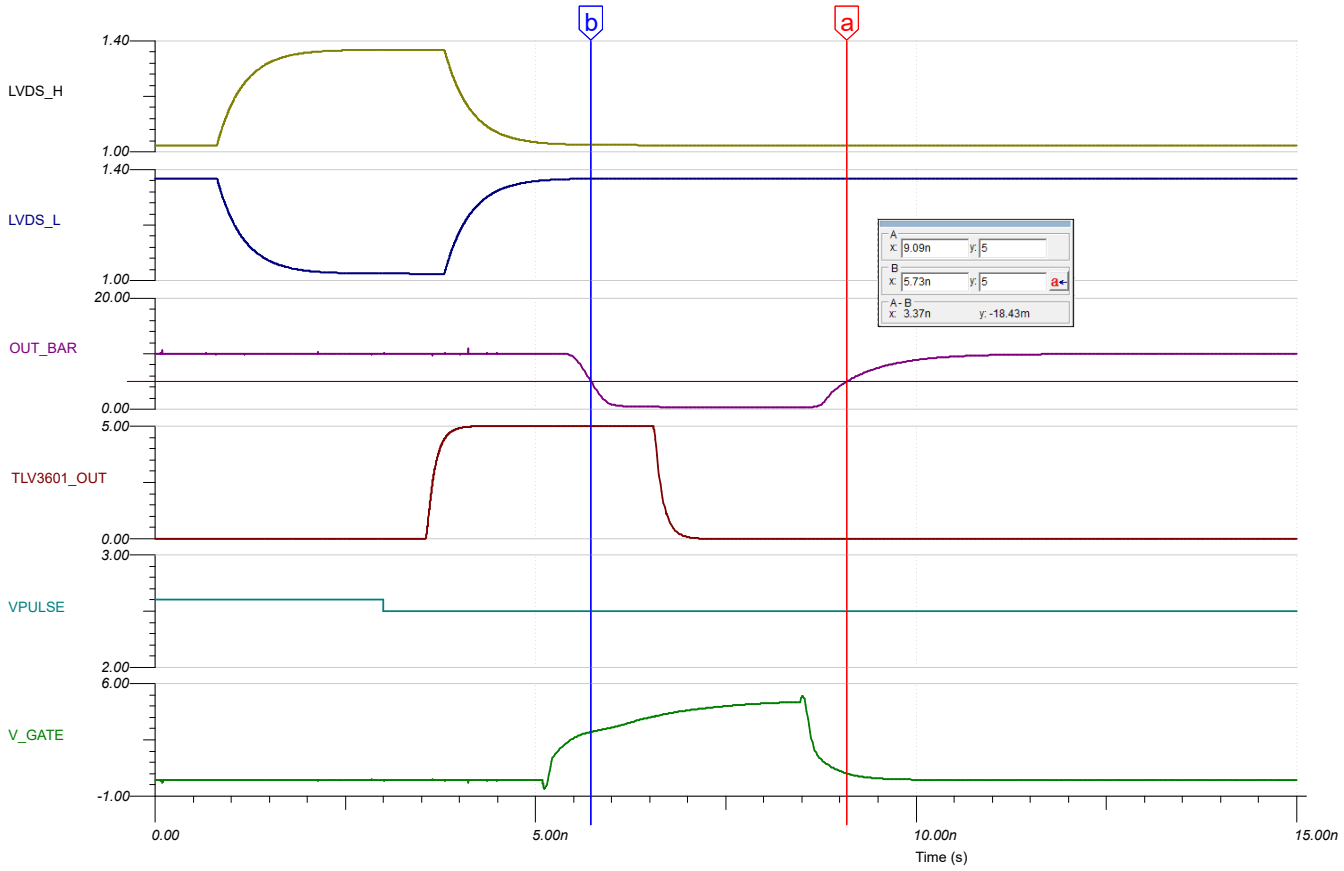
Next, the circuit is simulated again to see if the pulse width has been reduced to meet the design requirements.



Simulation Results After Removing Resistor

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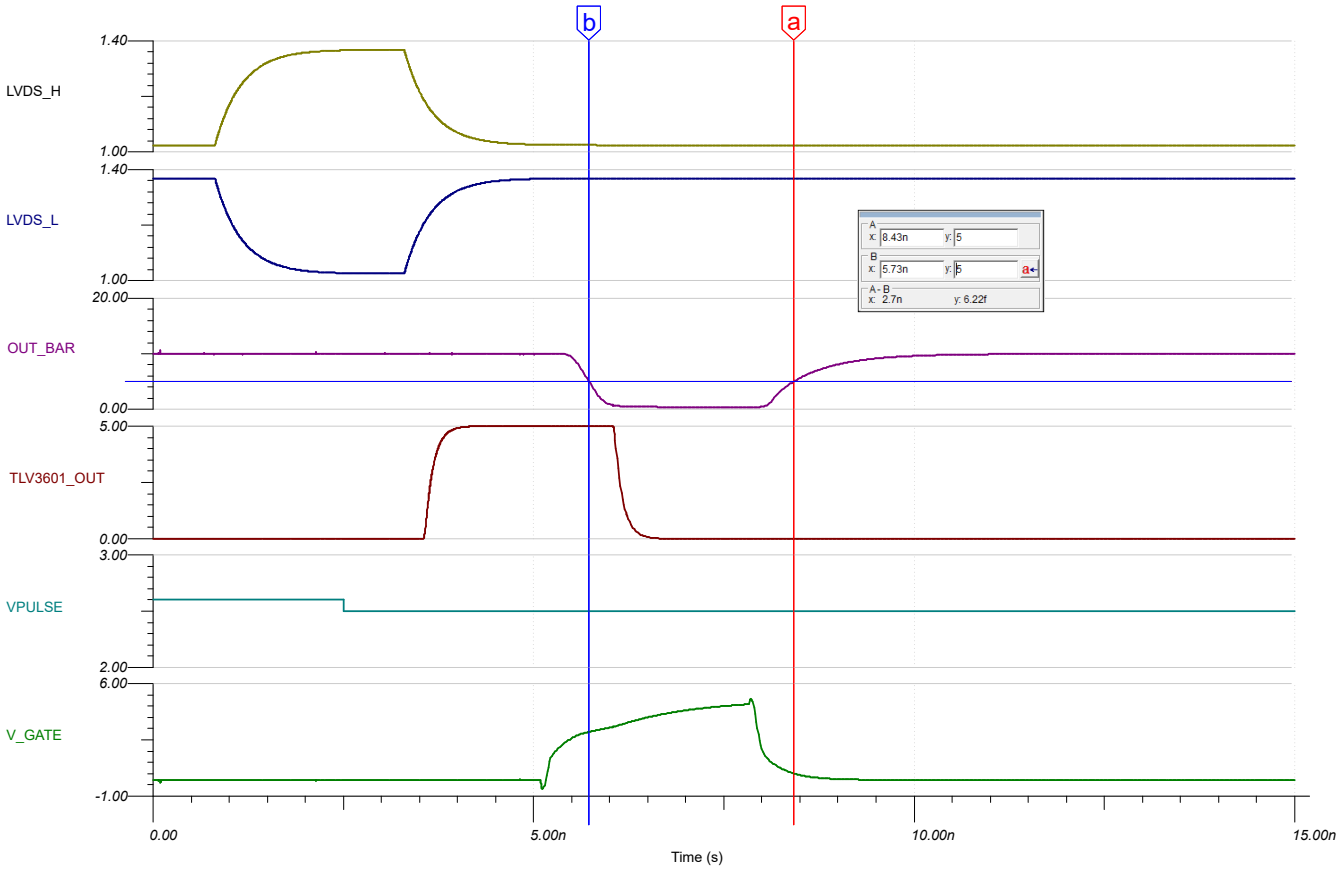
As illustrated by the simulation results in Simulation Results after Removing Resistor, the width of OUT_BAR is slightly out of the design requirement with a pulse width of 3.37 ns. To further improve the pulse width, a narrower LVDS pulse is sent to the TLV3601. To do this, the pulse width of the generator driving the non-inverting input of the TLV3604, VPULSE is reduced. The generator pulse width is adjusted to 2.5 ns to ensure the pulse width is within the design requirement. Design Compliant Simulation illustrates a simulated pulse width of 2.70 ns that complies with the design requirement.



Design Compliant Simulation

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Design References

See the Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See the following documents from Texas Instruments:

- *When to Use High-Speed Comparators or ADCs for Distance Measurements in Optical Time-of-Flight Systems* application report
- *TLV3601, TLV3603 325 MHz High-Speed Comparator with 2.5 ns Propagation Delay* data sheet
- *LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-ns Pulse Width Applications* data sheet

Circuit SPICE Simulation File: SNOM733

For more information on many comparator topics including hysteresis, propagation delay, and input common-mode range, see the TI Precision Labs training.

Design Featured Comparator

TLV3601	
V_S	2.4 V–5.5 V
V_{inCM}	–0.2 V to 5.7 V
V_{os} (offset voltage at 25°C) (Max) (mV)	5
I_q	6 mA per channel
T_{PD} (ns)	2.5
Output type	Push-pull
#Channels	1
TLV3601	

Design Alternate Comparator

	TLV3603	TLV3501
V_S	2.4V–5.5V	2.7 V–5.5 V
V_{inCM}	–0.2V to 5.7V	–0.2 V to 5.7 V
V_{os} (offset voltage at 25°C) (Max) (mV)	5	6.5
I_q	6 mA per channel	3.2
T_{PD} (ns)	2.5	4.5
Output type	Push-pull	Push-pull
#Channels	1	1
Features	Configurable Hysteresis	Shutdown
Product Folder	TLV3603	TLV3501

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