Application Brief

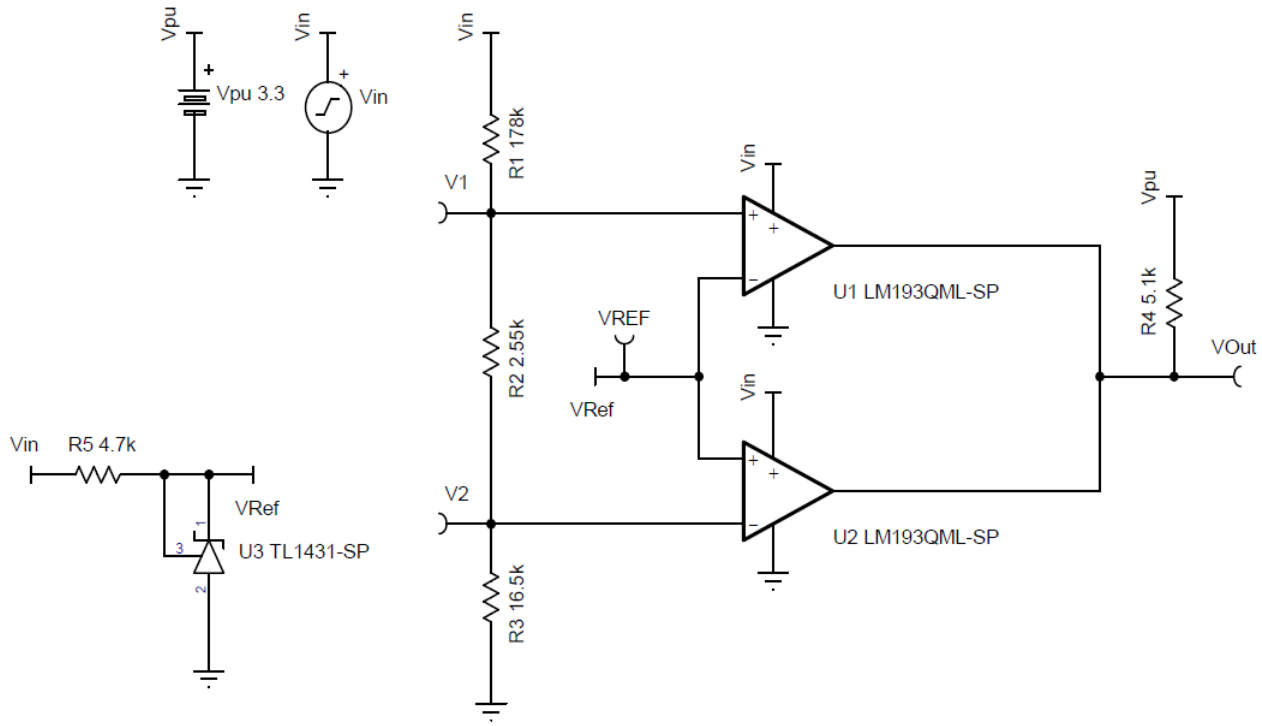
Space-Grade, 100-krad, Window Comparator Circuit

Design Goals

Input Supply	Comparator Output Status (OUT)		Radiation	
Operating Range	$26V \le V_{in} \le 30V$	$V_{in} < 26V$ or $V_{in} > 30V$	Total Ionizing Dose (TID)	SEL Immunity to LET
20 V to 36 V	$V_{out} = V_{pu}$	V_{out} = GND	100 krad(Si)	85 MeV·cm^2/mg

Design Description

This application brief shows how to implement a voltage window comparator circuit, targeted to monitor a 28-V power rail, a spacecraft bus voltage commonly found in smaller aircraft. This wide single-supply window comparator circuit utilizes a dual open-collector comparator and 3 resistors to set the window voltage. A shunt regulator, TL1431-SP, is used to provide a reference voltage from the input voltage. Therefore, only a single power supply is utilized for the input portion of the circuit. The LM193AQML-SP was used for its open collector output, radiation specifications, and two channel count. Whenever the input voltage, V_{in}, is within the window of comparison (26 V to 30 V), the output of the circuit, V_{OUT}, is high. Whenever Vin is outside of the window of comparison, the V_{OUT} is pulled down to GND.



Design Notes

1. Select a high-voltage comparator with an open collector output stage.
2. Select a comparator with low input offset voltage to optimize accuracy.
3. Calculate values for the resistor divider so that V_{OUT} goes high whenever V_1 crosses V_{REF} and goes low whenever V_2 crosses V_{REF}.
4. Calculate R5 such that shunt regulator is within sink current specification for entire operating range.

Design Steps

1. Select a high-voltage comparator with an open collector output stage that can operate at the highest possible supply voltage. In this design, the highest input/supply voltage is 36 V.
2. Determine an appropriate reference level, V_{REF}, for the window comparator. The TL1431-SP internal reference voltage, 2.5 V, was used for ease of calculations. If another reference voltage were to be used with the TL1431-SP, a voltage divider would be needed between the cathode and anode of the shunt regulator, with V_{REF} between the resistors.
3. Calculate the value of R_5, the resistor across V_{IN} and V_{REF}, by relating V_{REF} to the operating voltage range. Ensure that R_5 is at a level where the shunt regulator is sufficiently biased for the entire operating range. The current needed to bias the TL1431-SP, I_{Bias}, has to be between 1 mA and 100 mA. A 4.7-kΩ resistor was chosen as it kept the bias current within this range for the entire voltage operating range.

$$I_{Bias\ (Min)} = \frac{V_{in\ (Min)} - V_{Ref}}{R_5} = \frac{20\ V - 2.5\ V}{4.7\ k\Omega} = 3.72\ mA$$

$$I_{Bias\ (Max)} = \frac{V_{in\ (Max)} - V_{Ref}}{R_5} = \frac{36\ V - 2.5\ V}{4.7\ k\Omega} = 7.12\ mA$$

   Values between 350 Ω and 16 kΩ could be used in this design. Consideration was made to minimize the bias current, yet give some buffer from the 1 mA minimum specification. If V_{REF} is seen to be noisy, a decoupling capacitor can be placed between the node and GND to filter out the noise.
4. The positive input to the top comparator, V_1, and the negative input to the bottom comparator, V_2, can be related to V_{in} through voltage division:

$$V_1 = V_{in}\left(\frac{R_2 + R_3}{R_1 + R_2 + R_3}\right), \quad V_2 = V_{in}\left(\frac{R_3}{R_1 + R_2 + R_3}\right)$$

   The window comparator trips when V_1 passes V_{REF} to output high, and again when V_2 passes V_{REF} to output low. The comparator is low if V_1 is less than V_{REF}. In this design, the window comparator will trip high when V_{in} equals 26 V and trip low when V_{in} equals 30 V; both while V_{REF} equals 2.5 V.

$$2.5 = 26\left(\frac{R_2 + R_3}{R_1 + R_2 + R_3}\right) \rightarrow 10.4 = \frac{R_1 + R_2 + R_3}{R_2 + R_3}$$

$$2.5 = 30\left(\frac{R_3}{R_1 + R_2 + R_3}\right) \rightarrow 12 = \frac{R_1 + R_2 + R_3}{R_3}$$

5. Solve both equations from step 4 for $(R_1+R_2+R_3)$ and substitute one equation for the other.

$$10.4\ R_2 + 10.4\ R_3 = R_1 + R_2 + R_3$$

$$12\ R_3 = R_1 + R_2 + R_3$$

$$12\ R_3 = 10.4\ R_2 + 10.4\ R_3$$

$$10.4\ R_2 = 1.6\ R_3 \rightarrow 6.5\ R_2 = R_3$$

6. Using the relationship obtained in step 5, solve for a relationship between R_1 and R_2.

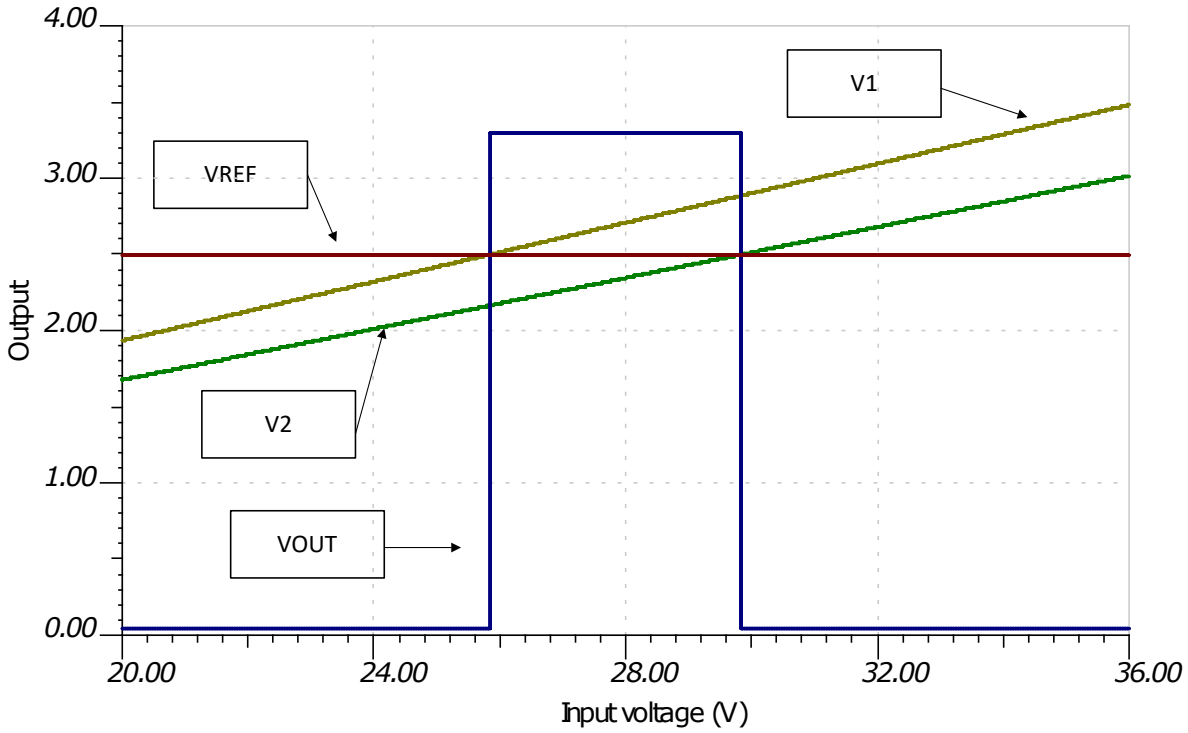
$$12\ (6.5\ R_2) = R_1 + R_2 + 6.5\ R_2$$

$$78\ R_2 = R_1 + 7.5\ R_2 \rightarrow 70.5\ R_2 = R_1$$

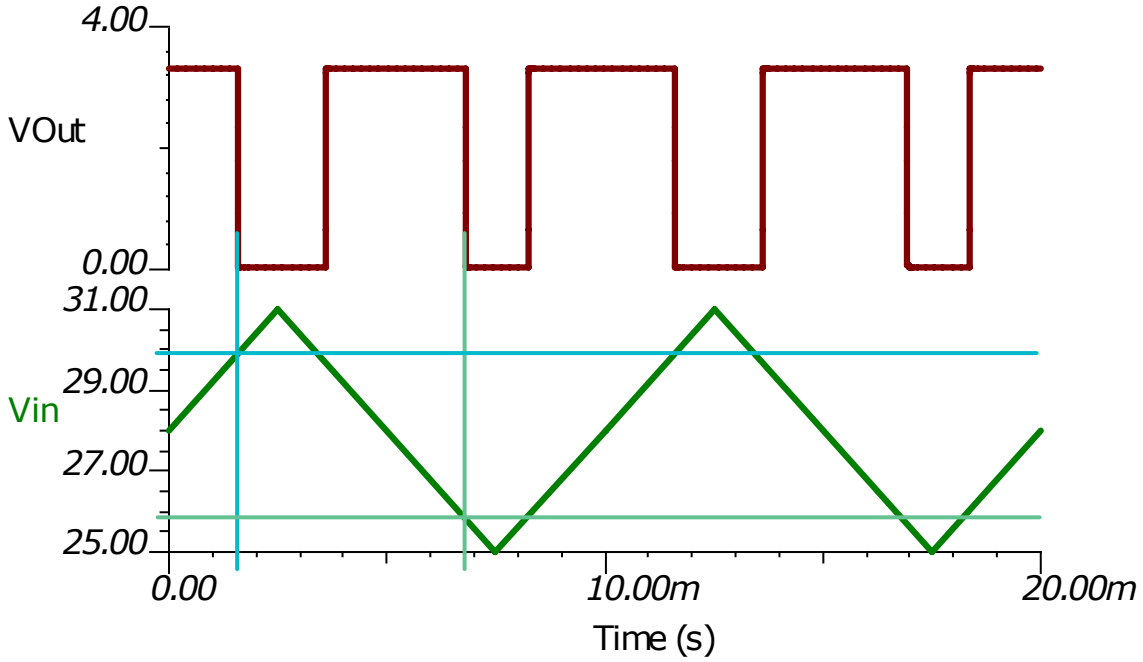
7. Using the equations derived in steps 5 and 6, size resistors R_1, R_2, and R_3 accordingly. For this design, R_2 was set to be 2.55 kΩ, which meant R_1 and R_3 would be 179.775 kΩ and 16.575 kΩ, respectively. The magnitude of these resistors were chosen based off of the current consumption across the voltage divider (around 100 to 180 µA across the operating condition).
8. Select a 5% tolerant resistor to act as the pullup resistor, R_4, from the output of the window comparator to V_{PU}. Size this component large enough to ensure the current sinked by the comparator is not large, but small enough that the leakage current drawn by the comparator output when high is not causing too large of a voltage drop.
9. The values obtained in step 7 were adjusted for 1% resistor tolerances to be 178 kΩ, 2.55 kΩ, and 16.5 kΩ for R_1, R_2, and R_3, respectively. Due to these changes, the window of comparison was shifted to trip earlier for overvoltage conditions and later for undervoltage conditions. In the *DC Simulation Results*, the window of comparison is between 25.8595 V and 29.856 V.

Design Simulations

DC Simulation Results



Transient Simulation Results



References:

1. SPICE Simulation File: http://www.ti.com/lit/zip/snom708.

Design Featured Comparator

LM193QML-SP	
V_S	2 V to 36 V
V_{inCM}	0 V to 34.5 V
V_{OUT}	Open-Collector
V_{OS}	5 mV
I_Q	200 µA/channel
$t_{PD(HL)}$	2.50 µs
TID Radiation Lot Acceptance Test (RLAT) / RHA	100 krad(Si)
TID Characterization (ELDRS-Free)	100 krad(Si)
SEL Immune to LET	SEL Immune (Bipolar process)
http://www.ti.com/product/LM193QML-SP	

Design Featured Shunt Reference

TL1431-SP	
V_{KA}	2.5 V to 36 V
I_{KA}	1 mA to 100 mA
$V_{I(ref)}$	2.5 V
Initial Accuracy	0.4%
TID	100 krad(Si)
SEL Immune to LET	SEL Immune (Bipolar process)
www.ti.com/product/TL1431-SP	

Design Alternate Comparator

	TLV1704-SEP	LM139AQML-SP
V_S	2.2 V to 36 V	2 V to 36 V
V_{inCM}	Rail-to-rail	0 V to 34 V
V_{OUT}	Open-Collector, Rail-to-rail	Open-Collector
V_{OS}	500 µV	2 mV
I_Q	55 µA/channel	200 µA/channel
$t_{PD(HL)}$	460 ns	2.50 µs
TID Characterization (ELDRS-Free)	30 krad(Si)	100 krad(Si)
TID Radiation Lot Acceptance Test (RLAT) / RHA	20 krad(Si)	100 krad(Si)
SEL Immune to LET	43 MeV·cm^2/mg	SEL Immune (Bipolar process)
	https://www.ti.com/product/TLV1704-SEP	https://www.ti.com/product/LM139AQML-SP

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