Radiation Report

LMP7704-SP SEE Report

ABSTRACT

This study characterizes the various Single-Event Effects (SEE) of heavy-ion irradiation of the LMP7704-SP. This device is a radiation-hardened, quad-channel, low offset voltage, rail-to-rail input and output (RRIO) precision amplifier with a CMOS input stage. During initial characterization, no incidences of Single-Event Latch-up (SEL) were detected up to LET_{EFF} = 85 MeV-cm^2/mg at 125°C. Single-Event Transients (SET) were detected and characterized from LET_{EFF} 2 to 85 MeV-cm^2/mg at 25°C.

Subsequent correlation testing identified a subcircuit that is vulnerable to SET, with the potential to cause device burnout under specific circuit criteria. Activation of the ESD clamping cell by a high-energy particle can lead to significant inrush current through the supply pins. Depending on the size, composition, physical distance, and parasitic resistance of the decoupling capacitors, this inrush current can be significant enough to cause localized damage, possibly resulting in a permanent high-conductance path from V+ to V–. The vulnerability can be mitigated by using relatively small (1nF-100nF) C0G decoupling capacitors at the pins, and by isolating larger (>100nF) bulk capacitors from the supply pins with series resistance. Effective shielding, including the intact package body of non-decapped units, was also shown to mitigate the vulnerability. See Extended Characterization for detailed discussion of experiments, root cause, and mitigation techniques.

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1 Overview

The LMP7704-SP is a precision amplifier with low input bias, low offset voltage, 2.5MHz gain bandwidth product, and a wide supply voltage. The device is radiation hardened and operates in the military temperature range of −55°C to +125°C.

The high dc precision of this amplifier, specifically the low offset voltage of ±60µV and ultra-low input bias of ±500fA, make this device an excellent choice for interfacing with precision sensors with high-output impedances. This amplifier can be configured for transducer, bridge, strain gauge, and transimpedance amplification.

Table 1-1. Overview Information (1)

DESCRIPTION	DEVICE INFORMATION
TI Part Number	LMP7704-SP
MLS Number	5962-1920601VXC
Device Function	Radiation Hardness Assured (RHA), Precision, Low Input Bias, RRIO, Wide Supply Range Amplifiers
Technology	VIP050
Exposure Facility	Radiation Effects Facility, Cyclotron Institute, Texas A&M University
Heavy Ion Fluence per Run	1×10^6 – 1×10^7 ions/cm^2
Irradiation Temperature	125°C (for SEL testing)

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2 SEE Mechanisms

The primary single-event effect (SEE) events of interest in the LMP7704-SP are single-event latch-up (SEL). From a risk and impact point-of-view, the occurrence of an SEL is potentially the most destructive SEE event and the biggest concern for space applications. The VIP050 process was used for the LMP7704-SP. CMOS circuitry introduces a potential for SEL susceptibility. SEL can occur if excess current injection caused by the passage of an energetic ion is high enough to trigger the formation of a parasitic cross-coupled PNP and NPN bipolar structure (formed between the p-sub and n-well and n+ and p+ contacts). The parasitic bipolar structure initiated by a single-event creates a high-conductance path (inducing a steady-state current that is typically orders-of-magnitude higher than the normal operating current) between power and ground that persists (is *latched*) until power is removed or until the device is destroyed by the high-current state.

The initial characterization study was performed to evaluate the SEL effects with a bias voltage of 5.5V on V_{IN} and supply voltage of 12V (V_S = ±6V). Heavy ions with LET_{EFF} = 85MeV-cm^2/mg were used to irradiate the devices. Flux of 10^5 ions/s-cm^2 and fluence of 10^7 ions/cm^2 were used during the exposure at 125°C. The VIP050 process modifications applied for SEL mitigation were shown to be sufficient because the LMP7704-SP exhibited no SEL with heavy-ions up to an LET_{EFF} of 85MeV-cm^2/mg at a fluence of 10^7 ions/cm^2 and a chip temperature of 125°C.

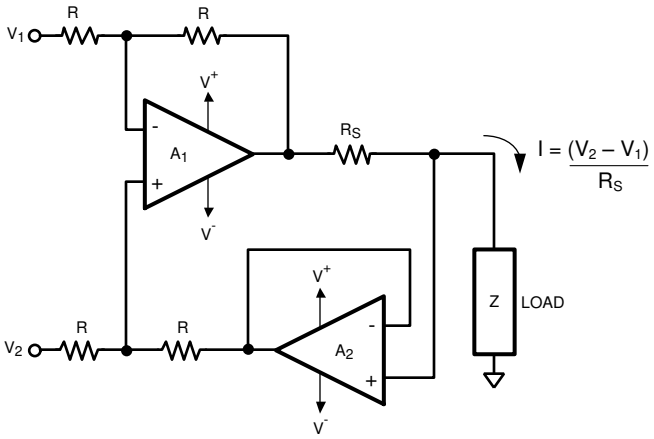

Figure 2-1. Typical LMP7704-SP Application Diagram

Subsequent analysis and retesting of the device identified a vulnerability in the device architecture, with one subcircuit having the potential to cause device burnout under specific circuit criteria. Though the activation of this vulnerability does not give rise to a parasitic bipolar structure, an unintended high-conductance path between V+ and V– still results. If enough current flows along this path, the resulting electrical overstress and associated localized heating can destroy the device. Because the structure can only be activated by a high-energy particle, the scenario is classified as a SEL. See Section 7 for detailed discussion of this vulnerability, including root cause.

3 Test Device and Test Board Information

The LMP7704-SP is packaged in an 14-pin, HBH CFP shown with pinout in Figure 3-1. Figure 3-2 shows the LMP7704-SP bias diagram.

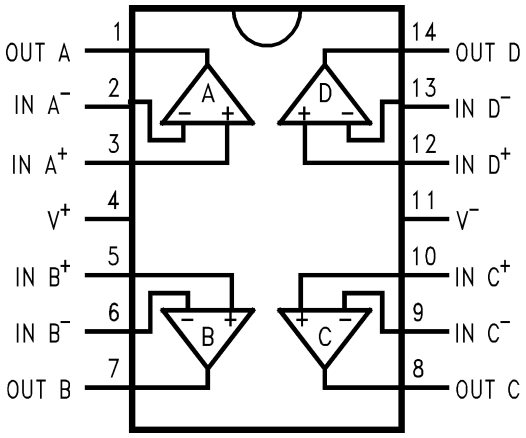

Figure 3-1. LMP7704-SP Pinout

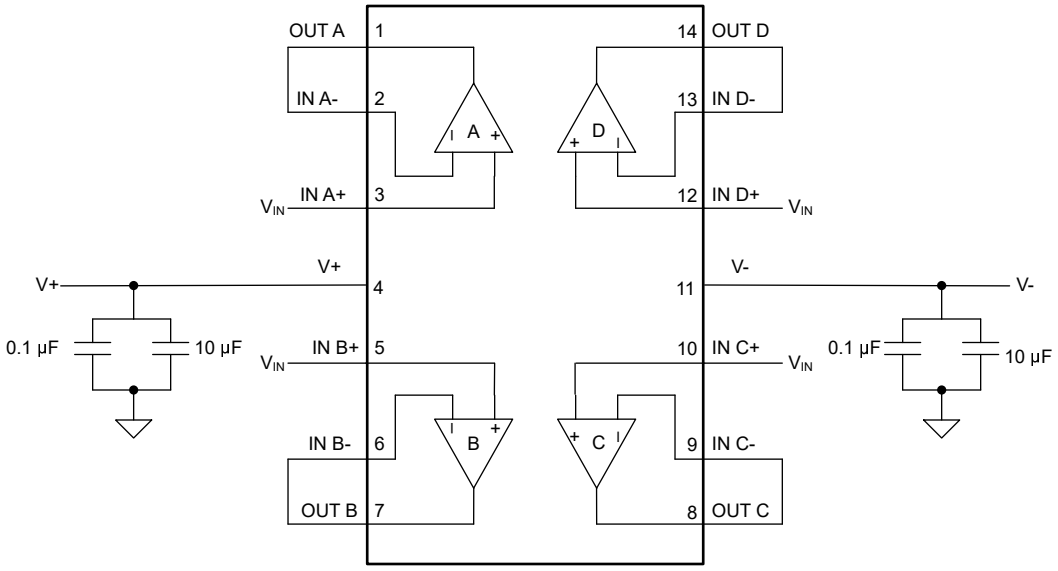

Figure 3-2. LMP7704-SP Bias Diagram

4 Irradiation Facility and Setup

The heavy ion species used for the original SEE studies on this product were provided and delivered by the TAMU Cyclotron Radiation Effects Facility [3] using a superconducting cyclotron and advanced electron cyclotron resonance (ECR) ion source. Ion beams are delivered with high uniformity over a 1-inch diameter circular cross sectional area for the in-air station. Uniformity is achieved by means of magnetic defocusing. The intensity of the beam is regulated over a broad range spanning several orders of magnitude. For the bulk of these studies, ion fluxes between 10^4 and 10^5 ions/s-cm^2 were used to provide heavy ion fluences between 10^6 and 10^7 ions/cm^2. For these experiments Praseodymium (Pr) ions were used. Ion beam uniformity for all tests was in the range of 91% to 98%.

For correlation SEL and SET testing, heavy ion species were provided and delivered by the MSU Facility for Rare Isotope Beams [9] using a linear particle accelerator ion source. Ion beams were delivered with high uniformity over a 17mm × 18mm area for the in-air station. A current-based measurement is performed on the collimating slits, which intercept 90 to 95% of the total beam, and this measurement is cross-calibrated against Faraday cup readings. These measurements are real-time continuous and establish dosimetry and integrated fluence. In-vacuum and in-air scintillating viewers are used for measurement of the beam size and distribution. An ion flux of 10^5 ions / s-cm^2 was used to provide heavy ion fluences to 10^7 ions / cm^2.

5 SEL Results

During SEL characterization, the device was heated using forced hot air, maintaining the IC temperature at 125°C. The temperature was monitored by means of a K-type thermocouple attached as close to the IC as possible. The species used for the SEL testing was a Praseodymium (^{59}Pr) ion with an angle-of-incidence of 39° for an LET_{EFF} = 85MeV-cm^2/mg. The kinetic energy in the vacuum for this ion is 2.114GeV (15-MeV/amu line). A flux of approximately 10^5 ions/s-cm^2 and a fluence of approximately 10^7 ions/cm^2 were used for two runs. The V_S supply voltage is supplied externally onboard at the recommended maximum voltage setting of 12V. Run duration to achieve this fluence was approximately 2 minutes. No SEL events were observed during both runs shown in Table 5-1. Figure 5-1 shows a plot of the current vs time.

Table 5-1. LMP7704-SP SEL Conditions Using ^{59}Pr at an Angle-of-Incidence of 39°

RUN #	DISTANCE (mm)	TEMPERATURE (°C)	ION	ANGLE	FLUX (ions/s-cm^2)	FLUENCE (ions/cm^2)	LET_{EFF} (MeV-cm^2/mg)
10	40	125	Pr	39°	1.00E+05	1.00E+07	85
311	40	125	Pr	39°	1.00E+05	1.00E+07	85

No SEL events were observed, indicating that the LMP7704-SP is SEL-immune at LET_{EFF} = 85MeV-cm^2/mg and T = 125°C. Using the MFTF method described in Appendix A and combining (or summing) the fluences of the two runs at 125°C (2 × 10^7 ions/cm^2), the upper-bound cross-section (using a 95% confidence level) is calculated in Equation 1:

$$\sigma SEL \leq 1.84 \times 10^{-7} \text{ cm}^2 \text{ for } LET_{EFF} = 85 \text{ MeV-cm}^2/\text{mg and T} = 125°C \quad (1)$$

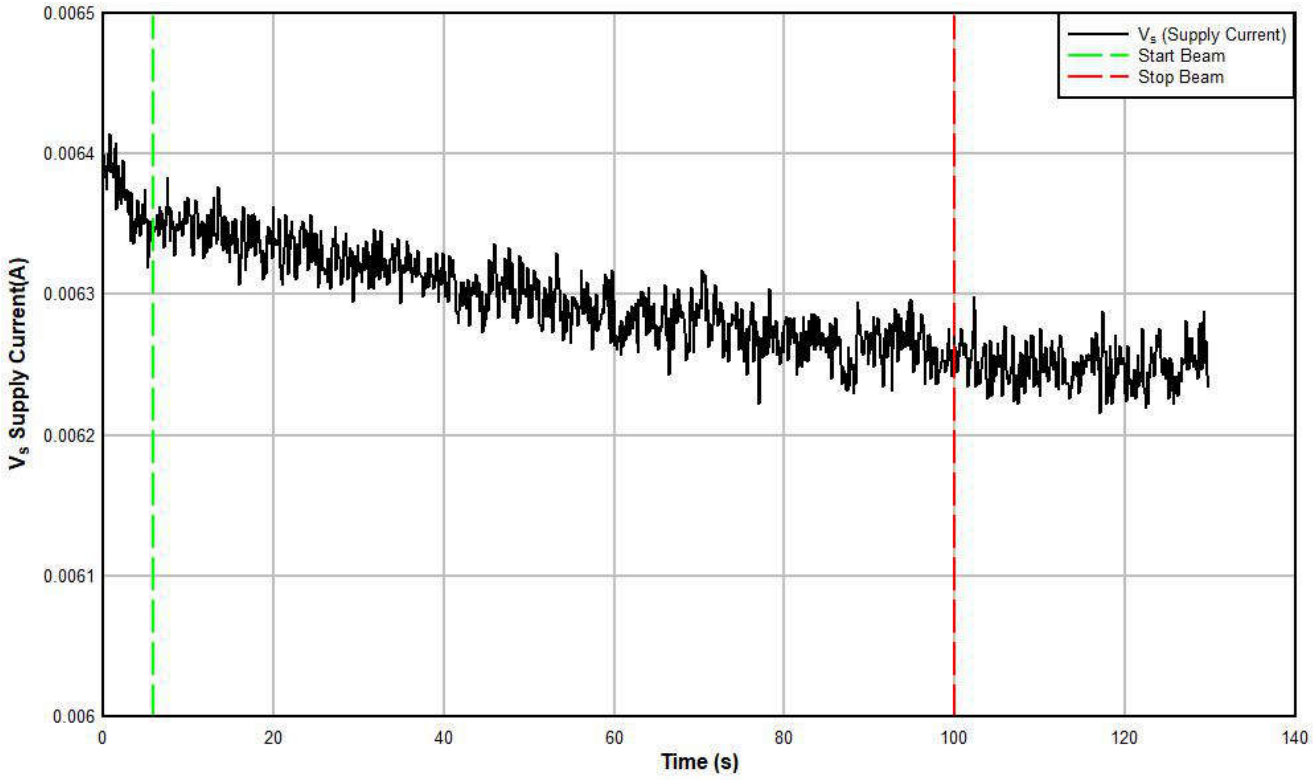

Figure 5-1. Current Versus Time (I vs t) Data for V_S Current During SEL Run # 10

6 SET Results

The LMP7704-SP was characterized for SETs from 2 to 85MeV-cm^2/mg. Table 6-2 lists the ions used for the testing.The device was tested at room temperature in a buffer configuration with the four different setups show in Table 6-1. A flux of 10^4 ions/s-cm^2 was used for all SET runs. The SETs discussed in this report were defined as output voltages that exceeded a window trigger of 5% from the expected output. Both positive and negative upsets were observed during the testing.

Table 6-1. DUT Configurations

Configuration	Gain	Power Supply (±V)	Input (V)	Expected Output (V)	Trigger Window (V)
1	1	1.35	1	1	0.95 to 1.05
2		6	2	2	1.9 to 2.1
3	10	1.35	0.1	1	0.95 to 1.05
4		6	0.2	2	1.9 to 2.1

Table 6-2. Ions and Incident Angles

LET_{EFF} (MeV-cm^2/mg)	Ion	Angle (Degree)
85	Ho	25.5
75	Ho	0
72	Pr	25.5

Table 6-2. Ions and Incident Angles (continued)

LET_{EFF} (MeV-cm²/mg)	Ion	Angle (Degree)
65	Pr	0
54	Ag	25.5
48	Ag	0
23	Cu	25.5
9	Ar	0
2	Ne	0

The number of events observed during the heavy ion runs are presented in Table 6-3 to Table 6-6. All four channels were monitored during the heavy ion runs. LMP7704-SP was tested to fluences ranging from 10^6 to 2 × 10^6 ions/cm².

Table 6-3. SET Results: V_S = ±1.35V, Gain = 1

LET_{EFF} (MeV-cm²/mg)	Fluence (ions/cm²)	Ch1		Ch2		Ch3		Ch4	
		# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)
85	9.96E+05	28	2.81E-05	252	2.53E-04	248	2.49E-04	45	4.52E-05
75	1.00E+06	20	2.00E-05	248	2.48E-04	194	1.94E-04	40	4.00E-05
72	1.01E+06	23	2.29E-05	17	1.69E-05	4	3.98E-06	4	3.98E-06
65	9.70E+05	18	1.86E-05	13	1.34E-05	6	6.19E-06	20	2.06E-05
54	2.00E+06	20	1.00E-05	17	8.52E-06	7	3.51E-06	26	1.30E-05
48	1.99E+06	16	8.04E-06	14	7.04E-06	10	5.03E-06	17	8.54E-06
23	2.00E+06	0	0.00E+00	0	0.00E+00	0	0.00E+00	1	4.99E-07
9	1.99E+06	1	5.03E-07	0	0.00E+00	0	0.00E+00	1	5.03E-07
2	2.00E+06	1	5.00E-07	0	0.00E+00	0	0.00E+00	2	1.00E-06

Table 6-4. SET Results: V_S = ±6V, Gain = 1

LET_{EFF} (MeV-cm²/mg)	Fluence (ions/cm²)	Ch1		Ch2		Ch3		Ch4	
		# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)
85	1.00E+06	14	1.40E-06	67	6.70E-05	41	4.10E-05	28	2.80E-05
75	1.00E+06	16	1.60E-06	53	5.30E-05	59	5.90E-05	11	1.10E-05
72	1.00E+06	14	1.40E-06	15	1.50E-05	10	9.97E-06	13	1.30E-05
65	9.80E+05	13	1.33E-05	11	1.12E-05	20	2.04E-05	12	1.22E-05
54	2.00E+06	21	1.05E-05	17	8.50E-06	16	8.00E-06	18	9.00E-06
48	2.00E+06	21	1.05E-05	24	1.20E-05	10	5.00E-06	18	9.00E-06
23	2.00E+06	2	1.00E-06	0	0.00E+00	0	0.00E+00	6	3.01E-06
9	1.99E+06	0	0.00E+00	0	0.00E+00	0	0.00E+00	0	0.00E+00
2	1.99E+06	0	0.00E+00	0	0.00E+00	0	0.00E+00	0	0.00E+00

Table 6-5. SET Results: V_S = ±1.35V, Gain = 10

LET_{EFF} (MeV-cm²/mg)	Fluence (ions/cm²)	Ch1		Ch2		Ch3		Ch4	
		# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)
85	1.01E+06	253	2.50E-04	214	2.12E-04	187	1.85E-04	288	2.85E-04
75	9.99E+05	175	1.75E-04	200	2.00E-04	145	1.45E-04	211	2.11E-04
72	9.68E+05	153	1.58E-04	154	1.59E-04	113	1.17E-04	209	2.16E-04
65	1.00E+06	101	1.01E-04	95	9.50E-05	72	7.20E-05	163	1.63E-04
54	2.00E+06	74	3.70E-05	81	4.05E-05	45	2.25E-05	124	6.20E-05
48	2.00E+06	61	3.06E-05	53	2.66E-05	32	1.60E-05	100	5.01E-05
23	2.00E+06	8	4.00E-06	15	7.50E-06	1	5.00E-07	21	1.05E-05
9	1.99E+06	0	0.00E+00	0	0.00E+00	0	0.00E+00	2	1.01E-06
2	1.99E+06	0	00.00E+00	0	0.00E+00	0	0.00E+00	0	0.00E+00

Table 6-6. SET Results: V_S = ±6V, Gain = 10

LET_{EFF} (MeV-cm²/mg)	Fluence (ions/cm²)	Ch1		Ch2		Ch3		Ch4	
		# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)	# of Events	Cross Section (cm²)
85	1.03E+06	22	2.14E-05	32	3.11E-05	20	1.94E-05	38	3.69E-05
75	9.97E+05	27	2.71E-05	20	2.01E-05	27	2.71E-05	34	3.41E-05
72	1.20E+06	22	1.83E-05	19	1.58E-05	24	1.99E-05	35	2.91E-05
65	1.00E+06	19	1.90E-05	14	1.40E-05	27	2.70E-05	30	3.00E-05
54	2.00E+06	31	1.55E-05	19	9.51E-06	38	1.90E-05	65	3.25E-05
48	2.00E+06	27	1.35E-05	19	9.50E-06	21	1.05E-05	27	1.35E-05
23	2.00E+06	2	1.00E-06	0	0.00E+00	1	5.00E-07	2	1.00E-06
9	2.00E+06	0	0.00E+00	0	0.00E+00	0	0.00E+00	2	1.00E-06
2	1.99E+06	0	0.00E+00	0	0.00E+00	0	0.00E+00	0	0.00E+00

Figure 6-1 to Figure 6-8 show the worst-case positive and negative transients at 85MeV-cm²/mg for each test configuration. Importantly, no SETs were observed that reached the voltage supply levels.

When testing with V_S = ±1.35V, Gain = 1, the worst-case positive transient occurred on channel 2 and reached a peak value of 1.189V. The event lasted 1.2µs. The worst-case negative transient occurred on channel 1 and reached a peak value of 0.79V. The event lasted 0.39µs.

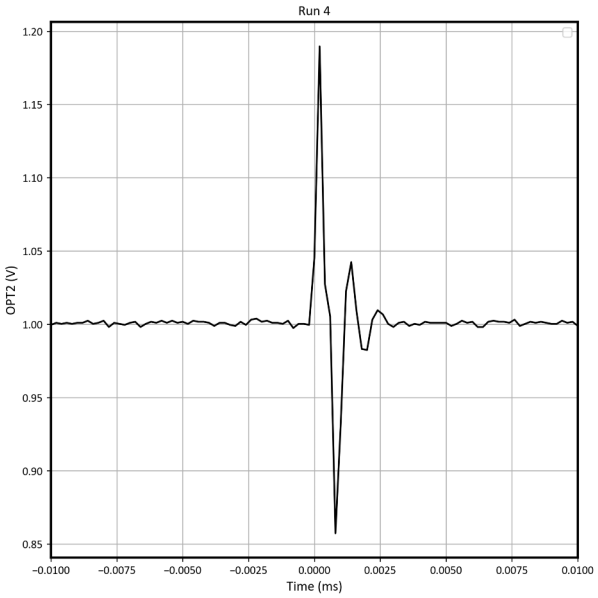

Figure 6-1. Worst-Case Positive Transient on Run #4 With V_S = ±1.35V, Gain = 1

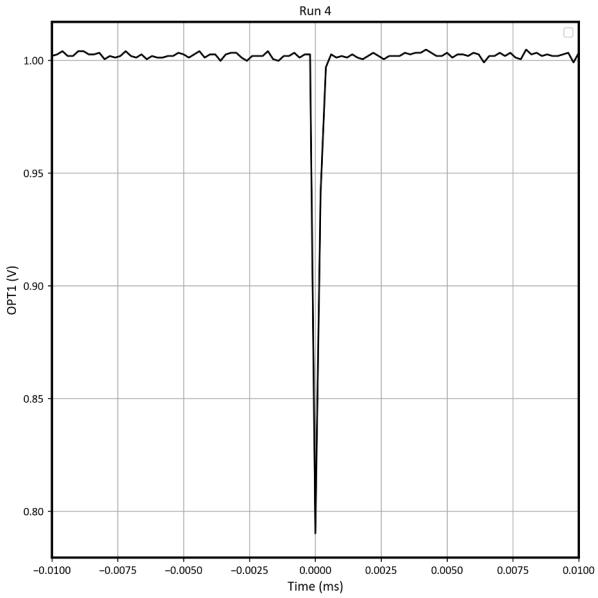

Figure 6-2. Worst-Case Negative Transient on Run #4 With V_S = ±1.35V, Gain = 1

When testing with V_S = ±6V, Gain = 1, the worst-case positive transient occurred on channel 2 and reached a peak value of 2.34V. The event lasted 0.81µs. The worst-case negative transient occurred on channel 4 and reached a peak value of 1.62V. The event lasted 0.39µs.

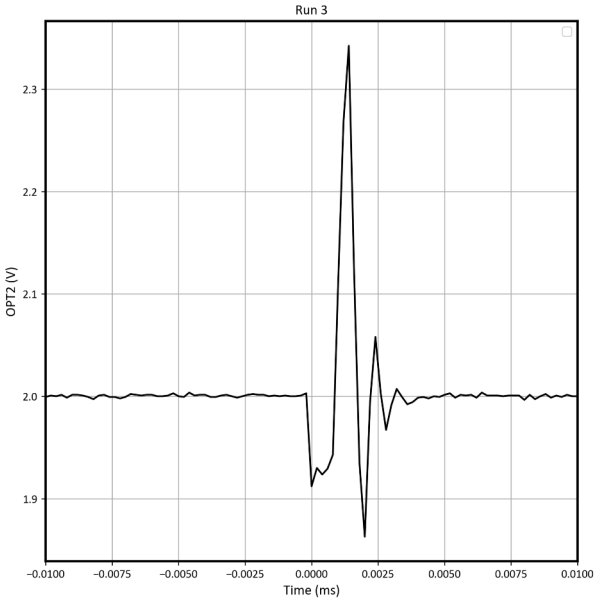

Figure 6-3. Worst-Case Positive Transient on Run #3 With V_S = ±6V, Gain = 1

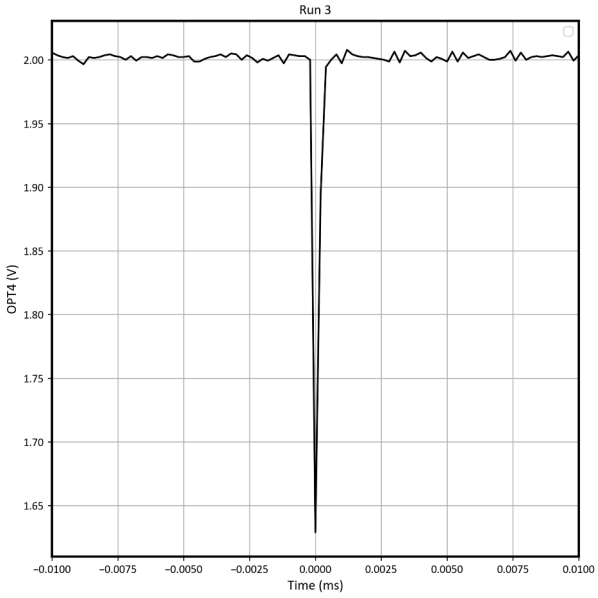

Figure 6-4. Worst-Case Negative Transient on Run #3 With V_S = ±6V, Gain = 1

When testing with V_S = ±1.35V, Gain = 10, the worst-case positive transient occurred on channel 3 and reached a peak value of 1.2V. The event lasted 1.44µs. The worst-case negative transient occurred on channel 4 and reached a peak value of 0.72V. The event lasted 1.43µs.

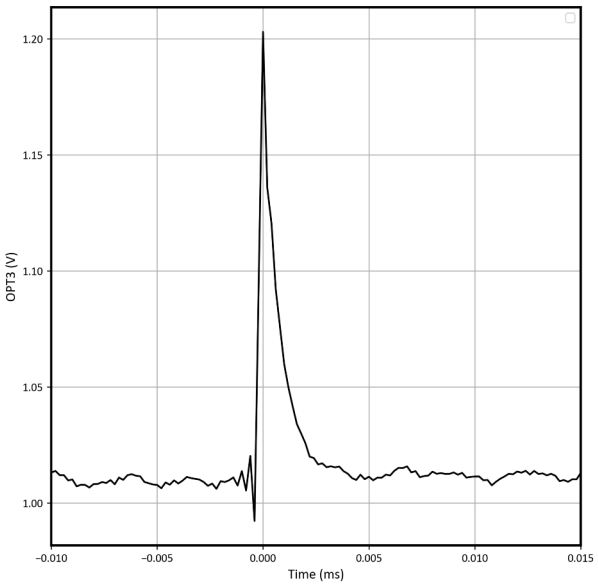

Figure 6-5. Worst-Case Positive Transient on Run #5 With V_S = ±1.35V, Gain = 10

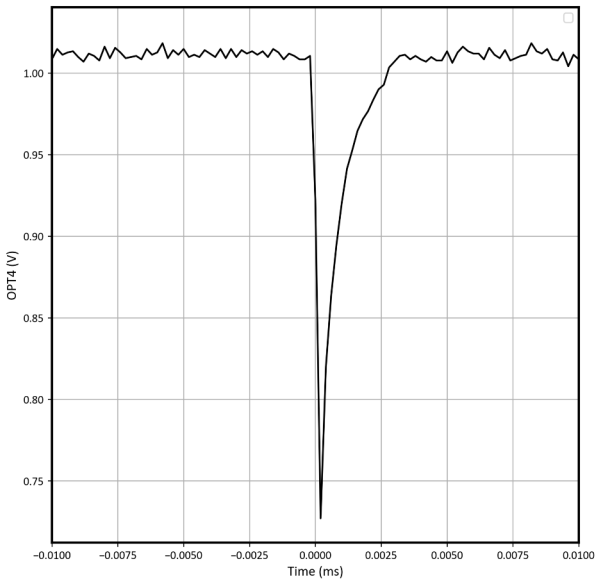

Figure 6-6. Worst-Case Negative Transient on Run #5 With V_S = ±1.35V, Gain = 10

When testing with V_S = ±6V, Gain = 10, the worst-case positive transient occurred on channel 4 and reached a peak value of 2.56V. The event lasted 0.32µs. The worst-case negative transient occurred on channel 1 and reached a peak value of 1.7V. The event lasted 2µs.

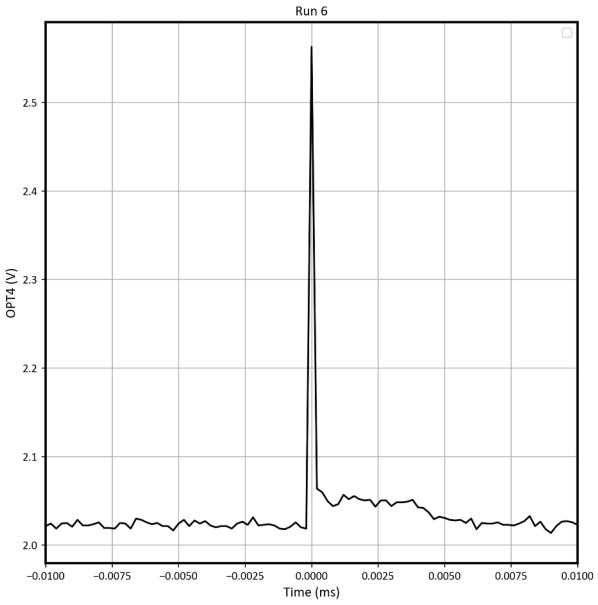

Figure 6-7. Worst-Case Positive Transient on Run #6 With V_S = ±6V, Gain = 10

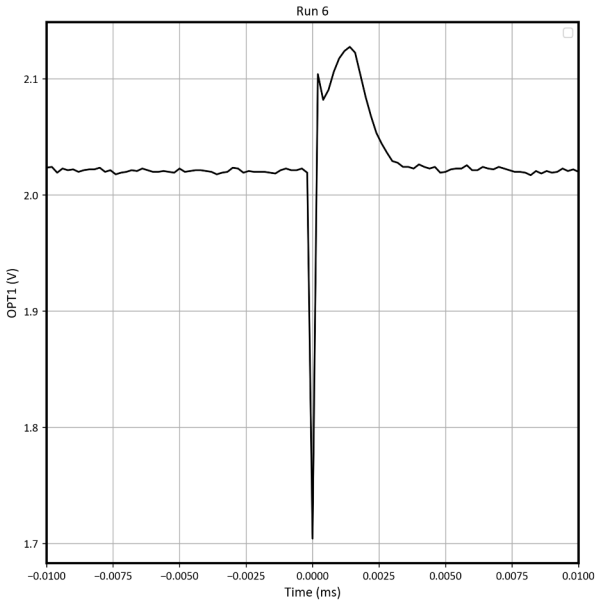

Figure 6-8. Worst-Case Negative Transient on Run #6 With V_S = ±6V, Gain = 10

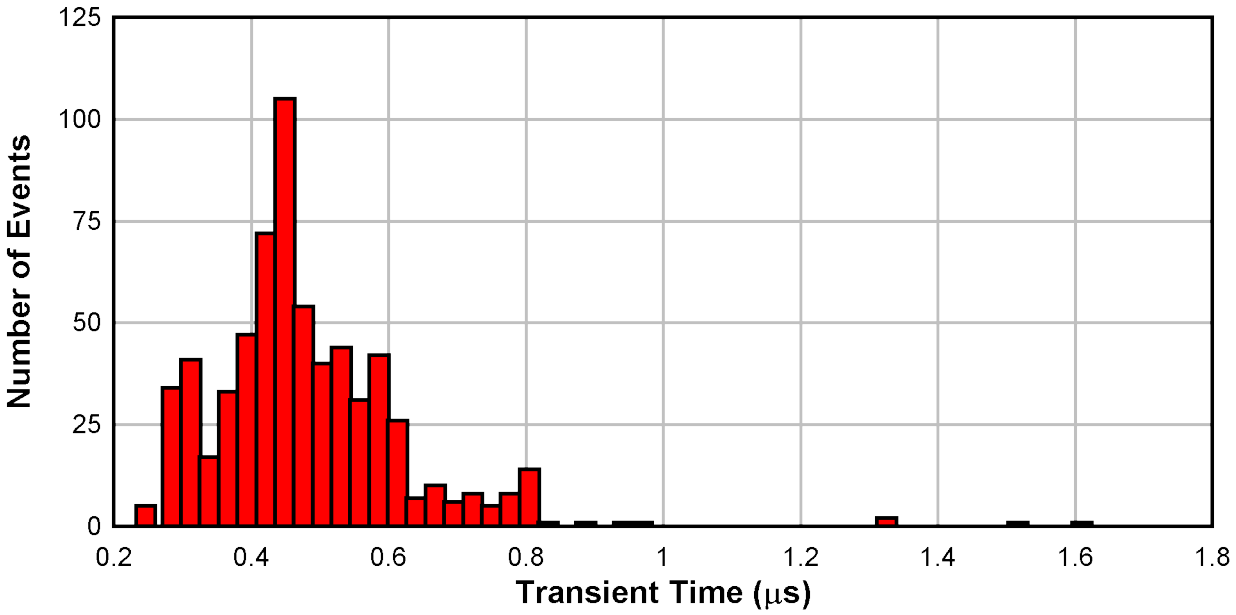

Figure 6-9. Histogram of the Transient Recovery Time for Each Upset at Supply Voltages of ±1.35V and a Gain of 1

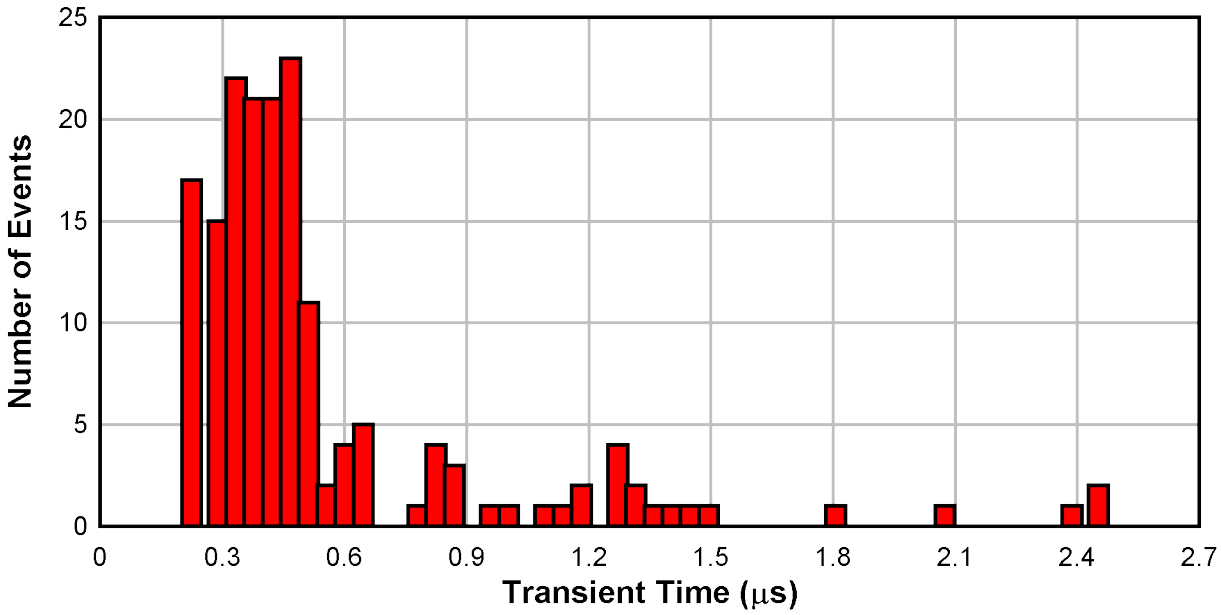

Figure 6-10. Histogram of the Transient Recovery Time for Each Upset at Supply Voltages of ±6V and a Gain of 1

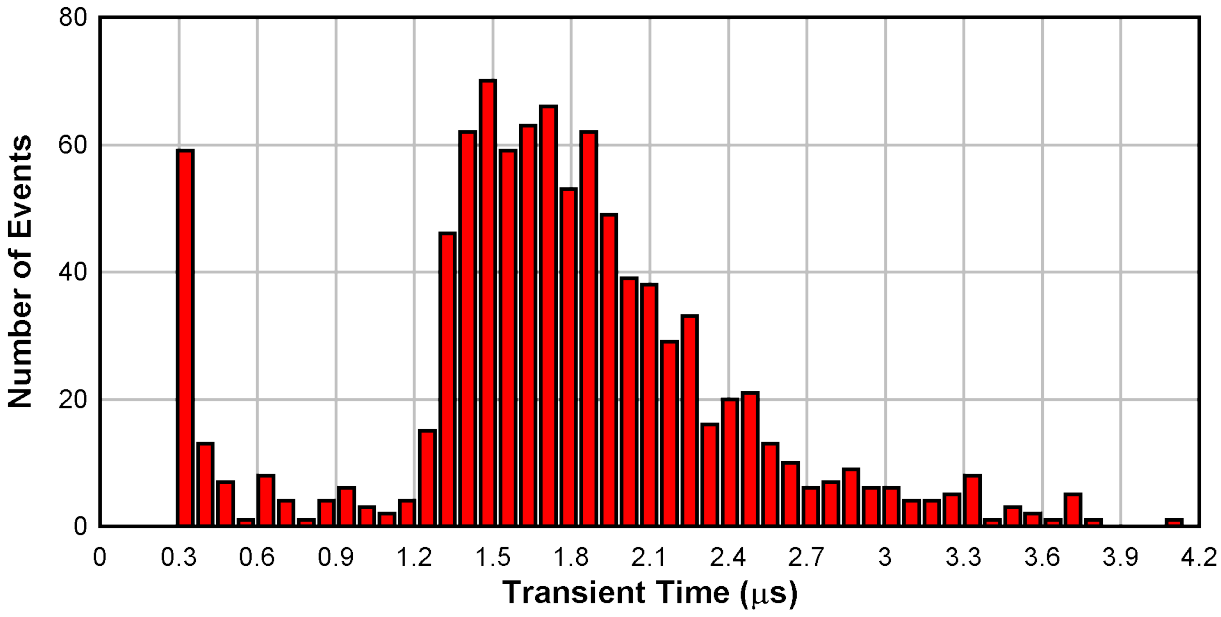

Figure 6-11. Histogram of the Transient Recovery Time for Each Upset at Supply Voltages of ±1.35V and a Gain of 10

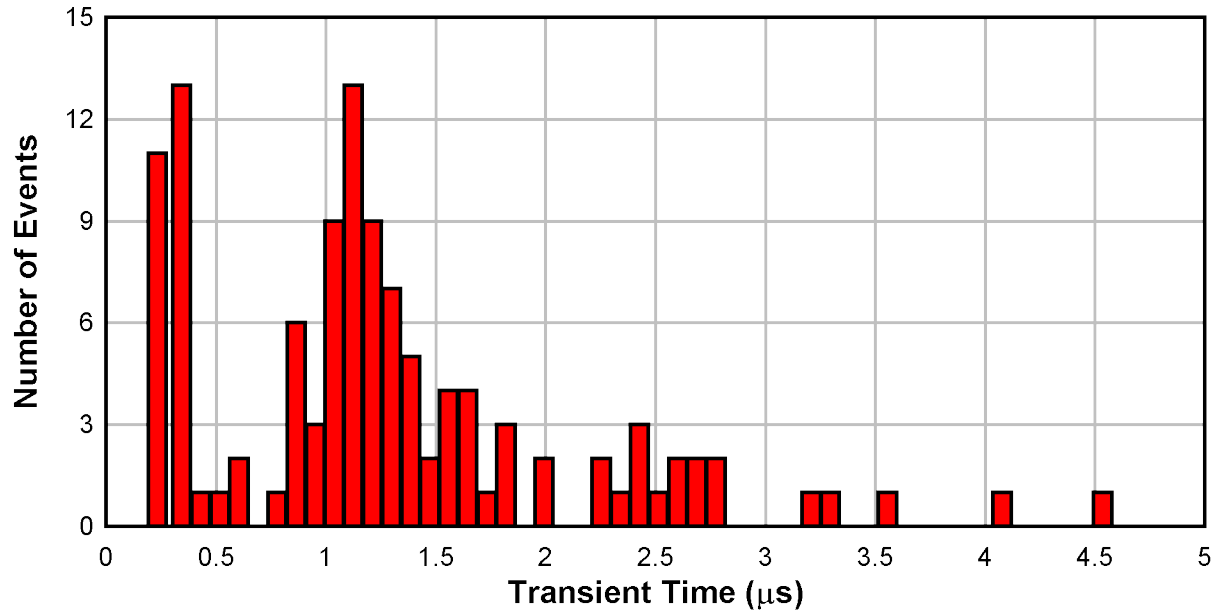

Figure 6-12. Histogram of the Transient Recovery Time for Each Upset at Supply Voltages of ±6V and a Gain of 10

Figure 6-13 through Figure 6-28 show the plots of the SET cross section versus LET for the different operating modes used during SET testing for each channel. At low LETs, a very low number of transient events (≤ 2) occurred, resulting in different onsets from channel to channel. This causes the cross section plots to look different for each channel.

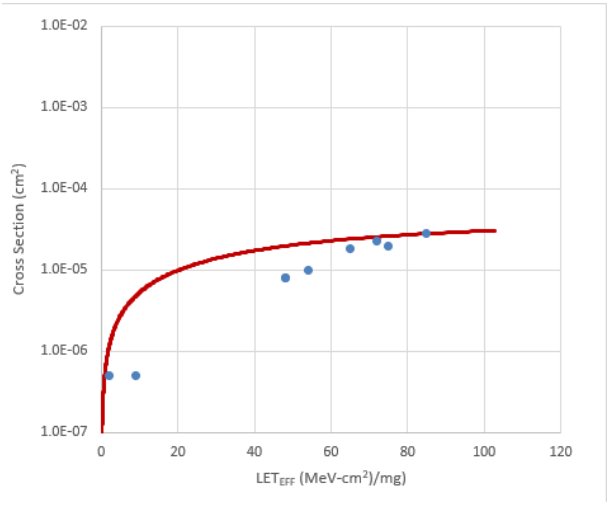

Figure 6-13. Weibull Plot: V_S ±1.35V and Gain = 1 - Channel 1

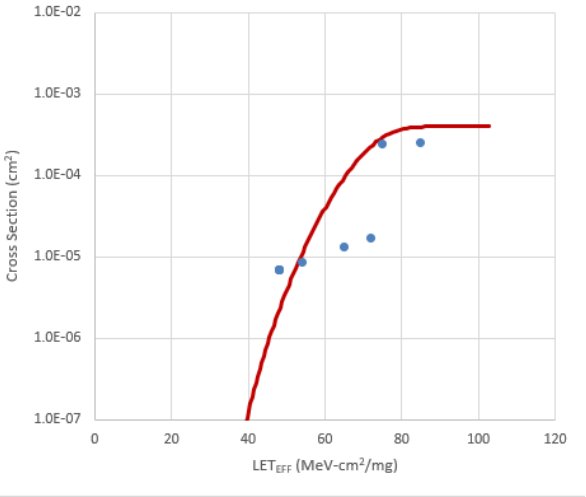

Figure 6-14. Weibull Plot: V_S ±1.35V and Gain = 1 - Channel 2

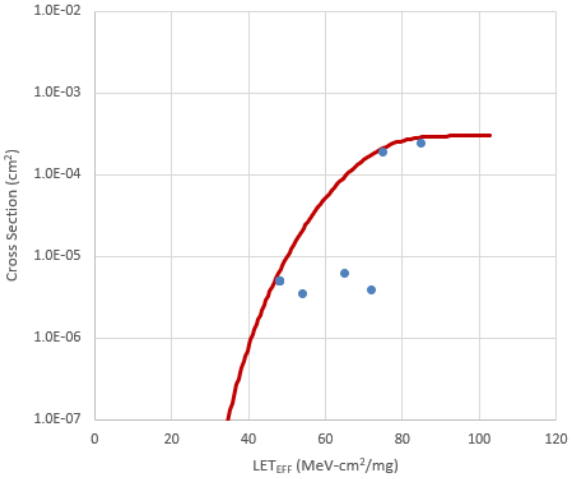

Figure 6-15. Weibull Plot: V_S ±1.35V and Gain = 1 - Channel 3

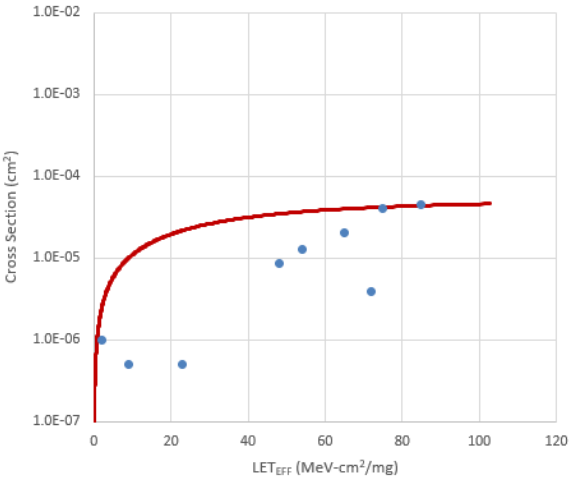

Figure 6-16. Weibull Plot: V_S ±1.35V and Gain = 1 - Channel 4

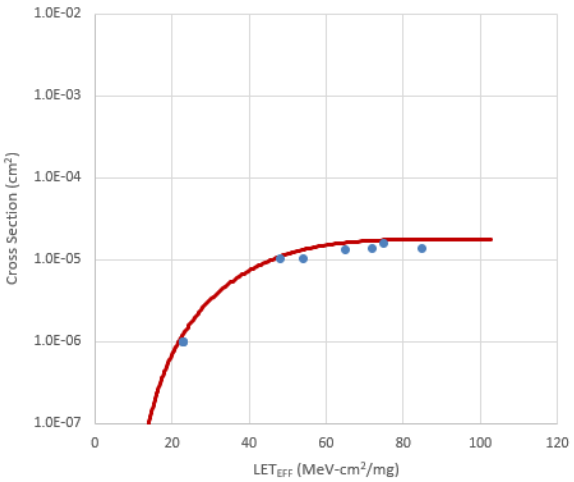

Figure 6-17. Weibull Plot: V_S ±6V and Gain = 1 - Channel 1

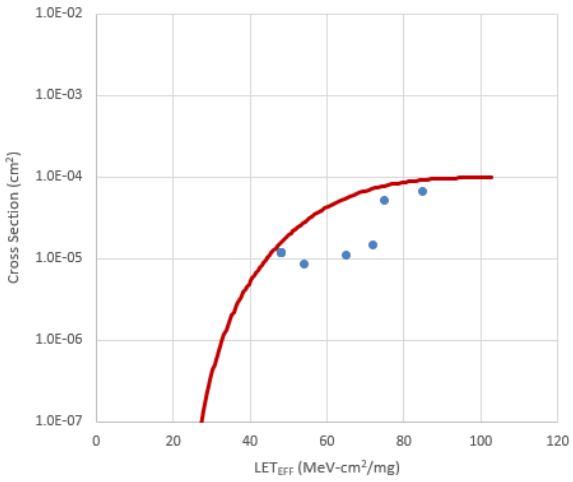

Figure 6-18. Weibull Plot: V_S ±6V and Gain = 1 - Channel 2

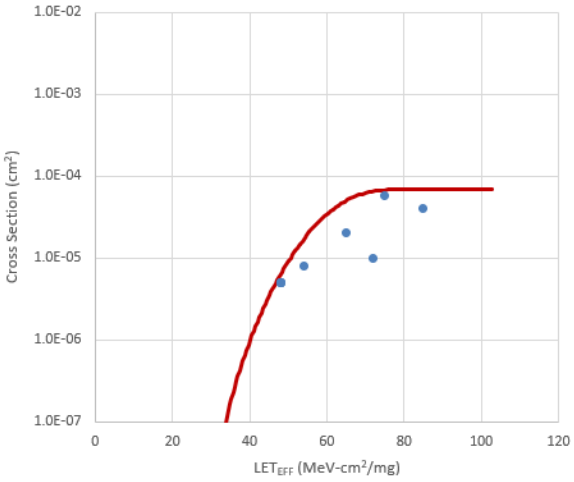

Figure 6-19. Weibull Plot: V_S ±6V and Gain = 1 - Channel 3

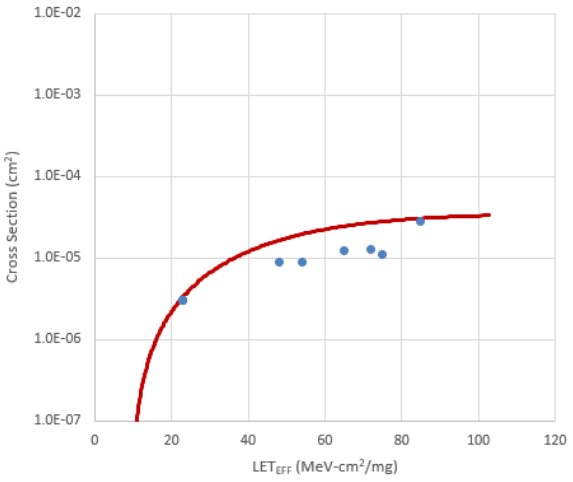

Figure 6-20. Weibull Plot: V_S ±6V and Gain = 1 - Channel 4

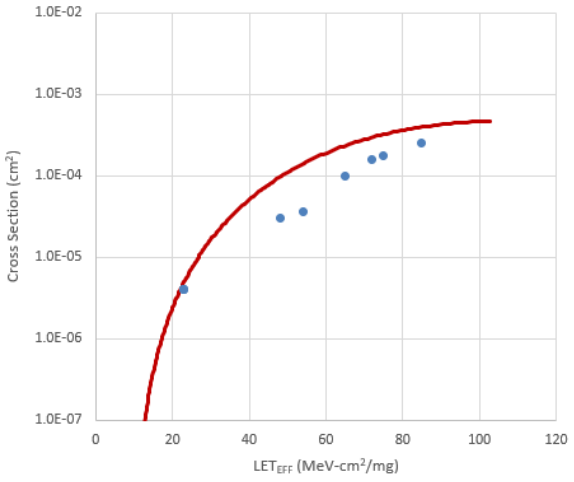

Figure 6-21. Weibull Plot: V_S ±1.35V and Gain = 10 - Channel 1

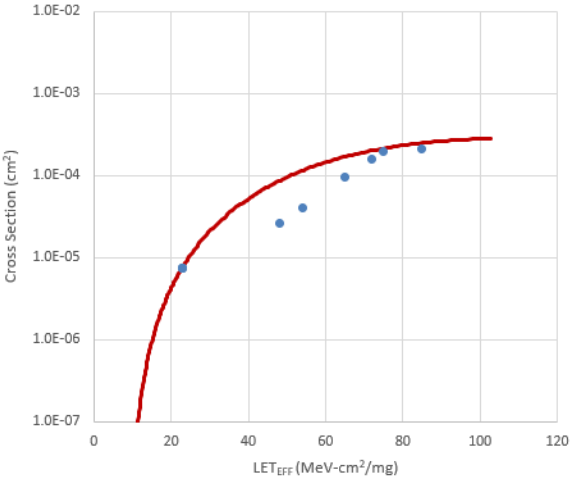

Figure 6-22. Weibull Plot: V_S ±1.35V and Gain = 10 - Channel 2

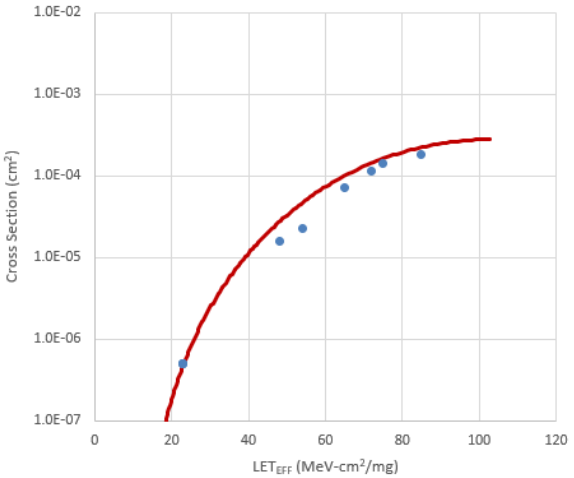

Figure 6-23. Weibull Plot: V_S ±1.35V and Gain = 10 - Channel 3

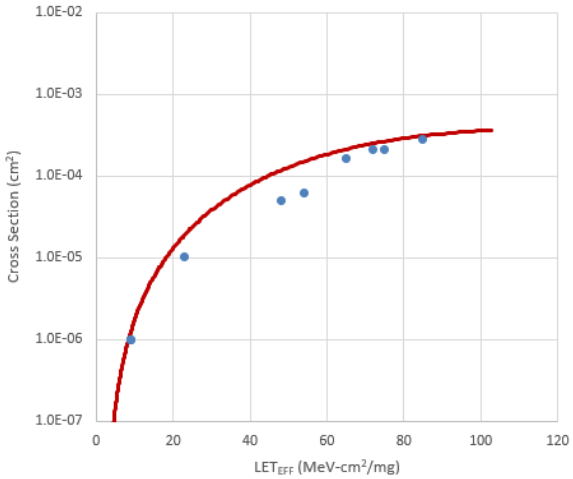

Figure 6-24. Weibull Plot: V_S ±1.35V and Gain = 10 - Channel 4

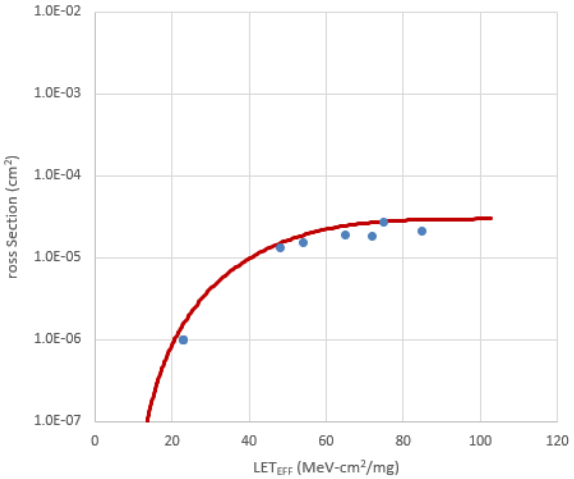

Figure 6-25. Weibull Plot: V_S ±6V and Gain = 10 - Channel 1

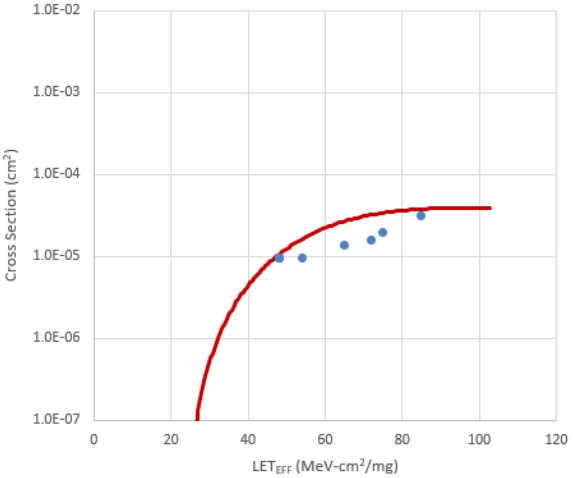

Figure 6-26. Weibull Plot: V_S ±6V and Gain = 10 - Channel 2

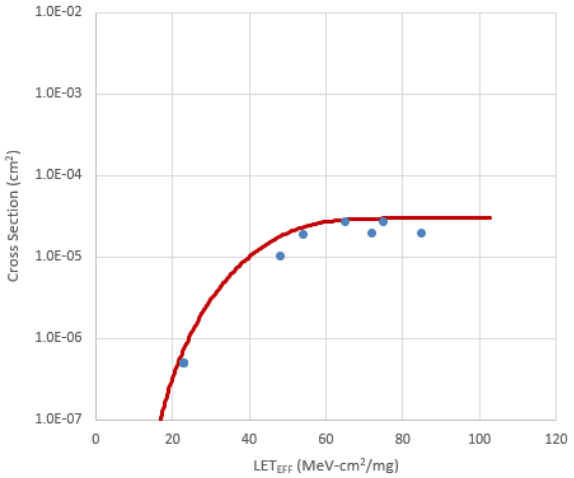

Figure 6-27. Weibull Plot: V_S ±6V and Gain = 10 - Channel 3

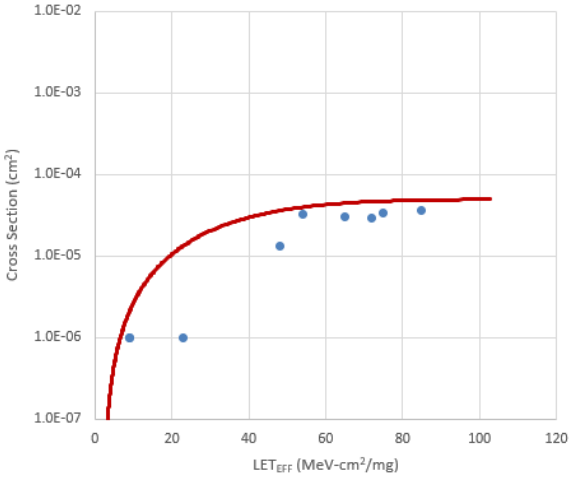

Figure 6-28. Weibull Plot: V_S ±6V and Gain = 10 - Channel 4

7 Extended Characterization

7.1 Correlation Test Results

As part of an initial experiment to correlate the SET performance of the LMP7704-SP between test facilities, a new SEE characterization PCB was designed and populated with LMP7704-SP units. When a device was observed to fail under the beam, a detailed investigation commenced. Preliminary experimentation implied different PCB designs resulted in passing or failing behavior, but further investigation showed differences in decoupling capacitance to be the most significant underlying difference between the boards. When testing a coupon-style design with only 100nF decoupling capacitors localized, and the bulk capacitance isolated by several inches of trace length and several connectors worth of parasitic capacitance, the device was observed to pass repeatedly. Testing on a more conventional EVM-style of PCB, where multiple bulk capacitors were physically adjacent to the 100nF decoupling capacitors, led to device failure.

Oscilloscopes were used to monitor the voltage directly at the supply pins of the devices. These scope captures revealed the rapid initial supply voltage drop and slowly ramping recovery up associated with the ESD clamp activation, eventually leading to identification of the root cause. A sanity check performed on a covered unit (with the lid intact) showed the device packaging provided sufficient shielding to prevent the initial SET, and thus prevent an SEL. This implies the risk to most user applications is extremely low, though the vulnerability is still worth considering as part of standard failure mode and effects analysis. Testing was performed at both TAMU and MSU, and findings were shown to be replicable.

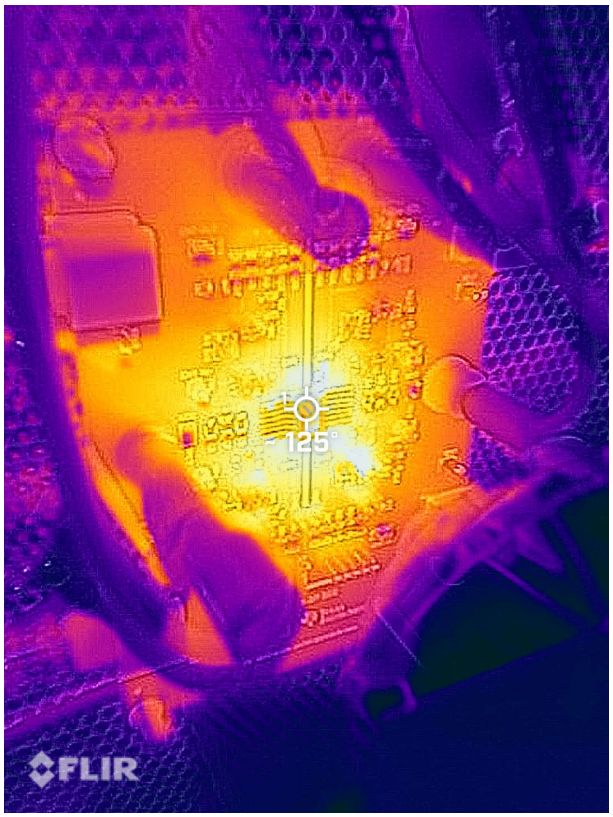

Figure 7-1. Die Temperature Verification with Thermal Camera, MSU

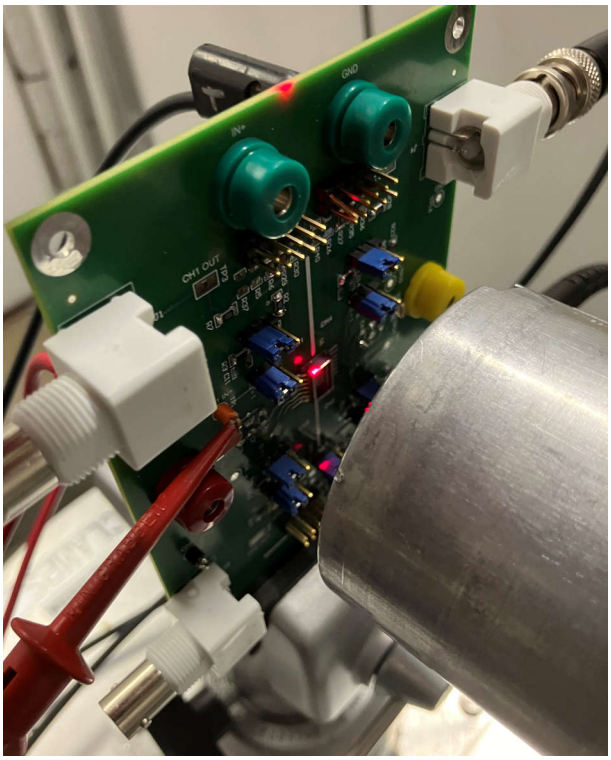

Figure 7-2. Board Alignment for Testing, TAMU

Multiple decoupling capacitor configurations were then explored, to identify a safe operating area for the device. When using only 100nF decoupling capacitors or less, no SEL was observed. Using a 100nF capacitor at the pin and 10µF bulk decoupling capacitor lead to failures in some cases, mostly correlating with higher power supply voltages and closer bulk capacitor placement. Using a 100nF capacitor at the pin and a 1µF bulk capacitor, or a 1µF and 10µF capacitor together, was more strongly correlated with SEL occurrence. The effect of capacitor

composition or material was not experimentally studied due to limited component availability during the test sessions, but is expected to affect the response. Adding a sufficiently large series isolation resistance between the 100nF decoupling capacitor and any subsequent bulk capacitors was observed to prevent SEL.

As an experiment, one prototypical DUT was subjected to the ion stream repeatedly and under multiple test conditions. All decoupling capacitors were removed from the PCB. The supply voltage was slowly stepped from the minimum to the maximum value, both at room temp and at 125°C, to the point that a total exposure of approximately 340krad(Si) was accumulated. 100nF decoupling capacitors were reinstalled at the pins and testing was repeated, again passing to the maximum voltage and reaching an accumulated dose of 410krad(Si). 1µF parallel decoupling capacitors were added and the testing repeated, with a failure observed at 9V supply. By the time of the failure, the part had experienced nearly 500krad(Si) of total ionizing dose.

7.2 Root Cause

The LMP7704-SP employs an ESD clamping structure to protect against ESD damage during storage, transit, and assembly. If the supply pins are floating and a high potential (such as an ESD event) manifests across them, the structure activates and breaks down to provide a low-impedance path between the supplies. Once the potential between the supplies has equalized and the discharge event is over, the structure becomes electrically high-impedance again.

This structure can be unintentionally and momentarily turned on if struck by an energetic particle, such as a heavy ion. The clamp is activated and a low-impedance path between VCC and VEE results. This path effectively establishes a momentary short across any decoupling capacitance at the pins, causing a localized high instantaneous current as the capacitor *charge bucket* is drained. The magnitude of this current follows the form below:

$$I\left(t\right) = C\frac{dV(t)}{dt} \tag{2}$$

An increase in the capacitance (C), supply voltage (V), or both leads to a corresponding increase in peak current (I). Series resistance and inductance between the supply pins and the decoupling capacitor, whether intended or deliberate, reduce the peak current flow. Capacitor ESR also plays a role in the response. For bipolar configurations with split supplies and decoupling capacitors between each supply and ground, the decoupling capacitors manifest in series.

If the peak current is not high enough to damage the device, then the clamp turns off once the voltage across the effective capacitance has drained and reached approximately two diode drops. By this time, the system power supply begins to recharge the decoupling capacitors back to the supply voltage, causing the device power supply to ramp back up. Transients at the device outputs can occur while the power supply is below the recommended minimum value (2.7V) or as the supply ramps back to the original value, especially if the nominal output voltage exceeds the supply voltage.

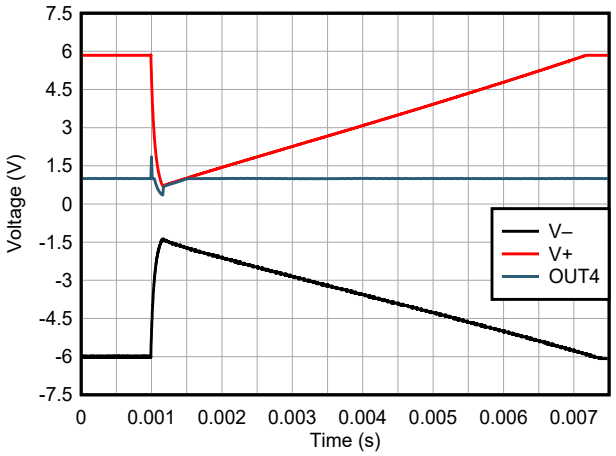

Figure 7-3. Supply and Output Voltages During SET

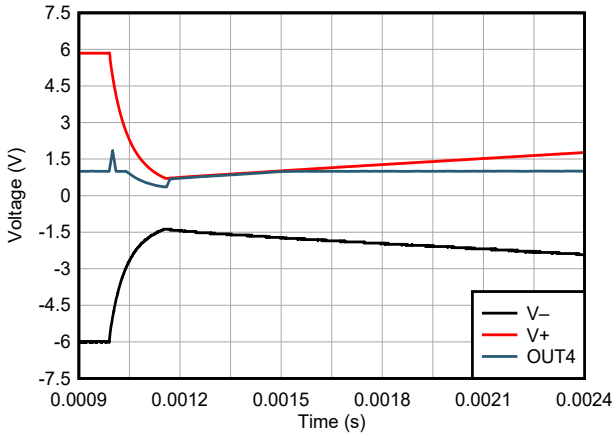

Figure 7-4. Supply and Output Voltages During SET

If the peak current is sufficiently high, localized heating can damage the ESD clamp. This damage in turn can cause the low-impedance path between the supply pins to persist, resulting in electrical and thermal overstress and part failure. Preventative measures include shielding and applications-level fixes, as discussed in subsequent sections.

Any relationship between ion energy and event incidence has not yet been explored in detail. Experiments were mostly performed around 75MeV-cm^2/mg. A test at 18.9MeV-cm^2/mg showed the structure was still able to be activated, though at a far lower rate (upsets per minute) than observed at the higher energy level. Back-to-back events can occur, especially at higher energy levels. Studies focused on bipolar supply conditions with input and output voltages near midsupply; note that some specifics of the response vary depending on circuit architecture.

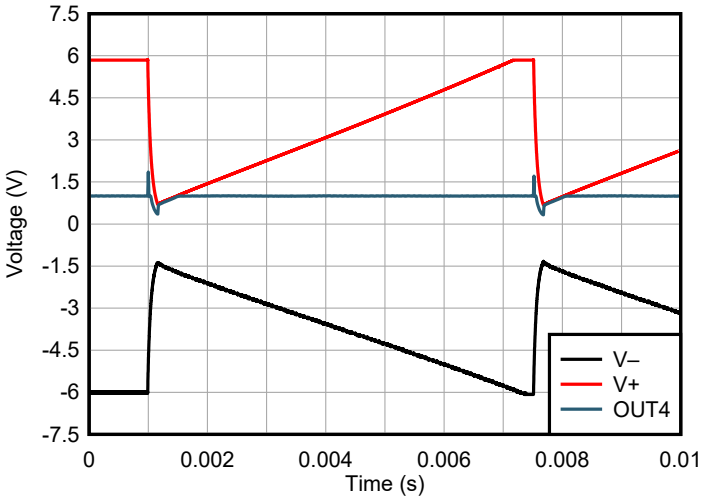

Figure 7-5. Back-to-back SETs

7.3 SEL Prevention

The ceramic body and metal lid of the LMP7704-SP package present a barrier to high-energy ions. For an energetic particle to trigger the ESD clamp cell and potentially cause an SET, the particle must first pass through or bypass the package. External damage such as high heat or mechanical stress can put stress on the package, possibly resulting in a detached lid if the stress were severe enough. Visual and physical inspection of assembled circuits can identify sites of concern and reduce the risk of undetected damage to the package. Additional shielding throughout the body of the satellite or other structure provides additional protection.

Utilize decoupling capacitors of 10nF to 100nF at the supply pins of the device. Avoid using large bulk decoupling capacitors where possible. If a capacitance of over 220nF is present on the supply bus, is near

the device, and is not significantly isolated by series resistance or inductance, consider adding a deliberate isolation resistance. In one experiment using 1206 capacitors placed adjacently, a 2.5Ω isolation resistor did not prevent an SEL, but a 5Ω isolation resistor did.

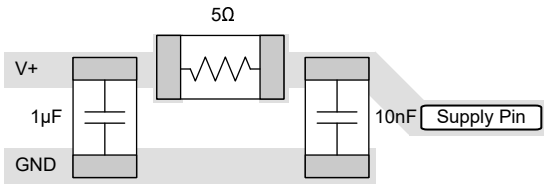

Figure 7-6. Example of Series Resistance Used to Isolate Bulk Decoupling Capacitor

SEL vulnerability increases for supply voltages in excess of 5.2V. Circuits using supply voltages at or below this level were not observed to experience SEL.

8 Summary

The radiation effects of the LMP7704-SP, a radiation-hardened precision amplifier with a rail-to-rail input and output and CMOS input stage, were studied. Initial characterization showed the device passed and is latch-up immune up to LET_{EFF} = 85 MeV-cm^2/mg and T = 125°C. SET was characterized from LET_{EFF} = 2 MeV-cm^2/mg to LET_{EFF} = 85 MeV-cm^2/mg. The worst-case transients and the cross-section plots are included. Testing was performed under multiple configurations and supply voltages.

Subsequent correlation testing showed the device can be vulnerable to SEL under very specific circuit criteria. An exposed die can theoretically occur as a result of external factors, such as preexisting damage. If significant bulk decoupling capacitance is present at the pins, such that a large *charge bucket* is present, an ion strike in the right portion of the die can activate an ESD structure and create a low-impedance path between the supplies. While this event is unlikely for most implementations, preventative and mitigating actions are proposed for risk management and reduction purposes.

A Confidence Interval Calculations

For conventional products where hundreds of failures are seen during a single exposure, one can determine the average failure rate of parts being tested in a heavy-ion beam as a function of fluence with high degree of certainty and reasonably tight standard deviation, and thus have a good deal of confidence that the calculated cross-section is accurate.

With radiation-hardened parts however, determining the cross-section is difficult because often few or no failures are observed during an entire exposure. Determining the cross-section using an average failure rate with standard deviation is no longer a viable option, and the common practice of assuming a single error occurred at the conclusion of a null-result can end up in a greatly underestimated cross-section.

In cases where observed failures are rare or non-existent, the use of confidence intervals and the chi-squared distribution is indicated. The chi-squared distribution is particularly an excellent choice for the determination of a reliability level when the failures occur at a constant rate. In the case of SEE testing where the ion events are random in time and position within the irradiation area, one expects a failure rate that is independent of time (presuming that parametric shifts induced by the total ionizing dose do not affect the failure rate), and thus the use of chi-squared statistical techniques is valid (because events are rare, an exponential or Poisson distribution is usually used).

In a typical SEE experiment, the device-under-test (DUT) is exposed to a known, fixed fluence (ions/cm^2) while the DUT is monitored for failures. This is analogous to fixed-time reliability testing and, more specifically, time-terminated testing where the reliability test is terminated after a fixed amount of time whether or not a failure has occurred (in the case of SEE tests fluence is substituted for time and hence being a fixed fluence test). Calculating a confidence interval specifically provides a range of values which is likely to contain the parameter of interest (the actual number of failures/fluence). Confidence intervals are constructed at a specific confidence level. For example, a 95% confidence level implies that if a given number of units were sampled numerous times and a confidence interval estimated for each test, the resulting set of confidence intervals brackets the true population parameter in about 95% of the cases.

To estimate the cross-section from a null-result (no fails observed for a given fluence) with a confidence interval, we start with the standard reliability determination of lower-bound (minimum) mean-time-to-failure for fixed-time testing (an exponential distribution is assumed) in Equation 3:

$$MTTF = \frac{2nT}{\chi^2_{2\left(d+1\right);\,100\left(1-\frac{\alpha}{2}\right)}} \tag{3}$$

where

- *MTTF* is the minimum (lower-bound) mean-time-to-failure
- *n* is the number of units tested (presuming each unit is tested under identical conditions)
- *T* is the test time
- χ^2 is the chi-square distribution evaluated at 100(1 – α / 2) confidence level
- *d* is the degrees-of-freedom (the number of failures observed)

With slight modification for our purposes we invert the inequality and substitute *F* (fluence) in the place of *T* as shown in Equation 4:

$$MFTF = \frac{2nF}{\chi^2_{2\left(d+1\right);\,100\left(1-\frac{\alpha}{2}\right)}} \tag{4}$$

where

- *MFTF* is mean-fluence-to-failure
- *F* is the test fluence
- X^2 is the chi-square distribution evaluated at 100(1 – α / 2) confidence
- *d* is the degrees-of-freedom (the number of failures observed)

The inverse relation between *MTTF* and failure rate is mirrored with the *MFTF*. Thus the upper-bound cross-section is obtained by inverting the *MFTF* as shown in Equation 5:

$$\sigma = \frac{\chi^2_{2(d+1);100\left(1-\frac{\alpha}{2}\right)}}{2nF} \quad (5)$$

Assume that all tests are terminated at a total fluence of 10^6 ions/cm^2. Also assume there are a number of devices with very different performances that are tested under identical conditions. Assume a 95% confidence level (σ = 0.05). Note that as *d* increases from 0 events to 100 events, the actual confidence interval becomes smaller, indicating that the range of values of the true value of the population parameter (in this case the cross-section) is approaching the mean value + 1 standard deviation. This makes sense when one considers that as more events are observed the statistics are improved such that uncertainty in the actual device performance is reduced.

Table A-1. Experimental Example Calculation of MFTF and σ Using a 95% Confidence Interval (1)

Degrees-of-Freedom (d)	2(d + 1)	χ^2 @ 95%	Calculated Cross-Section (cm^2)		
			Upper-Bound @ 95% Confidence	Mean	Average + Standard Deviation
0	2	7.38	3.69E–06	0.00E+00	0.00E+00
1	4	11.14	5.57E–06	1.00E–06	2.00E–06
2	6	14.45	7.22E–06	2.00E–06	3.41E–06
3	8	17.53	8.77E–06	3.00E–06	4.73E–06
4	10	20.48	1.02E–05	4.00E–06	6.00E–06
5	12	23.34	1.17E–05	5.00E–06	7.24E–06
10	22	36.78	1.84E–05	1.00E–05	1.32E–05
50	102	131.84	6.59E–05	5.00E–05	5.71E–05
100	202	243.25	1.22E–04	1.00E–04	1.10E–04

(1) Using a 95% confidence interval for several different observed results (d = 0, 1, 2,…100 observed events during fixed-fluence tests) assuming 10^6 ions/cm^2 for each test. Note that as the number of observed events increases the confidence interval approaches the mean.

B References

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2. G. Bruguier and J. M. Palau, "Single particle-induced latchup", *IEEE Trans. Nucl. Sci., Vol. 43(2)*, Mar. 1996, pp. 522-532.
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11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (Feb 2023) to Revision B (Oct 2024)	Page
• Added discussion of supply ESD clamp structure vulnerability in *Abstract*, *SEE Mechanisms*, and *Summary*	1
• Added description of MSU FRIB facility in *Irradiation Facility and Setup*	5
• Added *Extended Characterization* section and *Correlation Test Results*, *Root Cause*, and *SEL Prevention* subsections	16
• Changed formatting of *References* section and added reference for the MSU FRIB	21

Changes from Revision * (February 14, 2023) to Revision A (February 24, 2023)	Page
• Added clarification of supply voltage conditions to Section 2	3
• Changed *LMP7704-SP Bias Diagram* in Section 3 to correct V- power supply label	4
• Changed *LMP7704-SP SEL Conditions* table in Section 5 to correct units for Flux and Fluence	5
• Changed *SET Results* tables in Section 6 to add units for Fluence	6

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