Application Report
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Overcurrent Protection in High-Density GaN Power Designs

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ABSTRACT

With GaN devices, power electronics designers are now able to push the switching frequency of their designs to levels not possible with today's Si MOSFETs. Higher switching frequencies reduce the size of passive components in the system and in turn increase the overall power density. To make these solutions robust, protection against overcurrent events is needed. Traditional approaches using current sense transformer, shunt resistors, or de-saturation detection circuits remain ineffective due to slow response time. These techniques may also adversely affect the system performance by adding parasitic inductances and resistances in the power loop that may require slowing down GaN switching speed or cause additional power losses in the system. To solve this challenge, TI's LMG341X family of GaN power stages provide an integrated OCP function. This high-speed feature can turn off the GaN FET in less than 100-ns in an overcurrent or short-circuit event. This application note explains the importance of this feature as well as "latched" or "cycle-by-cycle" modes of operation.

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Trademarks

1 Why is Short-Circuit Protection a Must in GaN Applications?

Shoot-through and short-circuit are common failure modes in power supplies. Power converter designers do their best to minimize the risk of these type of failures based on the data provided by the component suppliers. However, there is always a risk of short-circuit and shoot-through events and power converter designers address it in their designs by adding necessary protection circuits. Short-circuit or shoot-through can occur due to many reasons including:

- Controller-related:
  - malfunctioning controller or glitching
  - inadequate dead-time
- Mechanical and environmental stresses
  - vibration, moisture, loose particles, and so forth

The protection schemes are fairly mature for Si based MOSFETs and IGBTs. In low power < 300-W, high-frequency Si MOSFET applications such as a diode bridge power factor correction (PFC) circuit, Si MOSFET is paired with a fast recovery SiC diode. This structure eliminates the risk of a shoot-through and therefore additional protection may not be included for cost reasons. In half-bridge applications such as motor drives, the current on low-side FET is monitored with a current sense resistor. For IGBTs, de-saturation based protection schemes are included in the gate driver.

GaN FETs, on the other hand, require much faster protection than Si FETs due to these two reasons:

- For the same blocking voltage and on-state resistance, the chip area is much smaller than Si FETs. It is more difficult to dissipate a significant amount of joule heating during a short-circuit condition.
- Unlike IGBTs, GaN FETs normally operate in the linear region. In the event of a short-circuit, GaN FET can enter into saturation region. This would cause excessive power dissipation. Therefore, overcurrent must be detected in the linear region.

To protect a half-bridge configuration from all overcurrent events, both the high and low side devices must be protected individually. The following section will discuss the details.

2 Why is Overcurrent Protection a Must in GaN Applications?

The power devices can experience overcurrent due to many reasons including:

- application use conditions such as transient load steps, overloading, start-up current,
- source related transients such as AC line brownout,
- magnetic component saturation.

The image shown in Figure 1 shows an example of a transient current captured during a line transient from a power factor correction (PFC) circuit running at 750-W of power. During the transient, the current increases about 3 times of its steady-state value. During AC brownouts or start-ups under heavy load, similar transients can be observed. For instance, in higher power server telecom applications such as > 2kW PFC, the current can reach to 35-A during the transients. This high transient current may cause a thermal failure in GaN power switches due to high power dissipation.

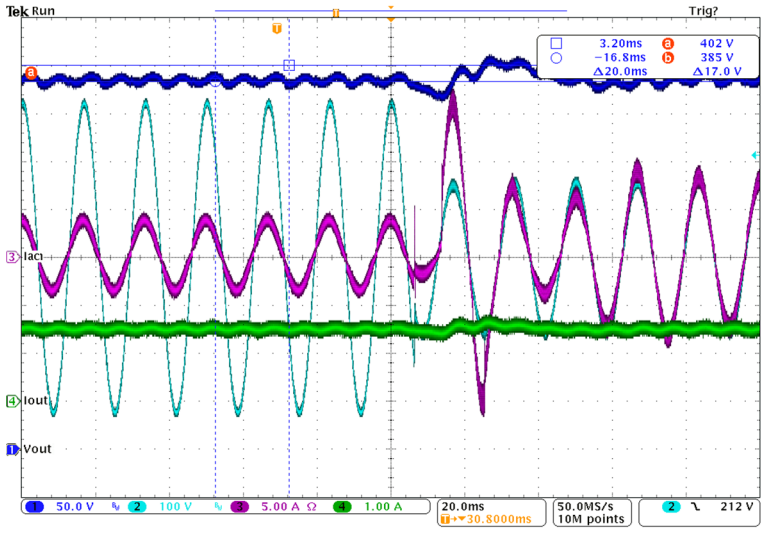

Figure 1. Transient Current of a PFC Circuit During an AC Line Voltage Change

3 Discrete Implementation of Overcurrent Protection

Discrete implementation of OCP schemes such as shunt resistors or current transformers introduce additional cost, board space, and increase in parasitic inductance that limits system performance. Another typical approach is to sense drain-source voltage (VDS) of GaN FET, that does not impact the system performance but lacks accuracy due to the large temperature coefficient of GaN. All of these methods require a current-sensing element, a level shifter to report the signal to the controller, and a detection circuit including a fast comparator, filters, and blanking circuits. Table 1 summarizes the performance, system impact, required components, area and cost comparison of the above mentioned discrete and LMG341X's integrated OCP schemes.

Table 1. Comparison of OCP Methods

OCP Option	OCP Performance	System Impact	Required Component	Area / Cost
Shunt Resistor	+ Low tolerance resistors can provide good accuracy	– High power loop inductance and power losses	– Sense resistor, detection circuit, level shifter	– Medium / Medium
Current Transformer	+ 0.1% linearity	– High power loop inductance, and it does not protect at high duty cycles	– Current transformer, detection circuit	– Large / High
VDS Sensing	– Process variations of FETs and large Rdson tempco	+ None	– Detection circuit, level shifter	– Medium / Medium
Integrated OCP	+ <100ns response time	+ None	– Level shifter	+ No external components

The shunt resistor based OCP scheme provides a good compromise between current transformer based scheme and VDS sensing schemes. It can achieve better accuracy than VDS sensing method while has lower parasitic inductance in comparison to current transformer-based approach. Figure 2 shows the necessary blocks needed for a shunt resistor based OCP implementation. As mentioned above, a shunt resistor, a detection circuit with a fast comparator, and a blanking time circuit is required for each OCP circuit. In addition, a level shifter for the high-side GaN is required for reporting the fault condition to the controller.

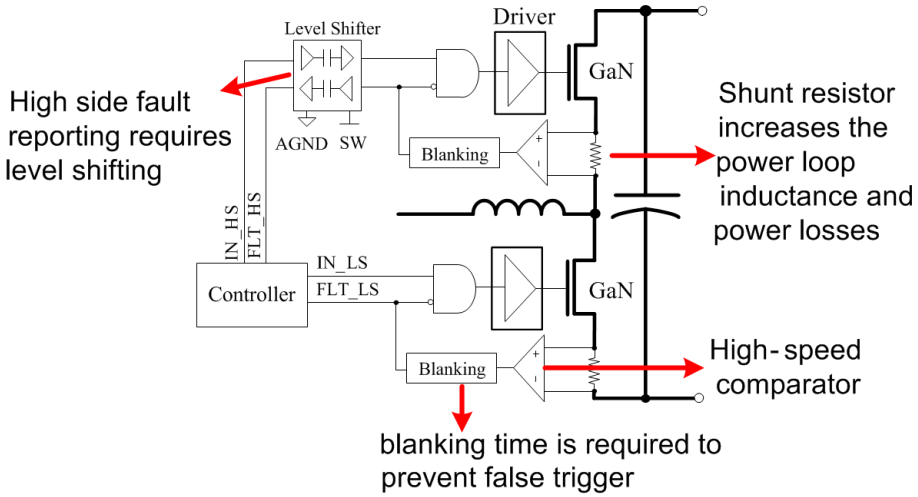

Figure 2. Block Diagram of Shunt Resistor Sensing Based Discrete OCP Implementation

An example board layout is shown in Figure 3. This example uses two shunt resistors in parallel to reduce the added power loop inductance. Considering the both high-side and low-side OCP circuits, a total of four shunt resistors are considered. This adds about 1.2-nH to the power loop. As a result of the large power loop inductance, the GaN FETs can no longer be switched at high speeds, that is, 100-V/ns due to increased voltage overshoot during switching instants. Moreover, the sense resistor adds to the on-state resistance of the GaN FET. Both of these system level complications cause additional power losses in the system. For 100-kHz switching converter, and a 5-mΩ sense resistor results in a power loss of 0.2-W at 1-kW output power, and 0.75-W loss at 2-kW of output power. The circuit also adds 233-mm^2 in board space. The system level impacts of a discrete solution are summarized in Table 2.

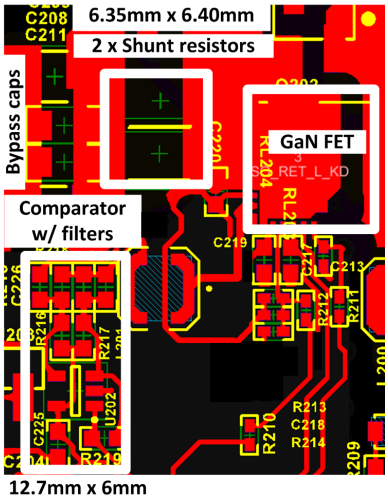

Figure 3. Example Board Layout of a Discrete Shunt Resistor Implementation

Table 2. System Level Impact of a Shunt Resistor Based OCP Implementation

Shunt Resistor	Resistive Shunt 2 × 10 mΩ in parallel
Added PCB Area	233 mm^2
Added Power Loop Inductance	1.2 nH
dv/dt	80 V/ns
Additional Power Loss at 100 kHz, Po = 1 kW	0.2 W
Additional Power Loss at 100 kHz, Po = 2 kW	0.75 W

4 LMG341XRxxx - Integrated Overcurrent Protection

To provide a fast and reliable protection of the system, the LMG341X power stage integrates an OCP function, as shown in the simplified block diagram in Figure 4.

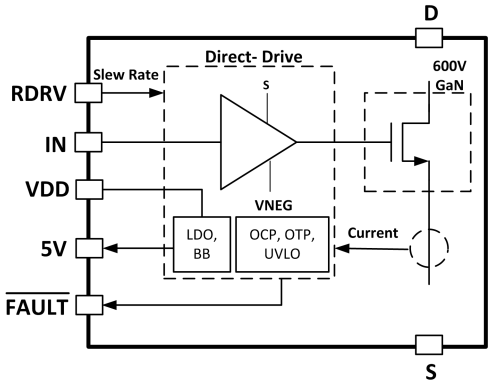

Figure 4. Simplified Block Diagram of LMG341XRxxx GaN Power Stage

The OCP circuit monitors the LMG341X's drain current and compares that current signal with an internally set limit. Upon detection of the overcurrent, the family of LMG341X has two optional protection actions:

1. latched overcurrent protection – in LMG3410Rxxx
2. cycle-by-cycle overcurrent protection – in LMG3411Rxxx

4.1 LMG3410R070's Latched OCP Function

The LMG3410R070 provides a latched OCP option, by which the FET is shut off and held off until the fault is reset by either holding the IN pin low for more than 350 microseconds or removing power from VDD. This part is designed for applications where the operation should be interrupted when a fault happens. These include industrial drives as well as safety critical applications. Moreover, latched protection is preferred in applications where controller cannot respond to fault signal.

The OCP is blanked to prevent mis-trigger during the switch node transitions. The blanking time is internally adjusted based on the slew rate. The blanking time for different slew rate settings of LMG341XR070 can be found in the datasheet. Higher slew rates require shorter blanking time as switch node transits faster. The OCP function has less than 100-ns response time when RDRV pin, that is used to adjust the gate drive strength, is set to 15-kΩ. This allows the hard switching turn-on edge to have 100-V/ns slew rate. Therefore, fast response OCP circuit protects the GaN device even under a hard short-circuit condition.

Figure 5 shows the test setup and OCP performance of LMG3410R070 during the shoot-through event. The high-side LMG3410R070 is kept on by supplying 5-V to its IN pin. While it is on, the low-side LMG3410R070 is turned on with a 500-ns pulse. In this case, the high-side GaN FETs OCP is triggered earlier than that of the low-side GaN FET as it was already on and the blanking time has already passed. The response time in this case was less than 40-ns. Due to low loop inductances, the DC bus voltage only peaks up to 550-V, which is well within the voltage spec of the device.

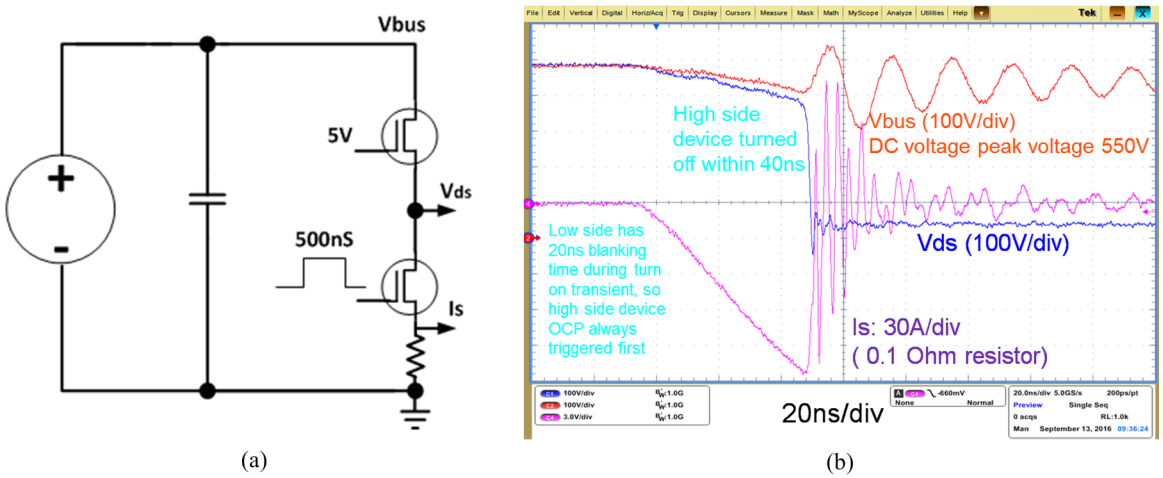

Figure 5. LMG3410R070's Shoot-Through Protection Performance: (a) Test Circuit, (b) Experimental Waveform

The OCP performance of LMG3410R070 during a short-circuit event is shown in Figure 6. In this case, the high-side switch is physically shorted with a help of wire, and a 500-ns pulse is sent to IN pin of low-side GaN FET. This time, low-side GaN FET waits for the blanking time dependent on the RDRV resistance placed. After the blanking time, overcurrent is detected and GaN FET is turned off immediately. The total response time is less than 90-ns.

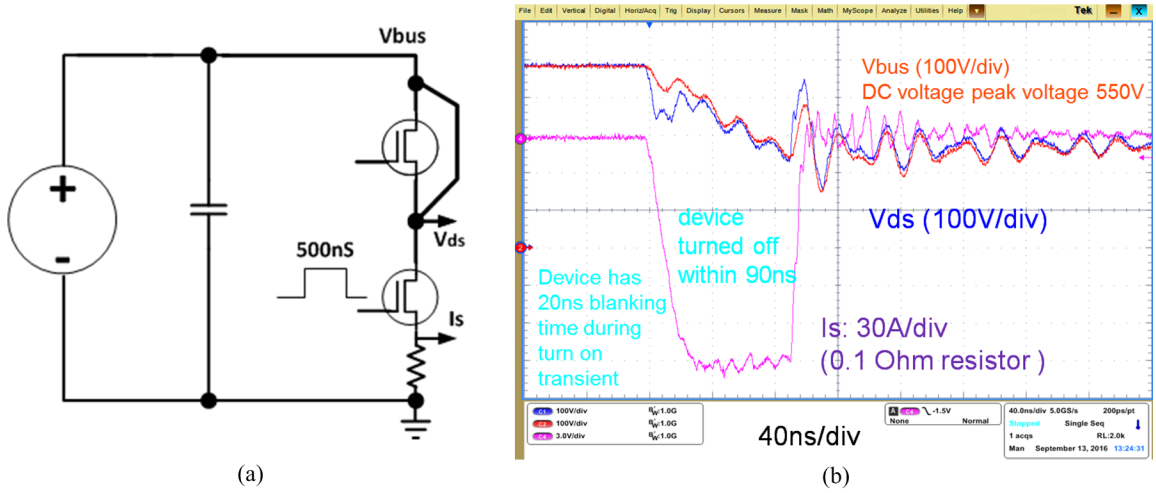

Figure 6. LMG3410R070's Short-Circuit Protection Performance: (a) Test Circuit, (b) Experimental Waveform

4.2 LMG3411R070's Cycle-by-Cycle OCP Function

The LMG3411R070 provides cycle-by-cycle OCP option. In this mode, the GaN FET is turned off when overcurrent happens, but the output fault signal will clear after the input PWM goes low. In the next cycle, the FET can turn on as normal. The cycle-by-cycle function can be used in cases where steady-state operation current is below the OCP level but transient response can still reach high current, while the circuit operation cannot be paused. Typical applications include server and telecom power supplies.

During cycle-by-cycle operation, after the current reaches the upper limit with the PWM input still high, the load current can flow through the third quadrant of the other FET of a half-bridge with no synchronous rectification. The extra high negative voltage drop (–6 V to –8 V) from drain to source could lead to high third quadrant loss, similar to dead time loss but with much longer time. Therefore, it is critical to design the control scheme to make sure the number of switching cycles in cycle-by-cycle mode is limited, or to change PWM input based on the fault signal to shorten the time in third quadrant conduction mode of the power stage.

An experimental waveform of a LMG3411R070 operation is given in Figure 7. As shown in Figure 7, the inductor current slowly ramps up and OCP shuts off the GaN FET whenever OCP threshold value, 35-A, is exceeded. Different than the LMG3410R070, this time fault is not latched and reset every switching cycle as soon as IN pin goes low. This automatically limits the current being transferred to output in a reliable manner, which eliminates the need for a software overcurrent monitoring scheme.

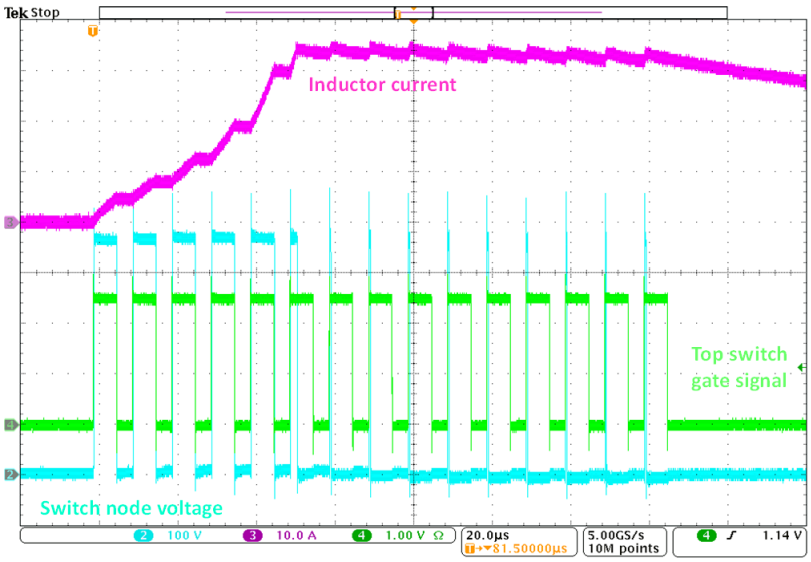

Figure 7. Experimental Waveform Showing Cycle-by-Cycle OCP Performance of LMG3411R070

5 Summary

Ultra-fast and reliable OCP is a must in GaN-based applications due to small active chip area and possibility to enter into saturation region during a short-circuit event. The response time of the OCP circuit should be less than 250-ns to be able to prevent short-circuit failures. Traditional discrete implementations of OCP either degrade system performance by adding inductance to the power loop and resistance to the current flow path resulting in higher power losses, or unable to achieve good accuracy which impacts to the response time. Moreover, discrete approaches add to the footprint area and cost of the total solution. TI's LMG341X family of GaN power stages offer an integrated OCP function with less than 100-ns response time. LM3410Rxxx family provides a "latched" version while LMG3411Rxxx family integrates a "cycle-by-cycle" OCP function. The integration of this robust and ultra-fast OCP function makes sure GaN FETs are protected even under hard-short circuit condition and gives a piece of mind to the users.

6 References

- *LMG341xR070 600-V 70-mΩ GaN With Integrated Driver and Protection* data sheet (SNOSD10)

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