Application Report

Thermal Considerations for Designing a GaN Power Stage

Serkan Dusmez, Yong Xie, Masoud Beheshti, and Paul Brohlin

ABSTRACT

Thermal design is an important consideration in any power electronic converters. An optimized thermal design enables engineers to use GaN in a wide range of power levels, topologies, and applications. This application note discusses the most important tradeoffs and considerations for TI's LMG341XRxxx GaN power stage family, including guidance for PCB layout, thermal interface, heat sink selection and mounting methods. Examples of designs using 50-mΩ and 70-mΩ GaN devices will also be provided.

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1 Introduction

GaN FETs have enabled high-frequency power converter designs that are much higher in power density, smaller in size, and are light-weight due to superior switching characteristics and lack of reverse recovery losses. To get full benefit of GaN's fast switching speeds, the power loop inductance needs to be minimized. This necessitates careful PCB layout as well as very low inductance package for GaN FETs. TI's LMG341XRxxx family uses 8-mm × 8-mm low inductance bottom side cooled QFN package for switching speeds of greater than 100 V/ns. A good thermal design is important for power electronic converters. An ideal heat transfer should provide good thermal conductivity with minimum thermal resistance in the heat flow path. Figure 1-1 shows a typical equivalent thermal circuit, which includes the thermal resistance of junction to case of GaN FET, PCB, thermal interface material (TIM), and heat sink. The junction temperature of GaN FETs is a function of power losses and total thermal resistance from junction to air. The junction temperature can be estimated as Equation 1.

$$T_j = P_{Loss} \times R\theta_{j\text{-}a} + T_{amb} \quad (1)$$

where

- T_j is the junction temperature
- P_{Loss} is the total dissipated power
- $R\theta_{j\text{-}a}$ is the total thermal resistance
- T_{amb} is the ambient temperature

The engineer can use Equation 2 to approximate $R\theta_{j\text{-}a}$.

$$R\theta_{j\text{-}a} = R\theta_{j\text{-}c(bottom)} + R\theta_{PCB} + R\theta_{TIM} + R\theta_{hs} \quad (2)$$

where

- $R\theta_{j\text{-}c(bottom)}$ is the thermal resistance between junction of the die and package DAP
- $R\theta_{PCB}$ is the thermal resistance of the PCB
- $R\theta_{TIM}$ is the thermal resistance of the TIM
- $R\theta_{hs}$ is the thermal resistance of the heat sink

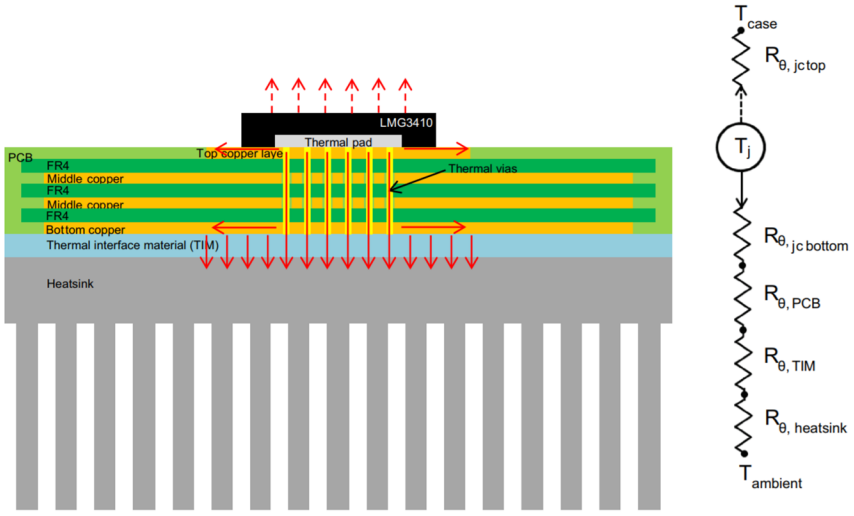

Figure 1-1. QFN Package on a PCB (Green), TIM (Blue) and Heat Sink (Gray)

The top path resistance, depicted by dotted arrows in Figure 1-1, is minimal compared to the bottom path resistance in forced cooled applications. In a typical bottom-cooled configuration where thermal vias, finned heat sink, and sufficient air flow are used, less than 10% of the dissipated heat goes through the top path.

2 Thermal Considerations

2.1 Package Thermal Resistance

TI's LMG341XRxxx GaN power stages are in low inductance QFN packages to avoid high inductance of long leads and bond wires for fast switching speeds. The thermal pad placed on the bottom of the device is soldered down to the board and used to effectively spread the heat from the junction down to the PCB. The typical junction to case thermal resistance is 0.5°C/W.

2.2 PCB Stack

The heat from the junction is transferred from the thermal pad to the top layer of the PCB, and then to the bottom layer of the PCB through a number of thermal vias. The thermal resistance of the PCB is a function of the board thickness, copper thickness of layers, orientation, and number of thermal vias.

2.2.1 Copper Thickness of Layers

The top copper layer acts as a heat spreader. As the copper layer area increases, the effective thermal resistance in the vertical direction decreases. The heat spreading reaches saturation beyond a certain point, which is determined by the copper thickness. Therefore, it is beneficial to have large and thick top copper layer that is larger than the thermal pad area. An example heat spreader on top copper layer (shown in red) from LMG3410R050-HB-EVM board is shown in Figure 2-1.

The internal copper layers spread out the heat flux and increase the heat conduction area. The bottom copper layer makes contact with TIM. It is important that the bottom layer Cu area covers an area of the thermal plane placed on the top Cu layer, and has sufficient Cu thickness for heat spreading. For these reasons, TI recommends that the engineer use at least 2-oz copper in each layer. It is also important to remove solder mask of this heat spreading plane to reduce thermal resistance.

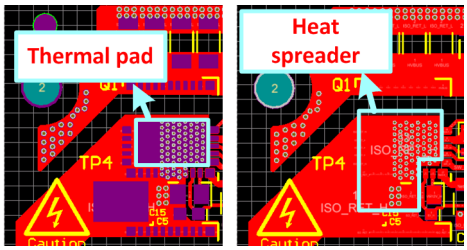

Figure 2-1. Thermal Pad of LMG341X GaN Power Stage and Top Copper Layer Heat Spreader of LMG3410R050-HB-EVM

2.2.2 Board Thickness

The board thickness is determined by the number and thickness of layers, electrical routing, and the requirements for mechanical strength, and has a direct impact on the total thermal resistance from the GaN package to the TIM surface. As the board thickness increase, the thermal resistance increases proportionally.

To minimize the power loop inductance, a 4-layer board is recommended such that power loop can be returned from the adjacent layer. An example board layer stack is shown in Figure 2-2. Typically, the dielectric 2 thickness is changed to get thicker or thinner boards. The minimum thickness is determined by the signal isolation requirement of adjacent layers considering the signal integrity of critical signals and added parasitic capacitance to the switch node. A minimum of 32-mils board thickness with 2-oz copper is recommended for low power levels less than 1-kW, where dielectric 2 thickness is 10.6-mils.

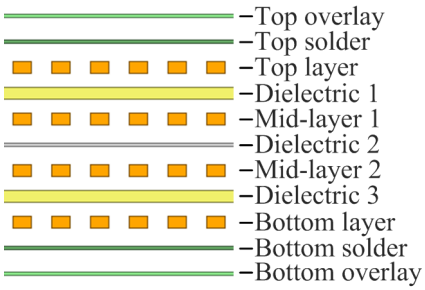

Figure 2-2. An Example Layer Stack of a 4-Layer Board

For higher power levels >1-kW, TI recommends a minimum of 47-mils thickness to prevent board warpage and to accommodate different heat sink mounting methods. In this case, the dielectric 2 thickness is increased to 25.8-mils.

2.2.3 Number of Thermal Vias

FR-4 material is a poor thermal conductor. Its conductivity can be improved using plated thermal vias. The thermal vias, typically 8-12 mils in diameter, should be placed right under the thermal pad of the GaN package. The thermal vias placed on the LMG3410R050-HB-EVM are shown in Figure 2-1. There are 71 vias for each GaN with a hole size of 8-mils. All layers including the internal layers have thermal planes for better heat spreading and transfer.

To improve the power loop inductance, the entire plane under the thermal pad of the device should not be filled with thermal vias. The reason is that the power loop is returned on the mid-layer 1 and underneath the devices to minimize the power loop inductance, as discussed in the application note *High Voltage Half Bridge Design Guide for LMG3410 Smart GaN FET* (SNOA946).

2.2.4 PCB Thermal Resistance

The total thermal resistance of the PCB can be approximated to the equivalent thermal resistance of the thermal vias that are conducting the heat in parallel. The engineer can use Equation 3 to calculate the thermal resistance of each via.

$$R_{via} = \text{Resistivity} \times L / A \tag{3}$$

where

- L and A denote the length and area of the thermal via, respectively

The thermal resistivity of a plated Cu is 0.249 cm-K/W (at 300K). The length of the via is approximately equal to the board thickness. The area of the conductive Cu plated wall of via is expressed as Equation 4:

$$A = (dia + p_{thk}) \times p_{thk} \times \pi \tag{4}$$

where

- dia and p_{thk} represent the diameter and plated wall thickness, respectively

The typical via is plated with 25-µm copper. Using Equation 3 and Equation 4, thermal resistance of a single thermal via in LMG3410R050 HB-EVM board is calculated as 166°C/W, which makes the total PCB thermal resistance as 2.33°C/W. Similarly, the LMG3410R070 HB-EVM board is using 39 vias with a 12-mils diameter and a board thickness of 32-mils, which makes the total board thermal resistance 2°C/W. This estimation is based on filling the vias with conductive epoxy. For better thermal performance, a costly alternative Cu via filling can be considered.

2.3 Thermal Interface Material (TIM)

A thermal interface material (TIM) is used to thermally couple and electrically insulate the heat sink from the bottom copper layer of the PCB. A certain thickness is required to provide gap filling to make a good thermal interface.

Commonly used TIM are shown in Table 2-1 and include:

- Adhesive: This type of TIM does not need constant pressure however they usually have low thermal conductivity due to the addition of adhesives into the material.
- Gap pad: Typically has the best thermal conductivity but have higher thermal resistance at the contact interfaces (PCB to TIM and heat sink to TIM). Gap pads require a mounting mechanism that keeps constant pressure between the heat sink and the PCB.
- Phase change material: This TIM's thermal conductivity lies between adhesive and gap pad types, but has the capability to wet the contact interface thus providing the most consistent performance. It also needs the heat sink to be mounted with pressure.

The gap filling material shows the highest thermal conductivity but at a larger thickness. Under pressure, this material can compress up to 50%, which significantly improves the thermal resistance. However, large pressure of >100 psi can cause board warpage and result in mechanical failure of the PCB. Also unequal pressure on the bottom copper layer can lead to uneven thermal resistance and temperature of GaN FETs. On the other hand, phase changing material does not require large compression force as its thermal resistance does not change significantly with compression force.

Adhesive TIM, on the other hand, shows a larger thermal resistance than the other two types of materials. However, it is one of the few alternatives when using smaller heat sink as will be depicted in Section 2.4 while providing an easier assembly process.

A practical method to compare and select TIM is to measure the thermal resistance from junction to the surface of the TIM, shown as $R\theta_{j\text{-}s}$ in Figure 1-1. Our lab measurements are summarized in Table 2-1. Cost should also be a consideration in the selection process.

Table 2-1. TIM Property and Performance Comparison

TIM	Part	Thermal Conductivity	Thickness	Breakdown Voltage	Measured $R\theta_{j\text{-}s}$
Phase change	HF300P	1.6 W/m-K	0.1mm	50 kV/mm	5.5 C/W
Gap filling pad	GR45A	6 W/m-K	0.5mm	17 kV/mm	6 C/W
Adhesive	Bondply-100	0.8 W/m-K	0.1mm	30 kV/mm	8 C/W

For some applications, where radiated EMI can be suppressed with enclosed metal casing, non-insulating TIMs such as thermal grease or direct soldering of heat sink may be a viable option for reducing the thermal resistance significantly. Direct soldering of heat sink down to the PCB requires electro-plating of the Al heat sink baseplate with either TIN-lead or silver. This is a custom design approach and may be more costly than using thermal grease.

2.4 Heat Sink

Heat sink is one of the most important element of thermal management, and it impacts the overall power density of the system. For low power applications less than 1-kW, the heat sink size is typically less than 30 mm × 30 mm. It is difficult to find mounting mechanism for these smaller heat sinks, so adhesive TIM are typically used.

At higher power levels > 1-kW, the performance of thermal management becomes more important. For heat sinks equal to and larger than 30 mm × 30 mm, attached push-pin heat sink can be coupled with better thermal conductivity TIMs. For heat sinks larger than 35 mm × 35 mm, QSZ clips with anchor pins are preferred. The advantage of attached push-pin heat sink is that the compression force can be easily adjusted with spring and push-pin combinations. The applied force is not uniformly distributed, however, middle of the heat sink experiences the minimal pressure while the corners experiences the highest pressure where force is applied.

QSZ clips, on the other hand, have bars that run in the middle of the heat sinks to push down the heat sink base to the thermal interface underneath. This keeps a relatively constant pressure across the interface and provides a more consistent thermal interface than a corner-mounting mechanism. The applied pressure, however, can be too high to warp the PCB, which dictates the thickness of the daughter card PCB. The thicker the PCB is, the higher the thermal resistance becomes on the PCB stack. Therefore, TI recommends that the engineer use attached push-pin heat sinks for daughter card designs and QSZs clip with anchor pins in applications where GaN FETs are mounted on the main board. Table 2-2 summarizes the discussion above about heat sinks.

Table 2-2. Heat Sink Mounting Mechanisms

Heatsink dimension	Mounting mechanism	Advantage	Disadvantage	Recommended Use Case
<30x30mm	Adhesive TIM	Easy mounting – no pressure is needed	Low thermal conductivity	Low power <1kW
≥30x30mm	Push-pin attached	Adjustable applied force with spring and push-pin combinations	Uneven pressure	>1kW on daughter card board
>35x35mm	QSZ clip with anchor pins	Uniform pressure across heat sink surface	Possible board warpage due to applied force	>1kW on main power board

3 Design Example: Totem-Pole PFC Converter

Totem-pole (TP) power factor correction (PFC) is a common power topology for GaN-based converters in various industrial, telecom, and server application. Thermal management plays an important role in achieving the system efficiency and power density targets in these designs. Typical system specifications are summarized in Table 3-1.

Table 3-1. TP PFC Converter Operation Specifications

Parameters	Value
Input voltage (Vin)	230 V
Output voltage (Vo)	400 V
Slew rate transition	100 V/ns
Tambient	50 °C
Tj,max	110 °C
Dead-time	50 ns

3.1 Thermal Optimization and Performance for <1.2-kW Designs

For these applications, smaller heat sinks mounted using adhesive type TIMs are typically sufficient. The LMG3410R070-HB-EVM board, shown in Figure 3-1, is designed using a 32-mils board with 39 of 12-mils diameter vias for heat transfer for high-side GaN FET and Bondply-100 as the TIM.

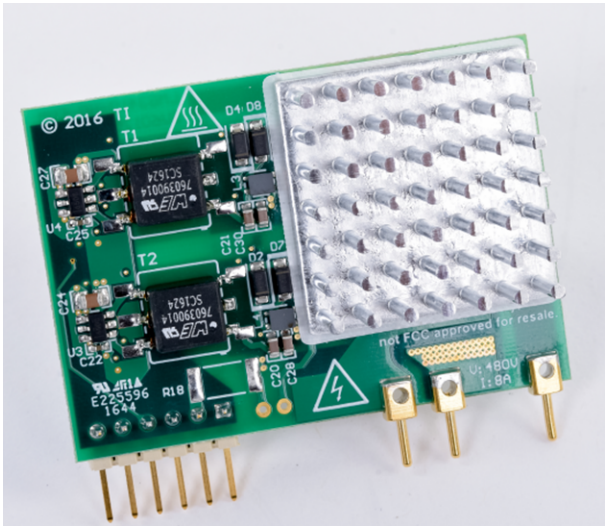

Figure 3-1. 1.2-kW Half-Bridge Design

With these board parameters, the measured junction to heat sink thermal resistance is about 8°C/W, which leaves about 5.5°C/W for the TIM itself under 400-LFM forced air cooling, as summarized in Table 3-2. To cover 1.2-kW at 100-kHz switching frequency, a 20-mm × 20-mm × 10-mm heat sink is chosen, which roughly gives a junction to ambient thermal resistance about 16.4°C/W per FET.

Table 3-2. LMG3410R070-HB-EVM Thermal Resistance at 400-LFM Forced Air Cooling

Thermal Resistance	Value [°C/W]
Junction to case thermal resistance ($R\theta_{j-c}$)	0.5
PCB thermal resistance for high side LMG3410R070 ($R\theta_{PCB}$)	2
Estimated TIM thermal resistance ($R\theta_{TIM}$)	5.5
Heat sink thermal resistance ($R\theta_{hs}$) per FET	8.4
Total junction to air thermal resistance ($R\theta_{j-a}$) per FET	16.4

With the 20-mm × 20-mm × 10-mm heat sink, the expected power losses from LMG3410R070-HB-EVM board and estimated junction temperatures are plotted in Figure 3-2 and Figure 3-3. These curves provide information on what to expect from LMG3410R070-HB-EVM in a TP PFC application with application specifications given in Table 3-1.

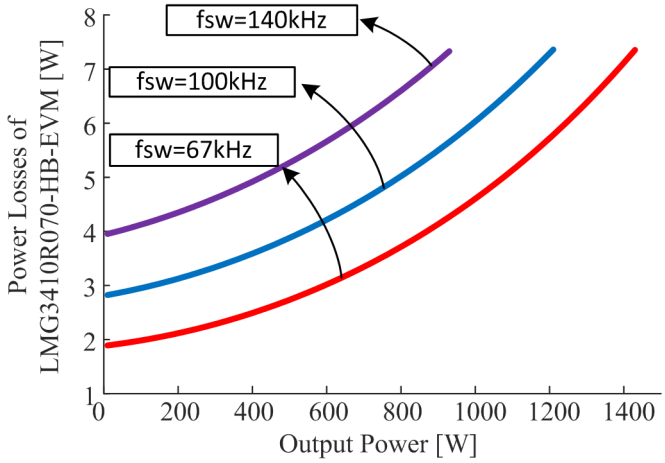

Figure 3-2. Power Losses of LMG3410R070-HB-EVM Board for TP PFC Applications at 400-LFM Cooling

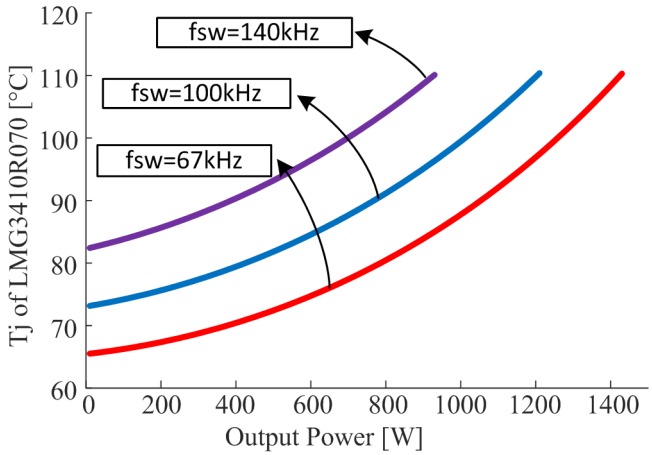

Figure 3-3. Junction Temperature of High-Side LMG3410R070 in TP PFC Applications at 400-LFM Cooling

LMG3410R070-HB-EVM is tailored for 1.2-kW applications using adhesive TIM. Table 3-3 shows the air cooling required for the LMG3410R070-HB-EVM board for various power levels.

Table 3-3. Required Cooling for LMG3410R070-HB-EVM With Respect to Power Levels

Output Power	Switching Frequency					
	67kHz		100kHz		140kHz	
	HB Loss	Airflow	HB Loss	Airflow	HB Loss	Airflow
3oo W	2.3 W	Natural convection	3.3 W	Natural convection	4.6 W	100 LFM
600 W	3.1 W	Natural convection	4.3 W	100 LFM	5.7 W	200 LFM
900 W	4.2 W	100 LFM	5.5 W	150 LFM	7.1 W	400 LFM
1200 W	5.8 W	200 LFM	7.2 W	400 LFM	8.9 W	>2000 LFM

3.2 Thermal Optimization and Performance for >1.2-kW Designs

The thermal management design for higher power applications requires a better TIM and larger heat sink. The LMG3410R050-HB-EVM, shown in Figure 3-4, uses Gr-45A gap filling pad TIM and a board thickness of 47-mils to avoid any board warpage. Gap pad is chosen over phase change TIM, as it has lower cost and similar thermal performance. To achieve board thermal resistance of approximately 2.3°C/W, via diameter is set to 8-mils with 71 thermal vias used. The TIM thermal resistance is approximately 3.2°C/W. With a 30-mm × 30-mm × 20-mm push-pin heat sink, the total thermal resistance from junction to air per FET is 9.2°C/W, as summarized in Table 3-4.

Figure 3-4. 2-kW Half-Bridge Design

Table 3-4. LMG3410R050-HB-EVM Thermal Resistance at 400-LFM Forced Air Cooling

Thermal Resistance	Value [°C/W]
Junction to case thermal resistance ($R\theta_{j\text{-}c}$)	0.5
PCB thermal resistance for high side LMG3410R050 ($R\theta_{PCB}$)	2.3
Estimated TIM thermal resistance ($R\theta_{TIM}$)	3.2
Heat sink thermal resistance ($R\theta_{hs}$) per FET	3.2
Total junction to air thermal resistance ($R\theta_{j\text{-}a}$) per FET	9.2

Based on the thermal stack of LMG3410R050-HB-EVM, as discussed in Table 3-3, the expected power losses and junction temperature of high-side GaN FET is shown in Figure 3-5 and Figure 3-6. These curves provide information on what to expect from LMG3410R050-HB-EVM in a TP PFC application.

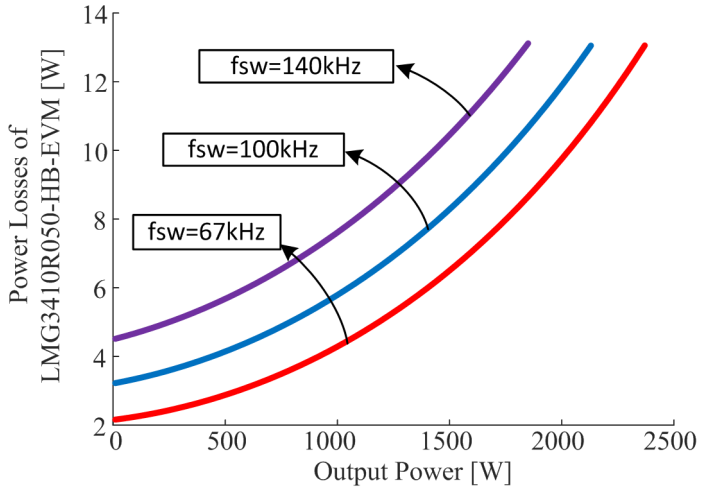

Figure 3-5. Power Losses of LMG3410R050-HB-EVM Board for TP PFC Applications at 400-LFM Cooling

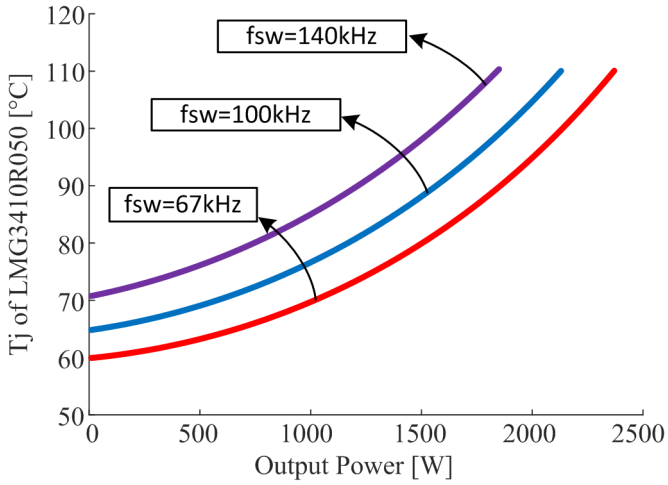

Figure 3-6. Junction Temperature of High-Side LMG3410R050 in TP PFC Applications at 400-LFM Cooling

The LMG3410R050-HB-EVM is tailored for 2-kW applications using a gap filling pad. Table 3-5 shows the air cooling required for the LMG3410R050-HB-EVM board for various power levels.

Table 3-5. Required Cooling for LMG3410R050-HB-EVM With Respect to Power Levels

Output Power	Switching Frequency					
	67 kHz		100 kHz		140 kHz	
	HB Loss	Airflow	HB Loss	Airflow	HB Loss	Airflow
1200 W	5.1 W	Natural convection	6.7 W	Natural convection	8.6 W	100 LFM
1500 W	6.5 W	Natural convection	8.3 W	100 LFM	10.4 W	150 LFM
1800 W	8.3 W	100 LFM	10.3 W	150 LFM	12.7 W	400 LFM
2100 W	10.6 W	150 LFM	12.8 W	400 LFM	15.5 W	>2000 LFM
2200 W	11.4 W	200 LFM	13.7 W	600 LFM	16.5 W	-

4 Summary

Thermal performance is as important as the electrical and magnetic component performances impacting the efficiency, reliability, and power density of power converters. This article briefly introduced the thermal stack and optimization of each component including PCB, thermal interface material, and heat sink. This guide particularly focused on a 1.2-kW half-bridge design using LMG3410R070 and a 2-kW design using LMG3410R050 on a totem-pole PFC example. This guide also discussed the expected half-bridge power losses and junction temperatures of GaN FETs in the designed EVMs, along with the required air cooling for different power levels.

5 References

- Eric Faraci and Jie Mao, *High Voltage Half Bridge Design Guide for LMG3410 Smart GaN FET*, TI application report (SNOA946)

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2018) to Revision B (August 2020)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2

Changes from Revision * (October 2018) to Revision A (October 2018)	Page
• Changed the *Junction Temperature of High-Side LMG3410R070 in TP PFC Applications at 400-LFM Cooling* graph	7

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