ADC32RF45: Amplifier to ADC Interface

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ABSTRACT

This application report discusses interfacing RF sampling ADCs and RF amplifiers.

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1   Introduction

System designs using amplifiers and analog-to-digital converters (ADC) should focus on using the best features of each device. Amplifiers provide power gain, isolation, voltage gain, and impedance transformation. Data converters would seem more simple, offering only the digitization of a voltage; however, the ADC sample rate is a degree of flexibility that can be quite powerful. This application note focuses on combining the best performance characteristics of amplifiers and ADCs for high speed, high linearity data capture. This document concentrates mainly on the LMH5401 family of amplifiers and the ADC32RF4x series of ADCs.

The LMH5401 family of amplifiers includes the LMH3401 fixed-gain amplifier, the LMH5401 fully-differential amplifier (FDA) and the LMH3404, dual-fixed-gain amplifier. Because the ADC32RF45 ADC is a dual-channel device, this document focuses on the LMH3404 amplifiers; however, the other amplifiers in the family can be used with similar design guidelines.

This application note covers a typical system design which is applicable to either high speed data acquisition or communications systems. Both the amplifier and the ADC are dual channel devices which will contribute to close phase and gain matching between channels. This is important for complex data sampling where one signal is composed of two signals that are 90 degrees out of phase and must be recombined digitally. This design focuses on a signal with up to 1 GHz of bandwidth (2 GHz for complex signals) and a single-ended signal source, such as an antenna or mixer. The system consists of the amplifier, a simple, anti-alias filter, and the ADC.

The LMH3404 amplifier offers excellent performance up to 1 GHz signal bandwidth. This amplifier also offers 20 dB of gain and up to a 5-V differential signal swing. It is an excellent choice for broad band, dual channel systems.

The LMH3404 amplifier has 7 GHz of –3-dB bandwidth, and the ADC34RF45 has an input bandwidth of 4 GHz. Without a noise filter between the amplifier and the ADC, the ADC samples all noise in the 4-GHz bandwidth of the ADC. In order to reduce the sampled noise, and also to reduce the harmonic distortion of the sampled signal, a low-pass filter is used between the amplifier and the ADC.

The ADC32RF45 is a high-performance, 14-bit, 3.0-GSPS ADC. With a 1.5-GHz first Nyquist zone, this ADC affords a very large amount of flexibility in filter design. With a 1-GHz desired signal bandwidth, there is an additional 1 GHz of frequency guard band to ensure that undesired noise and harmonic distortion products are rejected. Half of the frequency guardband is between the 1 GHz desired signal bandwidth and the 1.5 GHz first Nyquist band of the ADC. The other half of the frequency guardband is in the ADC second Nyquist band. Because the lower frequencies of the second Nyquist band alias into the upper portion of the first Nyquist band the guard band doubles. This illustrates the benefit of over-sampling, which is basically using a faster than necessary ADC to improve signal fidelity.

Designing a filter to pass the desired frequencies is fairly easy. However, one of the largest drawbacks to real filter implementation is the loss of signal through the filter, or insertion loss. This signal loss contributes dB-for-dB to the ADC noise figure. What may be even worse is that the amplifier driving the ADC will generate distortion at multiples of the filter loss. For example, if a filter has 7 dB of loss, the amplifier needs to drive a signal 7 dB stronger. This results in second-order products with 7 dB higher levels and third-order products will be 14 dB worse. Some of these distortion products (intermodulation in particular) cannot be filtered out, so keeping filter loss to a minimum is critical to system performance. For this reason this application report focuses on using a low loss, low component count filter.

As shown in [Figure 1](#) we are using a double terminated filter. The ADC input is approximately 50 Ohms, which can provide termination for the filter output; however, the LMH5401 output impedance is 20 Ω, so termination resistors are required. In this example termination resistors of 15 Ohms would be the best choice. The losses in this example are 6 dB in the termination resistors and 1 to 2 dB in the filter. Low order filters are easier to manufacture and have lower losses so use the lowest order filter that gives the required noise and harmonic attenuation. With over-sampling there is more frequency margin to allow flexibility in the filter design.
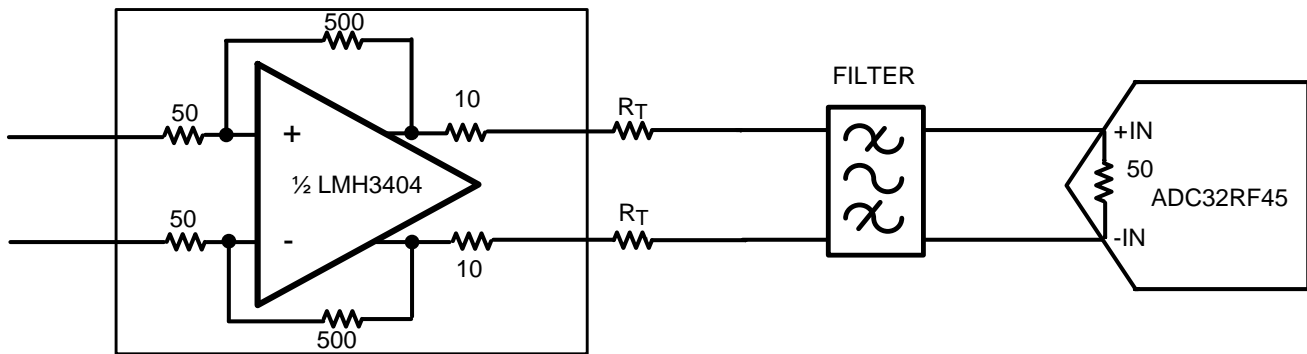
Figure 1. Filter-Related Losses

2 Design Parameters

Typically, the ADC sets the initial design parameters. For example, the ADC2RF45, has an input full-scale voltage swing of 1.35 Vpp and a common mode voltage of 1.4 V. With an input impedance of approximately 50 Ohms, the 1.35 Vpp input voltage is equivalent to approximately 7 dBm.

Working back down the signal chain from the ADC, next is the filter with expected losses of 1.5 to 2 dB. Termination resistors between the filter and the amplifier add another 3 dB (power) or 6 dB (Voltage). Because ADCs are not operated at full input amplitude, we can ignore up to 2dB of filter losses which brings the maximum voltage at the amplifier to 2.7 Vpp or 10 dBm. From the amplifier data sheet we see that a 1.4-V common mode and a swing of 2.7 Vpp is not possible on a single 5-V supply. This leaves two options, AC coupling or DC coupling but with split-power supplies. Because it is the more difficult case we will show DC coupling first.

With DC coupling selected, use the following parameters:
- Positive supply voltage, V+ = 4 V
- Negative supply voltage, V− = −1 V
- Output common mode, CM = 1.4 V
- Source resistance, R_S = 50 Ω
- Total load resistance, RL = 100 Ω (50-Ω ADC + 50-Ω filter)
- Output voltage swing, Vout Max = 2.7 Vpp
- Input common mode (set by source) = 0 V

2.1 Source Resistance

Most signal sources have some inherent resistance or impedance. Most RF sources have a specific design resistance, such as a 50-Ω, single-ended source like a mixer or a transmission line. Other sources may have a higher resistance like a 100-Ω mixer or a 100-Ω shielded twisted pair transmission line. Many fully-differential amplifiers (FDA) are capable of converting single-ended sources into a differential signal. The LMH3404 is one example.

As Figure 2 shows, there are additional resistors required to match a single 50-Ω source to the LMH3404. With the addition of two resistors, the source impedance can be matched and the effective gain of the circuit is 8 V/V. For more details on single-ended operation, see the LMH3404 product data sheet (SBOS739).
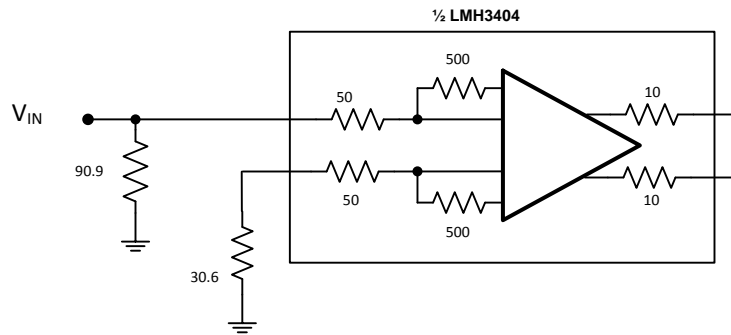
½ **LMH3404**

Figure 2. Single-Ended Input Matching

The LMH3404 has two on-chip gain set resistors of 50-Ω each, so the LMH3404 is internally matched for 100-Ω differential sources. Additional external resistors would be required to match other differential source impedances.

2.2 Source Common Mode Voltage

With the ADC common-mode voltage of 1.4 V, the ideal source common mode would also be 1.4 V. One of the benefits of using an FDA amplifier is the ability to shift common mode. The LMH3404 can shift common-mode voltages from mid-supply –2 V to mid-supply +1 V. In this example, the mid-supply voltage is 1.5 V. With a source resistance of 50 Ω and a source common mode voltage of 0-V, the amplifier input pin voltage will be approximately 80 mV or 1.42 V from the mid-supply voltage. While the static bias voltage of 80 mV is within the acceptable range, the input voltage range prevents the amplifier from achieving full output voltage swing of 2.7 V. To counter this resistors are added to the positive supply (R3 and R7). These resistors shift the amplifier input pin voltage from 80 mV to approximately 600 mV.
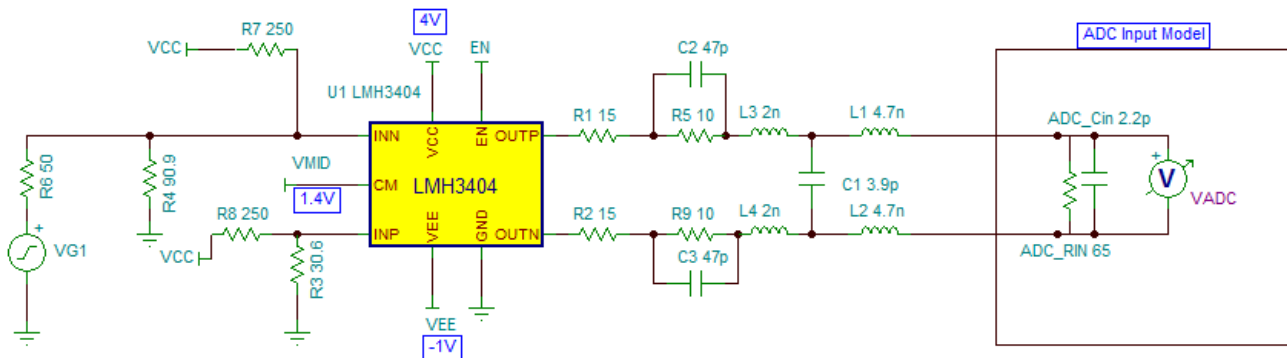

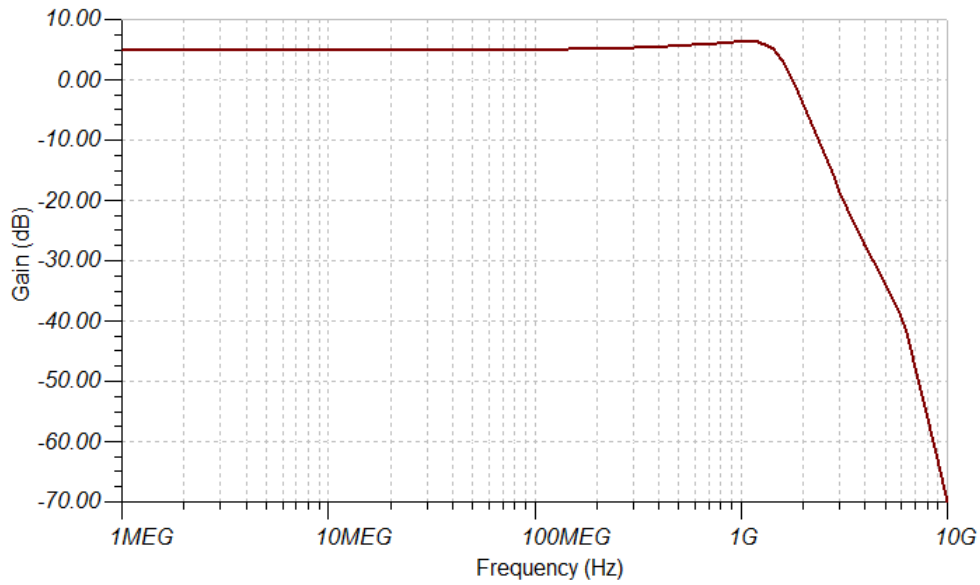**Figure 3. Single-Ended Input TINA Schematic**

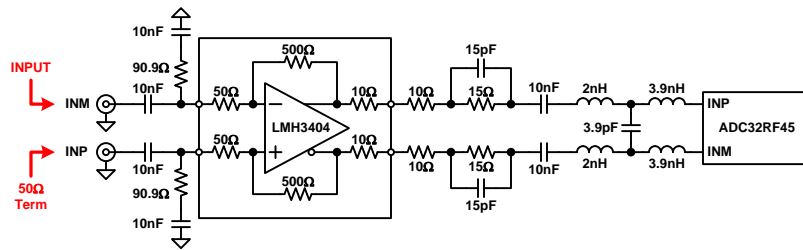**Figure 4. Filter Frequency Response Simulated**
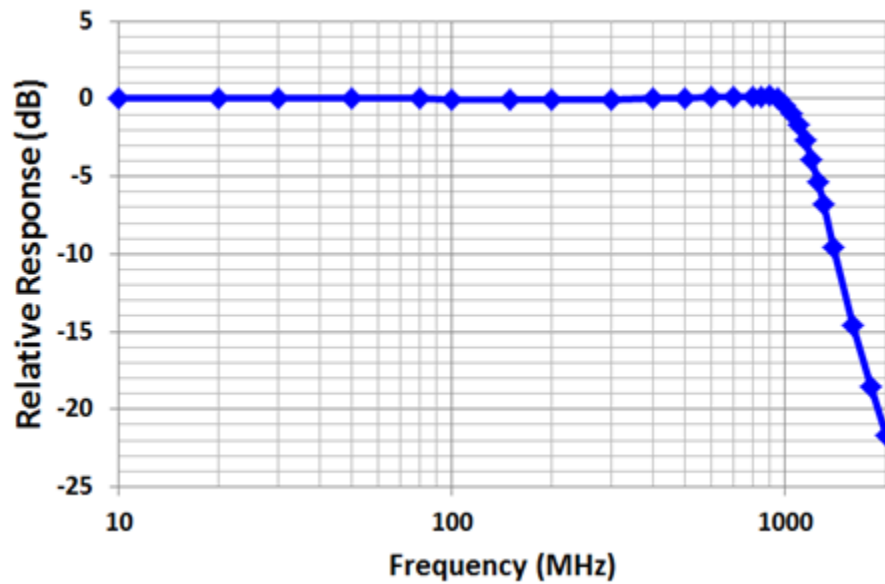

Figure 5. Single-Ended Input Circuit

Figure 6. Filter Frequency Response Measured

The figures above show a sample filter design. Figure 3 shows a TINA schematic for a 1GHz low pass filter and Figure 4 shows the simulated frequency response. The measured data follows with the schematic used shown in Figure 5 with measured response shown in Figure 6. There will be more details about the filter design in the section below Section 2.3. The reason this is covered below is that the ADC is a key part of the filter design.

2.3 ADC Input Resistance

As previously mentioned, the ADC input resistance is approximately 50 Ω. However, this approximation is not accurate enough to design a filter with a flat response. When designing a filter it is important to have as much detail on the ADC input impedance as possible. An analysis of the ADC input impedance (S11) shows that a better approximation of the ADC input impedance is 65-Ω resistance in parallel with 2.2pF capacitance. This approximation was chosen to match the ADC input impedance near the anti alias filter cutoff frequency. The ADC input impedance at lower frequencies will not impact the filter performance as much as it will near the cutoff frequency, so use these values when designing the filter. The filter response, simulated Figure 4 compared to the measured Figure 6 shows good agreement.

Because the ADC input impedance is a classical low pass filter we need to add some additional components to boost the filter response at high frequencies. The components in Figure 3 R5, R9, C2 and C3 create a high pass filter that negates most of the higher frequency losses in the filter passband. This gives a flat frequency response up to 1-GHz.

2.4 AC Coupling

Whenever an actual DC voltage is not a part of the signal being sampled, AC coupling the amplifier and the ADC should be considered. With AC coupling, the amplifier common mode voltage and the ADC common mode voltage are separated and so a single 5-V power supply can be used for the amplifier. This removes the need for a negative voltage power supply. With a single 5-V supply, the CM pin is biased to 2.5 V. The 2.5-V reference can be made from a simple resistor divider. Figure 7 shows a sample circuit with AC coupling. The sample circuit uses 100-nF capacitors for coupling. The frequency response for this circuit is shown in Figure 8. The low frequency corner is approximately 50 kHz. If lower frequencies need to be sampled, select a larger value capacitor.
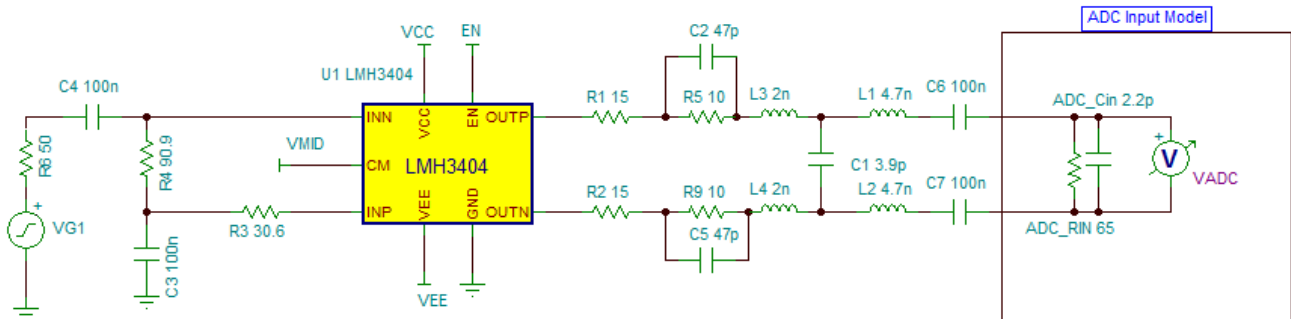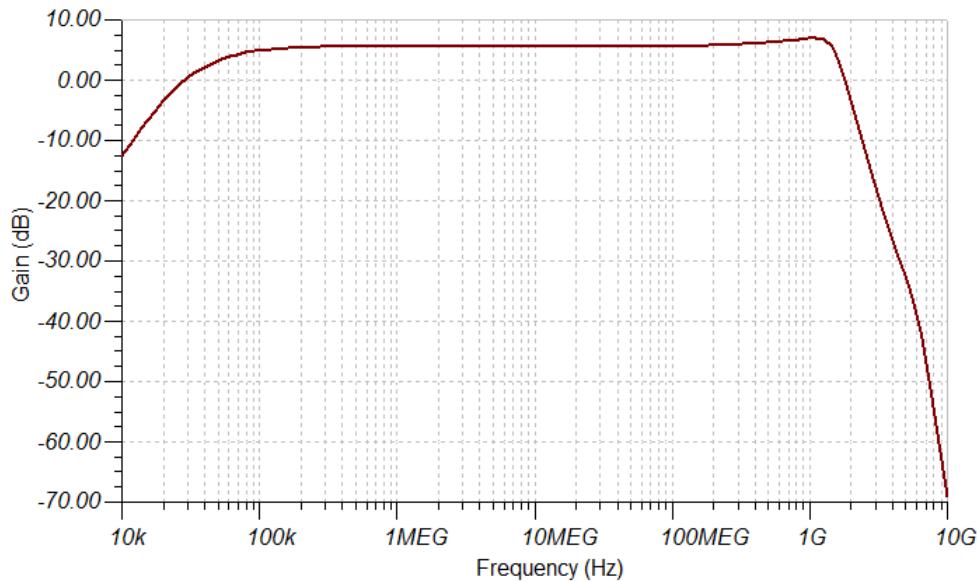

Figure 7. AC-Coupled Circuit Schematic

Figure 8. AC-Coupled Frequency Response

3 Printed Circuit Board Layout

The layout of the printed circuit board (PCB) has a dramatic influence on the system performance. Long PCB traces have a significant reactive characteristic. Inductance of long PCB traces limit system bandwidth and can also cause unwanted antenna effects. Signals on distant portions of the system board are readily picked up by long traces. When routing input and output traces for an amplifier, keep the input traces isolated from the output traces. When input and output traces are placed in close proximity there will be output-to-input coupling which could cause the amplifier to oscillate.

Power supply decoupling capacitors should be used and should be placed within 2 mm of the amplifier power pins. While bypass coupling capacitors are important, they are no substitute for using entire PCB planes to distribute power. If one entire board layer cannot be devoted to a particular supply voltage, have as much area as possible devoted to each voltage supply. See the LMH3404EVM user's guide (SBOU166) for a suggested amplifier board layout. Likewise; use the ADC32RF45EVM as a reference for the ADC layout.

Filter implementation is challenging at high frequencies as well. When laying out the filter on the PCB, it is helpful to remove ground and power planes for at least .020 in below the filter elements. This reduces the detuning of the filter response by the ground and power planes. Design filters for a frequency at least 10% higher than desired, because even with careful board design, the filter response will be shifted down. When designing a filter, make sure to carefully read the capacitor and inductor data sheets to be sure they will operate properly at the frequencies desired. Some common passive components are not specified for operation above 100 MHz.

While advancements in high performance, active circuits are making system designs more robust, there is still a need for the use of passive components. Using these filter techniques can make the most of that last passive stage in the signal path.

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