Application Report
SNOA946A–April 2016–Revised November 2018

High Voltage Half Bridge Design Guide for LMG3410x Family of Integrated GaN FETs

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ABSTRACT

As gallium nitride (GaN) power FETs become readily available for power designers to use, their promise of performance improvement with higher efficiencies and greater power densities can begin to become realized. By having better material properties over silicon, loss elements such as on-state resistance Rds(on) and output capacitance Coss are smaller for an equal die area. These GaN power FET devices, included in the LMG3410x family, are typically offered in high electron mobility transistor (HEMT) structures, which along with maximizing the material property benefits eliminate the reverse recovery Qrr when the device operates in third quadrant mode (conduction from source to drain). These benefits allow GaN power FETs to operate faster and at higher frequencies than previously capable. With typical slew rates around 30 V/ns to 100 V/ns at operating voltages around 380 V to 480 V, printed circuit board (PCB) layout optimization is even more essential since parasitic inductances and capacitances from poor layouts can drastically reduce performance or even prevent operation. When pushed to their limits to maximize system gains power GaN FETs provide the device can degrade and potentially overheat without a carefully designed thermal system to dissipate the generated heat. To prevent these problems from hampering designs and limiting performance layout recommendations, peripheral component selection and thermal system design are discussed.

Contents

Trademarks

1 Introduction

To maximize the performance benefit of the LMG3410x family of devices, a robust PCB layout is essential. While there are design rules that help improve performance for one parameter, they also can cause another parameter to become worse. This requires an understanding of all the main design tradeoffs to create an optimized layout. While following design recommendations for lower voltage GaN FETs are recommended for proper operation, the higher voltages seen by the LMG3410x devices requires special consideration to insure proper operation (see SNVA729).

1.1 Parasitic Inductance

By having smaller gate capacitance, output capacitance and on state resistance, GaN FETs are able to switch much faster with less loss. The LMG3410x devices have a user-controllable slew rate from 30 V/ns to 100 V/ns. While this helps reduce the power loss during each switching transition, it also increases the voltage and current slew rates. As Equation 1 shows, by increasing the current slew rate the voltage induced across any parasitic inductor is increased, increasing voltage overshoot on the power device.

$$V = L_{lk} \frac{di}{dt} \tag{1}$$

where

- L_{lk} is the parasitic inductance
- di/dt is the change of current with respect to time
- V is the induced voltage

Since high slew rates are desired to minimize switching transitions and reduce loss, it is important to keep the parasitic inductance as small as possible. One key current loop is the switching cell and bypass capacitor. Figure 1 highlights this loop for a half bridge configuration, which includes the high side FET, low side FET and bypass capacitor.

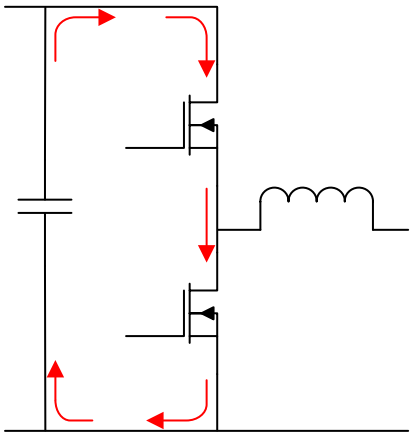

Figure 1. Critical Power Stage Current Loop

Any closed current loop has an inductance, which can be approximated with Equation 2 (see *Inductance Formulas for Circular and Square Coils*).

$$L_{trace} \approx \frac{\mu_0 \mu_r h}{W} l \tag{2}$$

where

- μ_0 is the permeability of free air ($4\pi \times 10\text{-}7$)
- μ_r is the relative permeability (1 for FR-4)
- h is the space between conductors
- w is the width of the conductor
- l is the length of the conductor
- L_{trace} is the parasitic inductance of the trace

The parasitic inductance Ltrace can be minimized by reducing the space between traces h and length l while maximizing the width w. By placing all the components on the top layer of a PCB, and have the return path on the next layer of copper, the space between conductors h can be greatly reduced, creating an optimal layout (see *Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter*).

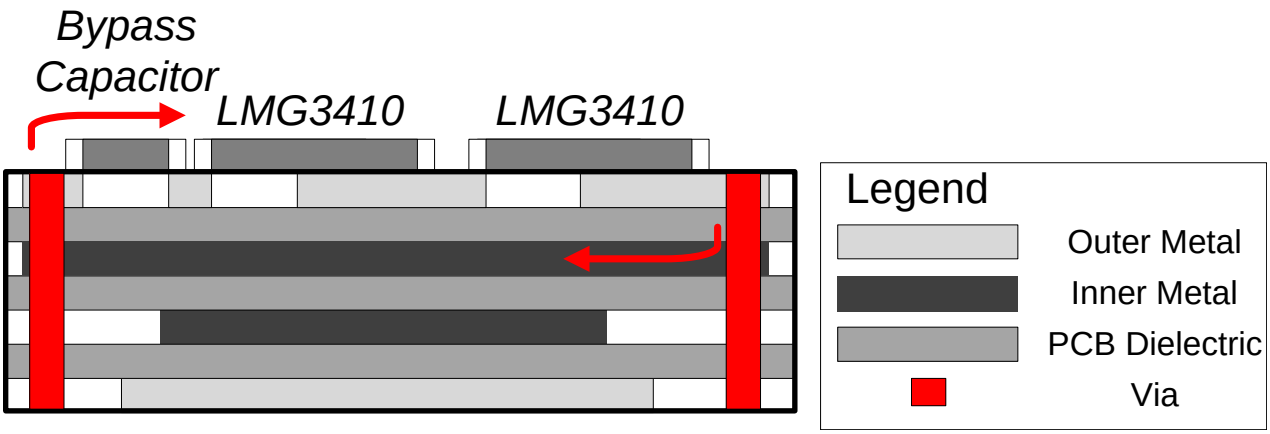

Figure 2. Optimal Layout (Cross-Section View)

By reducing this inductance with an optimized layout, the voltage overshoots that increase stress and losses are reduced, improving performance of the LMG3410x devices.

1.2 Parasitic Capacitance

1.2.1 PCB Layout

To properly layout PCBs that utilize GaN, multiple layer boards are required. Any time when a multilayer board is designed, copper overlaps between key nets need to be minimized to prevent undesired parasitic capacitors from being created and hurting performance. One key net that needs to be taken into consideration is the switch node, which is highlighted on Figure 3. Any capacitance from this node to ground or input voltage leads to additional energy that is dissipated through the GaN FET during turn on, increasing switching loss. Layouts that minimize the parasitic inductance by with large ground return current loop widths can have large parasitic switch node capacitance if not properly accounted for.

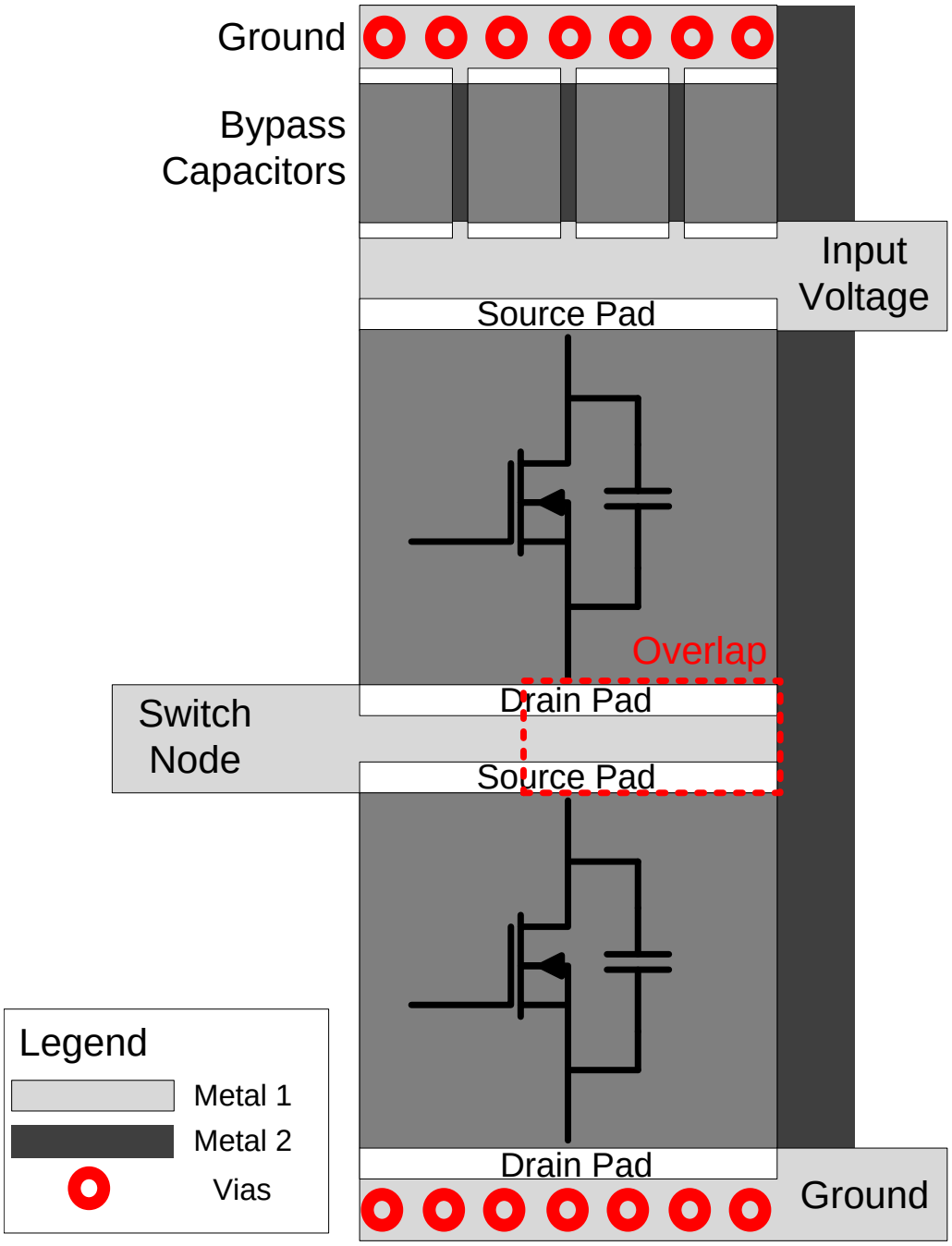

Figure 3. Parasitic Capacitance Example

The parasitic capacitance from a PCB can be approximated with Equation 3 (see SLYP173).

$$C = \frac{0.0886 \varepsilon_r A}{h} \quad (3)$$

where

- h is the distance between copper layers in cm
- A is the overlapping area in cm^2
- ε_r is the relative permittivity (4.5 for FR-4)
- C is the capacitance in pF

For example, if a board that has 5 mils between the switch node and ground return and has an overlap area of 0.64 cm^2 (the area of the LMG3410R070), then the additional capacitance is 20 pF. The LMG3410R070 output capacitance is only 90 pF under high Vds bias, which makes this capacitance a significant term that increases the total effective capacitance by 22%. This capacitance can increase the power loss dissipated by the LMG3410R070 during turn on, and can be approximated with Equation 4 (see SLYY071).

$$P_{cap} = \frac{1}{2} f_{SW} C_{OSS} V_{IN}^2 \quad (4)$$

where

- f_{sw} is the switching frequency
- C_{oss} is the output capacitance
- V_{IN} is the input switching voltage
- P_{cap} is the power loss

For example, at 140 kHz and 380 V, a capacitance of 20 pF will increase the loss dissipated by the active switched LMG3410R070 by 0.4 W. The capacitance of the ground-return path underneath the die attach pad (DAP) of the LMG3410R070 and the switch-node copper needs to be minimized, for example, by increasing the gap between the different PCB layers and reducing trace widths.

1.2.2 Heatsink

Another source of parasitic capacitance is the heatsink. Typically conductive materials such as aluminum are used to sink heat away. If one heatsink is used to cool two LMG3410x family devices in a half bridge, an insulating thermal interface material (TIM) is required. The LMG3410x family of devices dissipate heat through the die attached pad (DAP), which is also electrically connected to the source. In a half bridge configuration, this means the heatsink is capacitive coupled to the switch node and ground.

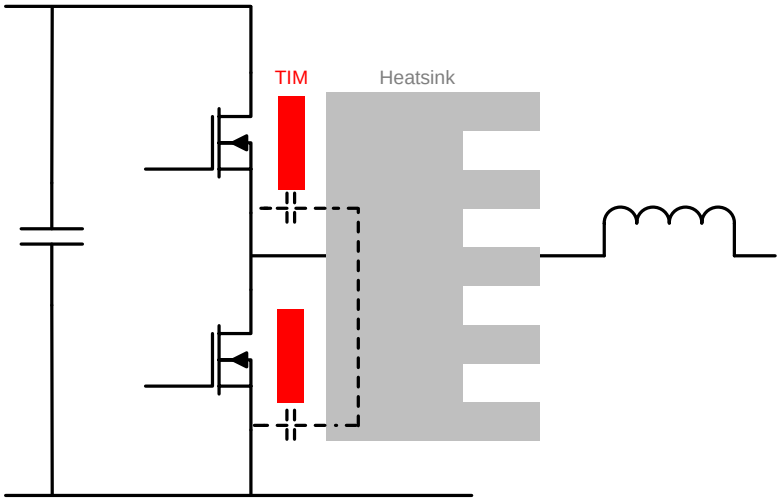

Figure 4. Parasitic Capacitance from Floating Heatsink Connection in Half Bridge Configuration

By sharing a heatsink in this configuration, a parasitic capacitance exists from switch node to ground. If the heatsink is grounded, this parasitic capacitance is increased. This means that a large copper plane to allow for high thermal conductivity to the heatsink may not be optimal for parasitic capacitance. High thermal conductivity and low parasitic capacitance should be traded off in system level to achieve optimal performance. Sometimes, it could become necessary to slip top-side and bottom-side heatsinks and ground differently. Thermal considerations are further discussed in the thermal section.

1.3 Interference

Even with the best design, the power stage switching still causes interference in the bias power and logic signals. This coupling can disturb sensitive logic signals, especially around the gate drive. Poor layouts can result in overshoots large enough to inadvertently turn on devices, creating damaging shoot through events, increase loss with unintended turn-off glitches or corrupting fault signals to trigger false events. This interference can be reduced by minimizing copper overlaps between nets that have large voltage swings, such as the switch node. Low pass RC filters on the input and fault signals are recommended to filter out any undesired ringing.

2 Component Selection

The performance of the LMG3410x family is largely dependent on the components that it interfaces with. To maximize the performance and prevent unforeseen problems from interfering with operation, proper component such as capacitors, diodes, and integrated circuits need to be selected.

2.1 Decoupling/Bypass Capacitor

Typically for high voltage systems, large bulk film or electrolytic capacitors are used to hold up the DC bus. While sufficient for low frequency operation, these capacitors do not perform well at the very high slew rates that the LMG3410x family operates at due to their large size and series inductance. To compensate for this, high quality surface mount capacitors are required to be placed in parallel. High quality ceramics with X7R or NP0/C0G dielectrics are recommended due to their low variation over temperature and voltage. By being in surface mount packages the parasitic inductance is significantly reduced and much tighter current loops can be achieved with the optimal layout discussed earlier, minimizing voltage overshoot during switching transitions.

The LMG3410x family of devices require three bias power supply bypass capacitors for VDD, LDO5V, and VNEG. To allow for these capacitors to properly supply the high speed transitions and filter out switching interference, they need to be placed as close as possible to the LMG3410x device. Figure 5 shows how to achieve this, with C9 bypassing VNEG, C5 bypassing the 5 V, and C8 bypassing VDD. It is recommended to keep all components and traces on the same layer.

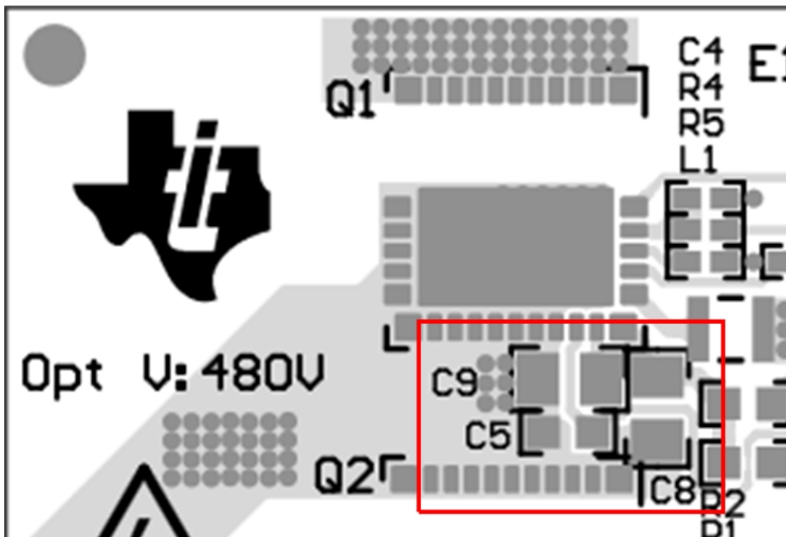

Figure 5. Layout of Aux Bypass Capacitors (C9, C5, C8)

2.2 Gate Driver

GaN FETs have gate structures that can require tight tolerances or negative voltages. By integrating the driver, the LMG3410x device family eliminates all these concerns for designers and only requires a single 12-V nominal supply.

2.3 High Side Level and Power Shifting

To supply logic and power to properly drive a high side device, level shifting needs to be provided externally to the LMG3410x devices. Design considerations need to be taken into consideration when selecting them, or else they will introduce adverse behaviors that will limit or prevent operation.

2.3.1 High Side Level Shifting

To convert logic signals from the controller to a high side device, a logic level shifter must be used. Digital isolators are recommended due to their low propagation delay. Isolators with high common mode transient immunity (CMTI) are required, since many standard isolators are only rated to 50 V/ns or less. Edge triggered isolators are not recommended since the interference generated by the high slew rates of the power stage can cause false triggers, causing circuit malfunction. On/off keyed isolators, such as the Texas Instruments ISO78xxF series isolators, are recommended since simple RC low pass filters on the inputs can eliminate any false pulses caused by high slew rates.

2.3.2 High Side Isolated Power

The recommended way to power the LMG3410x devices when configured as a high side device is with an isolated power supply, such as the Texas Instruments DCP010512BP-U. A power supply with low capacitance from the input to output must be used since this directly leads to additional capacitance at the switch node, increasing loss and creating a path for the switching transition to introduce interference in the logic signals.

2.3.3 High Side Bootstrap Power

While a transformer-isolated power supply is recommended to power the LMG3410x devices, a bootstrap supply can be used with the following recommendations. The LMG3410x family of devices can be configured to operate with a bootstrap supply as Figure 6 shows.

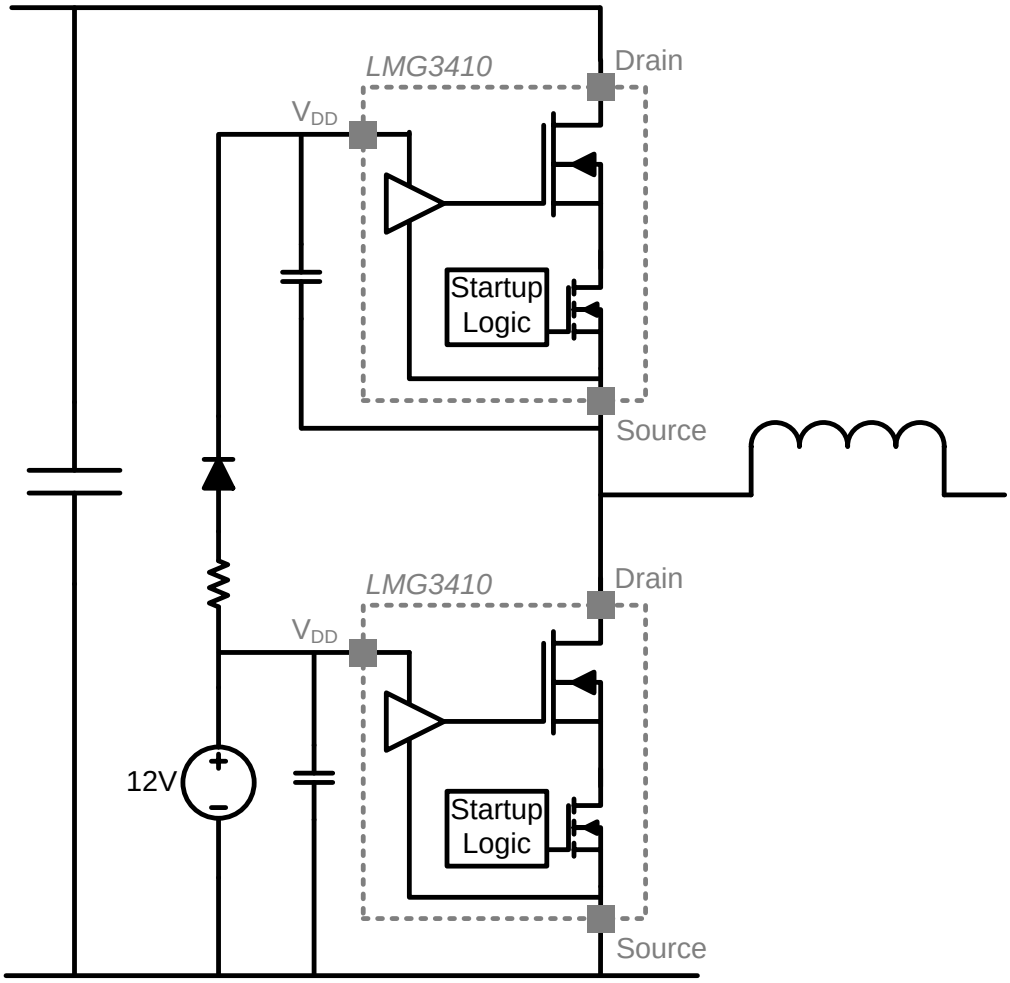

Figure 6. LMG3410x Configured as Bootstrap

To properly implement the bootstrap supply, there are several design considerations that need to be taken into consideration. During high frequency operation, the reverse recovery of this diode can become significant, which limits the minimum pulse widths and becomes a significant source of loss. To mitigate these problems an ultrafast diode, such as a Micro Commercial UFM15PL-TP, is recommended. Also, for control purposes in half bridge configurations, the high side device will not power on and clear any active low fault signal on the FAULT pin until the low side device is turned on to allow the bootstrap supply to charge.

With bootstrap operation it is recommended to slow down the slew rate during startup to 30 V/ns. This can be achieved by placing two resistors in parallel from RDRV to ground with one resistor enabled with a logic FET, as shown with Figure 7. During startup the high side fault signal is low, causing the resistance at RDRV to be equal to R2, which is 100 kΩ. This sets the slew rate at the minimum 30 V/ns. When the high side turns on, the high side fault signal turns on Q_{RDRV} and the slew rate is changes to the resistance of R1 in parallel with R2. The desired steady state operating slew rate can be set by R1 as shown with Equation 5.

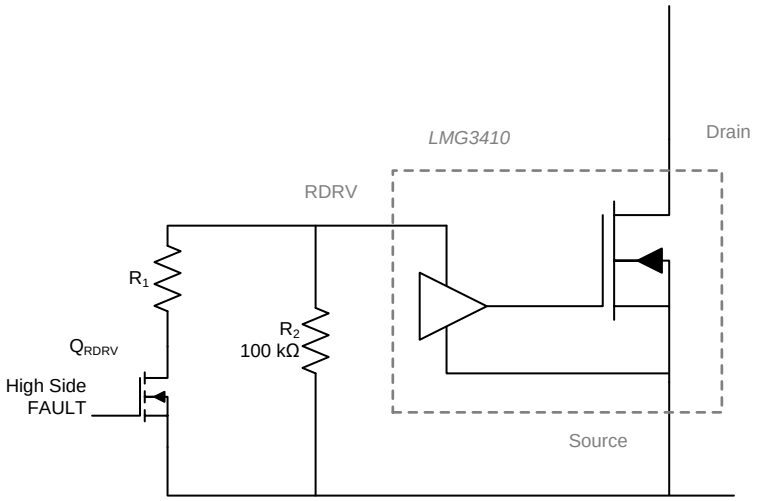

Figure 7. LMG3410x Slew Rate Startup Adjustment Circuit

$$R_{DRV}(\text{steady state}) = \frac{100\ k\Omega \times R_1}{100\ k\Omega + R_1} \quad (5)$$

One issue that many GaN FET designs have to compensate for is proper regulation of the bias voltage for the high side. During third-quadrant operation, the voltage drop from source to drain of the bottom FET may cause the high side bias voltage to overcharge by several volts. By integrating a voltage regulator on chip to provide the necessary voltages, the LMG3410x devices mitigate this problem by being able to operate with a V_{DD} of up to 18 V.

3 Thermal Design Considerations

While GaN FETs such as the LMG3410x family of devices have less loss when compared to silicon FETs, they can still get hot when pushed to their operating limits. To insure that these losses do not overheat the device, a properly designed thermal system is required. While the LMG3410x devices will protect against extreme over-temperature events, a properly designed systems will prevent nuisance trips of the fault protection features.

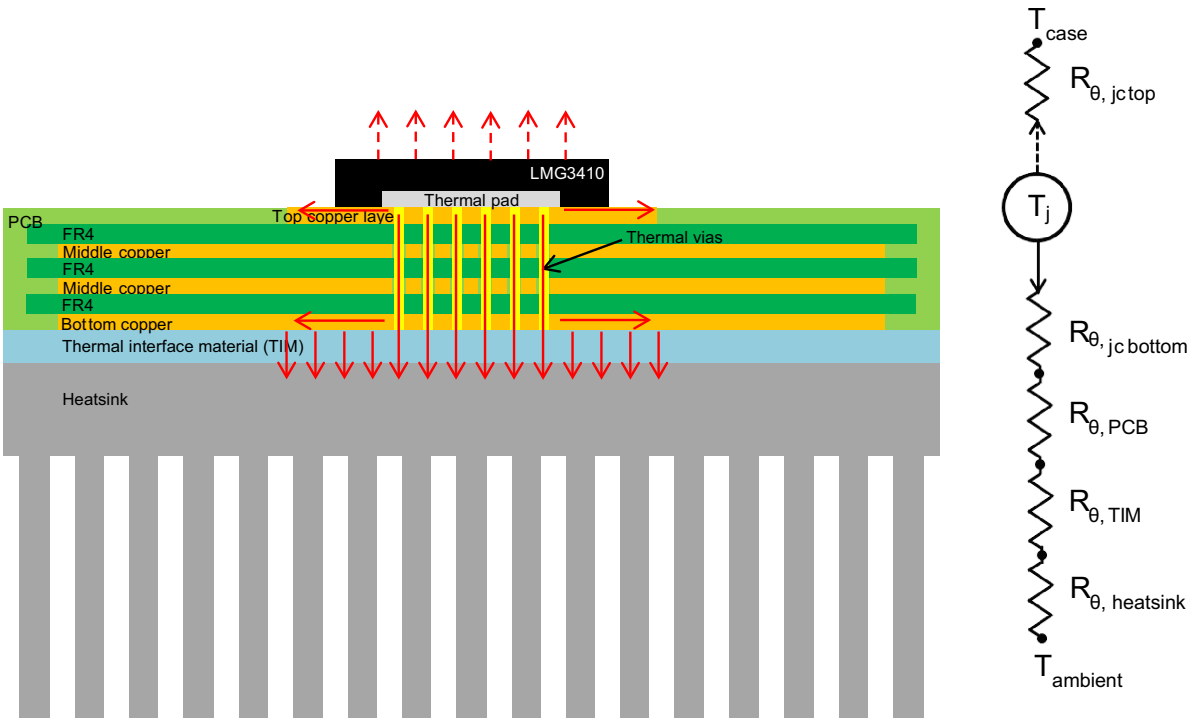

Figure 8. Typical System Stack Up and Major Thermal Resistance

The LMG3410x devices are designed to dissipate heat via the bottom of the package. System-level thermal performance of LMG3410x is influenced by topology, PCB design, thermal interface material (TIM) and active cooling system. In a typical bottom-cooled configuration, system thermal resistance consists of parts shown in Figure 8. There are two thermal paths for heat dissipation. The bottom path, depicted by solid arrows in Figure 8, is the major thermal path. The top path, depicted by dotted arrows in Figure 8, is minimal compared to the bottom path. In a typical bottom-cooled configuration, where thermal vias, finned heatsink and sufficient air flow are used, less than 10% of the dissipated heat goes through the top path. Therefore, thermal resistance of the bottom path dictates the thermal performance of LMG3410x in a bottom-cooled application. Thermal resistance of the bottom path can be further broken down into package resistance $R_{\theta(jcbottom)}$, PCB resistance $R_{\theta(PCB)}$, TIM resistance $R_{\theta(TIM)}$, and heatsink resistance $R_{\theta(heatsink)}$. Junction temperature can be estimated with Equation 6.

$$T_j = P_{loss} \times R_{\theta ja} + T_A \quad (6)$$

where

- T_j is junction temperature
- T_A is ambient temperature
- P_{loss} is total dissipated power
- $R_{\theta ja}$ is the total thermal resistance

$R_{\theta ja}$ can be approximated with Equation 7:

$$R_{\theta ja} = R_{\theta jc(bottom)} + R_{\theta(PCB)} + R_{\theta(TIM)} + R_{\theta(heatsink)} \quad (7)$$

where

- $R_{\theta jc(bottom)}$ is thermal resistance between junction of the die and package DAP
- $R_{\theta(PCB)}$ is thermal resistance of the PCB
- $R_{\theta(TIM)}$ is the thermal resistance of the TIM
- $R_{\theta(heatsink)}$ is the thermal resistance of the heatsink

Since Tj is a constant set by GaN material, reducing $R_{\theta ja}$ increases the power output of LMG3410x devices and also allows it to operate at higher ambient temperature. Thermal optimization can be achieved by reducing $R_{\theta jc(bottom)}$, $R_{\theta(PCB)}$, $R_{\theta(TIM)}$, and $R_{\theta(heatsink)}$ (see SPRABI3). $R_{\theta jc(bottom)}$ is an intrinsic property of LMG3410x, which has been optimized by package design and material selection. The following discussion will focus on thermal optimization of LMG3410x family via PCB design, TIM selection and heatsink selection.

3.1 PCB Thermal Optimization

3.1.1 Top Copper Layer

Just like electric resistance, thermal resistance is not an intrinsic material property. It is a function of material thermal conductivity and material dimensions, in a simple one-dimensional case:

$$R = \frac{t}{KA} \quad (8)$$

where

- t is material thickness
- A is material area
- K is material thermal conductivity

When the heat source area is smaller than the heat drain area, thermal conduction takes a 3-dimensional form and spreading resistance will come into play (see *Spreading Resistance in Cylindrical Semiconductor Devices*). The top surface of the copper layer can be viewed as the heat source, which is defined by the package thermal pad, and the bottom surface can be viewed as the heat drain. As the copper layer size increases, due to heat spreading, the effective thermal resistance in the vertical direction decreases and reaches saturation beyond a certain point, which is determined by the copper thickness. In general, it is beneficial to have a larger and thicker top copper layer. Since FR4 material in the PCB is a much poorer thermal conductor, only very limited heat spreading is expected in it. Heat spreading in top copper layer determines the heat conduction area through the FR4. As Equation 8 shows, increasing the area reduces the thermal resistance. Therefore, the overall thermal resistance of the PCB is reduced when a larger top copper layer is used. When other design constraints, electrical performance, cost, board dimensions, and so forth are satisfied, a larger top copper layer is preferred for thermal optimization.

3.1.2 Internal Layers and Thermal Via

Thermal performance of PCB can also be improved by utilizing internal layers and thermal vias, as shown in Figure 9.

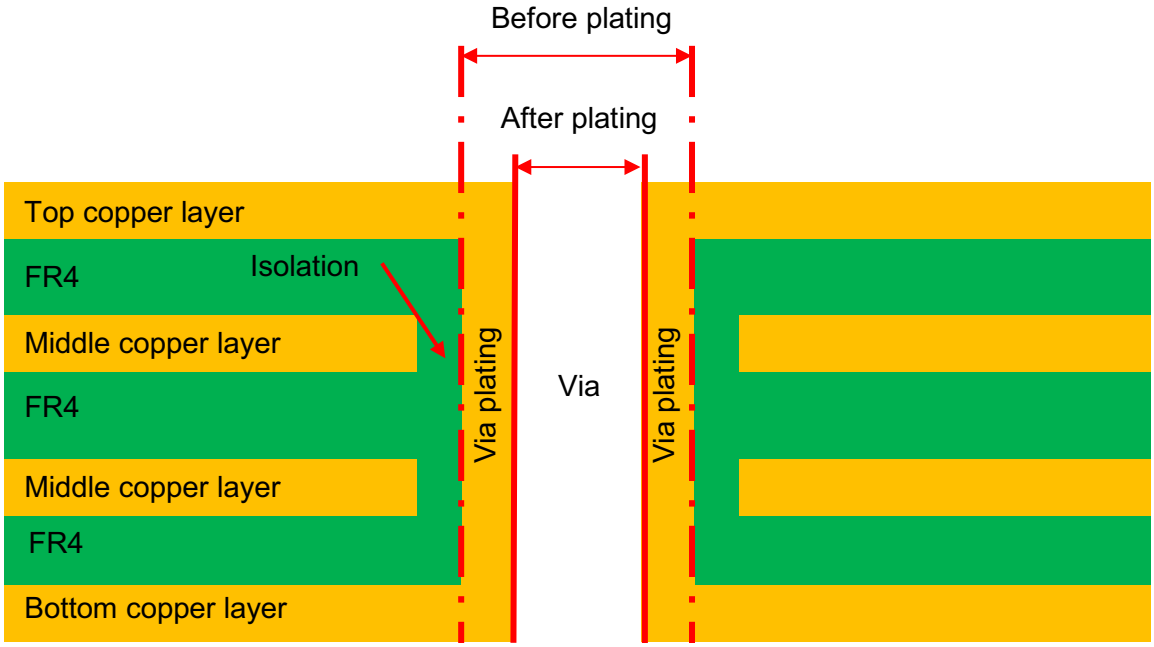

Figure 9. Schematic of a Thermal Via (Not to Scale)

In terms of heat dissipation, internal layers of PCB functions in a similar way as the top copper layer. These layers spread out the heat flux, increase the heat conduction area, and reduce the overall thermal resistance of the PCB. Therefore, thick internal layers with high coverage rate are preferred.

Another approach for improving PCB thermal performance is using thermal vias. By connecting the top copper layer with the bottom layer, thermal vias allow heat flow to bypass the low-thermal-conducting FR4 layers. Therefore, the overall effective thermal conductivity of the PCB is improved. Thermal vias are normally formed by mechanical drilling. Since air is a poor thermal conductor, a plated copper layer on the via inner surface is needed to conduct heat vertically through the PCB. For better thermal performance, higher via plating thickness is preferred. To further improve the effect of thermal vias, the air gap can be filled with high thermal conductive epoxy or even filled with copper. In terms of thermal performance, it is beneficial to connect thermal vias with internal copper layers, which promote vertical and lateral heat flow simultaneously. Therefore, if no electrical isolation is violated, it is preferred to connect thermal vias to the internal copper layers. More in-depth discussions on thermal vias can be found in (see SNVA419 and SLMA002).

3.2 TIM Thermal Optimization

Thermal interface material (TIM) between the heatsink and PCB is recommended to fully harness the performance potential of LMG3410x devices. There are many different types of commercially available TIMs, such as thermal grease, phase change material, thermal gel, adhesive tape, and filled polymer pad. Constituents, thermal performance, electrical isolation performance, and assembly complexity of these TIMs are summarized and compared in Table 1, based on a survey of major suppliers.

Table 1. Commercially Available Thermal Interface Materials

TIM NAME	MATERIAL	THERMAL PERFORMANCE	ELECTRICAL ISOLATION	ASSEMBLY
Thermal Grease	High-thermal conductivity particles (Al_2O_3 or BN) dispersed in silicone or non-silicone matrix	High	No	Moderate
Phase Change Material	High-thermal conductivity particles (Al_2O_3 or BN) dispersed in phase-change polymer (polyolefin, epoxy, polyesters, or acrylics) Can be laminated on carriers (Al foil, polyimide, or fiberglass) for mechanical or dielectric strength	High	Yes(1)	Difficult
Thermal Gel	High-thermal conductivity particles (Al_2O_3 or BN) dispersed in silicone or non-silicone matrix	Medium	No	Moderate
Adhesive Tape	High-thermal conductivity particles dispersed in silicone or non-silicone matrix and reinforced by glass fiber carrier or PET liner	Low	Yes(1)	Easy
Filled Polymer Pad	High-thermal conductivity particles (Al_2O_3 or BN) dispersed in silicone or non-silicone matrix Reinforced by glass fiber or polyimide film for improved mechanical and dielectric strength	Medium	Yes(1)	Moderate

(1) Only applies to the variants using insulation-reinforcing carriers, such as polyimide film, glass fiber, and PET liner. Other variants may not be electrically isolative.

Thickness and thermal conductivity are two of the most important parameters in TIM selection for LMG3410x. Depending on the TIM type, thickness can range from a few microns to a few millimeters. In general, a thinner TIM is preferred for lower thermal resistance. However, if electrical isolation between the PCB and the metal heatsink is needed, sufficient TIM thickness and material is needed to ensure the required isolation. Additional dielectric strength can be provided by purchasing a TIM where the thermal conducting polymer composite is laminated to a reinforcing carrier, such as glass fiber and polyimide film. This lamination approach also improves the mechanical strength of the TIM, which can prevent shorts caused by punctures from metal burs on the heatsink. Since the reinforcing material tends to have low thermal conductivity, this lamination approach reduces the overall thermal conductivity of the TIM.

For applications that require electrical isolation, such as half bridge configurations where two LMG3410x devices share the same heatsink, thermal grease and thermal gel are not recommended due to their poor and inconsistent dielectric strength. Phase change materials with dielectric reinforcement can excel in both thermal performance and electrical isolation. However, they tend to form voids over time, which can potentially create weak spots and compromise the dielectric strength. Therefore they are not recommended for the LMG3410x family.

Adhesive tape and filled polymer pad with fiber glass or polyimide reinforcement are recommended for the LMG3410x devices. In applications where large heat dissipation is expected, filled polymer pad is recommended due to its better thermal performance. However, filled polymer pads normally require pressure to achieve their claimed thermal performance. Therefore, a clamping mechanism is needed to press the heatsink to the PCB, which increases the assembly complexity and increases the system cost. In applications where a compromise between the thermal performance and the assembly complexity needs to be made, adhesive tape can be a viable TIM selection. In this case, the heatsink can be directly attached to the PCB without introducing any clamping mechanism, which reduces the assembly complexity and the system cost.

3.3 Heatsink Selection

To improve the thermal dissipation of the LMG3410x family of devices, a heatsink is recommended. By connecting a heatsink, the thermal resistance can be reduced since the heat dissipation to the surrounding air is greatly improved.

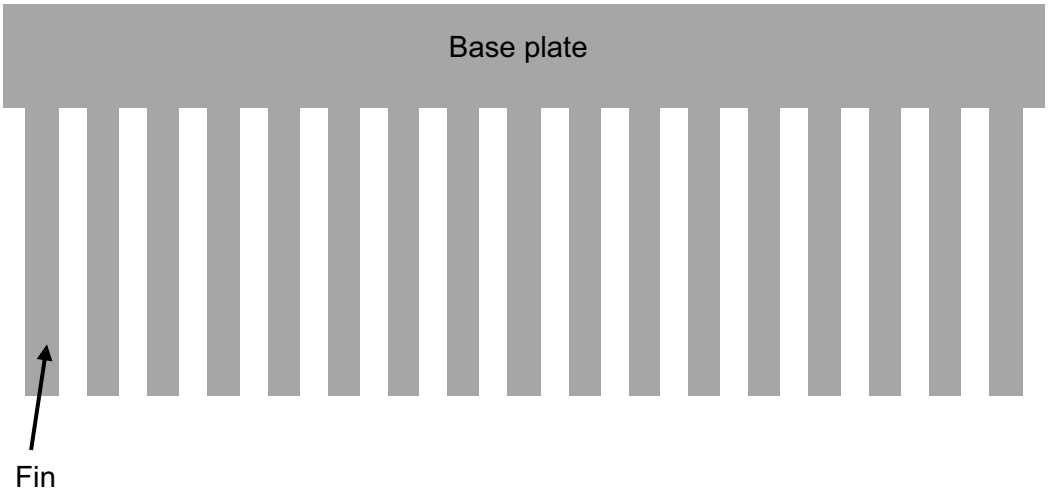

Figure 10. Schematic of a Heatsink

Heatsinks are made out of materials with high thermal conductivity, such as aluminum and copper. As shown in Figure 10, a typical heatsink consists of a base plate and a series of fin plates. To insure the heatsink conducts heat well a large copper pad connected to the DAP of the LMG3410x needs to be attached to the base plate. It is important to insure that the pad does not become too large though, since heatsinks are often times made out of electrically conductive materials and can create undesired parasitic capacitance that can hurt performance. By having fins the surface area is increased, improving the ability to dissipate heat into the surrounding air. The amount of heat that a heatsink can dissipate is quantified by its thermal impedance $R_{\theta(heatsink)}$, which is typically specified in °C/W and ideally is as low as possible. To insure that this resistance is as small as possible active cooling, which involves blowing air across the fins with a fan, is recommended for higher power applications. Typical heatsink data sheets include $R_{\theta(heatsink)}$ and airflow recommendations. It is recommended to select a heatsink by calculating the required $R_{\theta(heatsink)}$ with Equation 6 and Equation 7, then selecting one with an equal or lower resistance. Excessively large oversized designs are not recommended since they unnecessarily increase cost and increase parasitic capacitance impact (see *How to Select a Heatsink*).

4 Example PCB Layout

To demonstrate the layout recommendations, an example half bridge layout of two LMG3410R070 devices is shown.

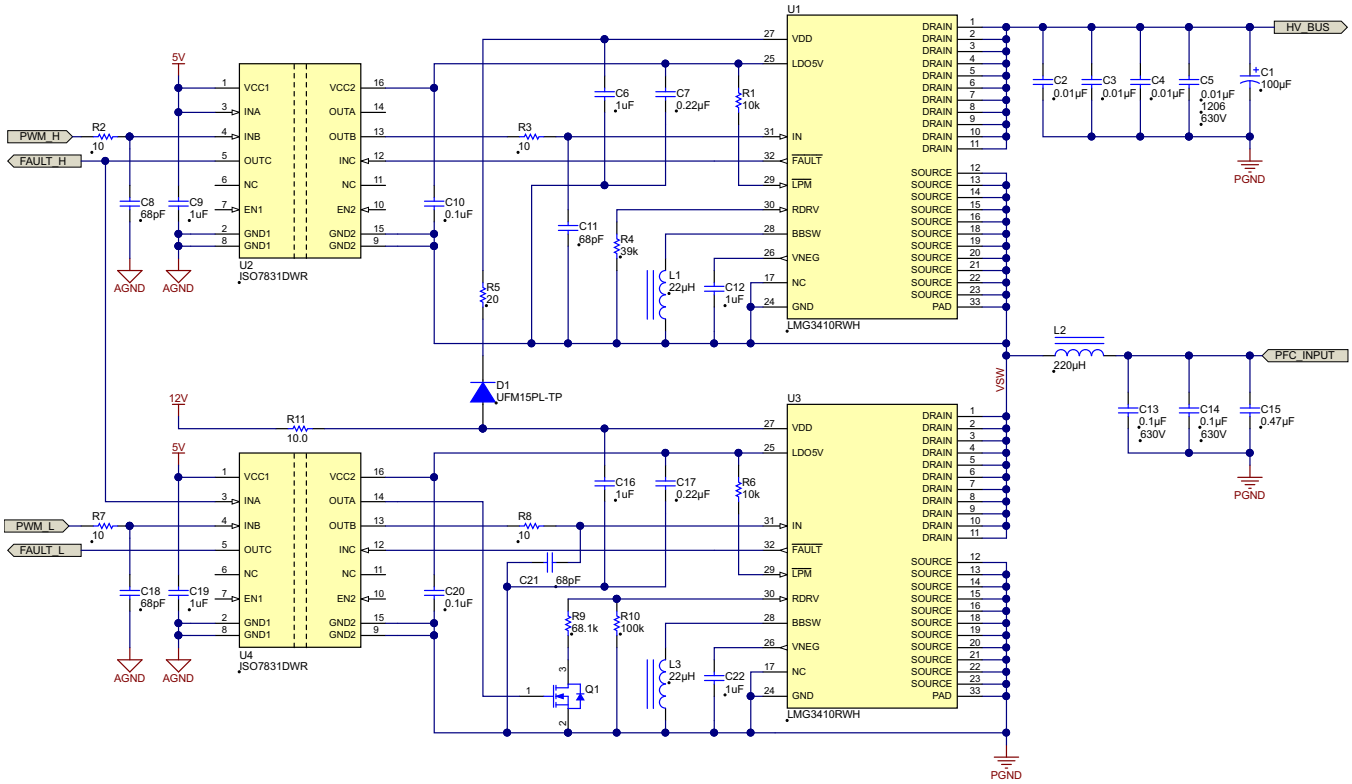

Figure 11. Schematic of Example LMG3410R070 Power Stage

It is recommended to keep all the key components used with the LMG3410R070 on the same layer. A multilayer board with a modified layer stack-up to minimize distance between the layer that the components are on and first internal layer of copper, while maintaining high voltage spacing requirements, is recommended. The example layout has all the components on the top layer and the mid-layer 1 copper only has a spacing of 5 mils.

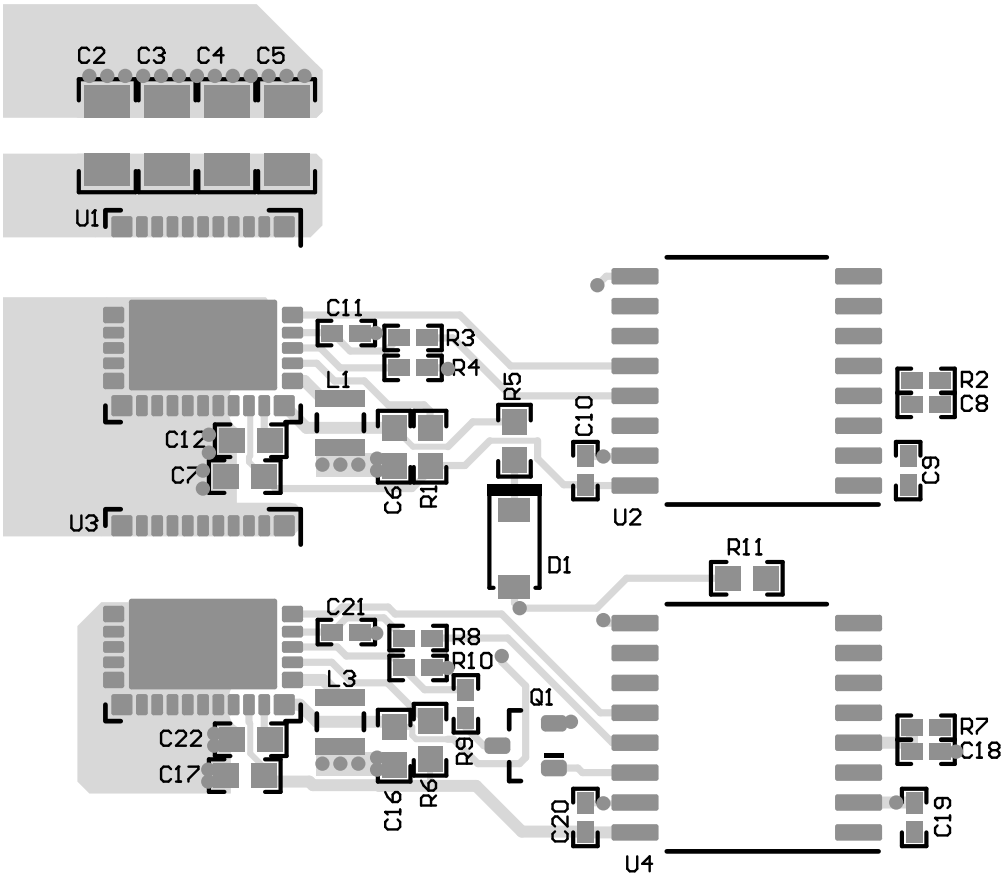

Figure 12. Top View of Example Power Stage

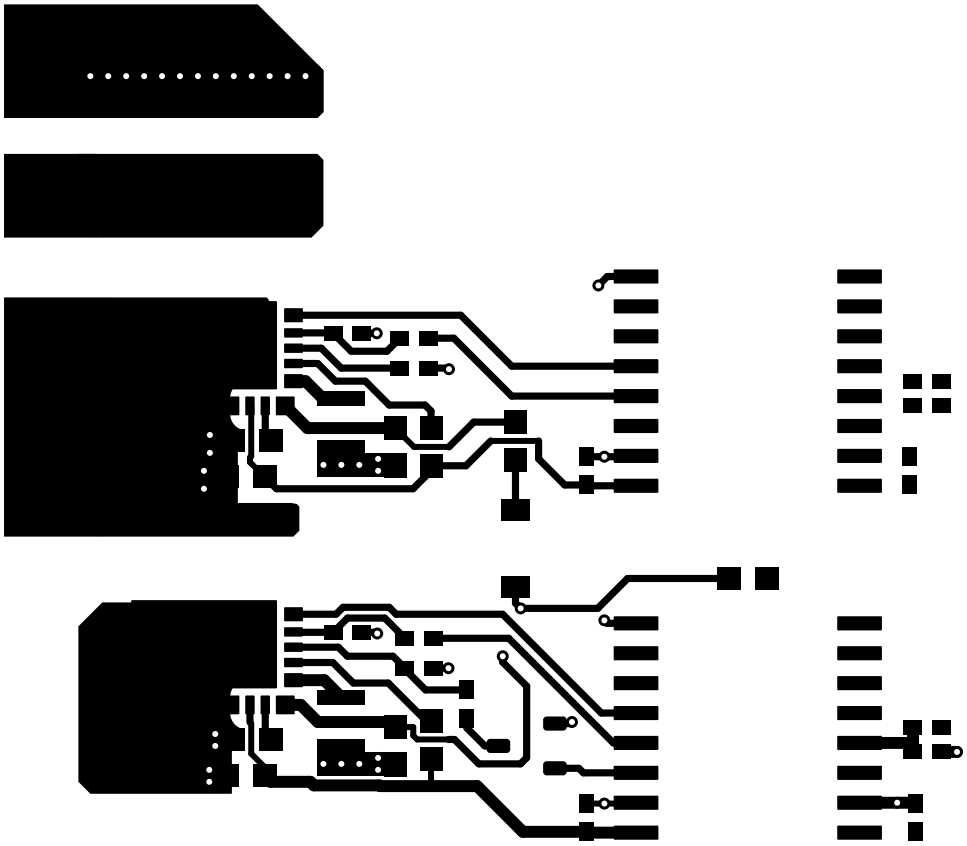

Figure 13. Top Copper of Example Power Stage

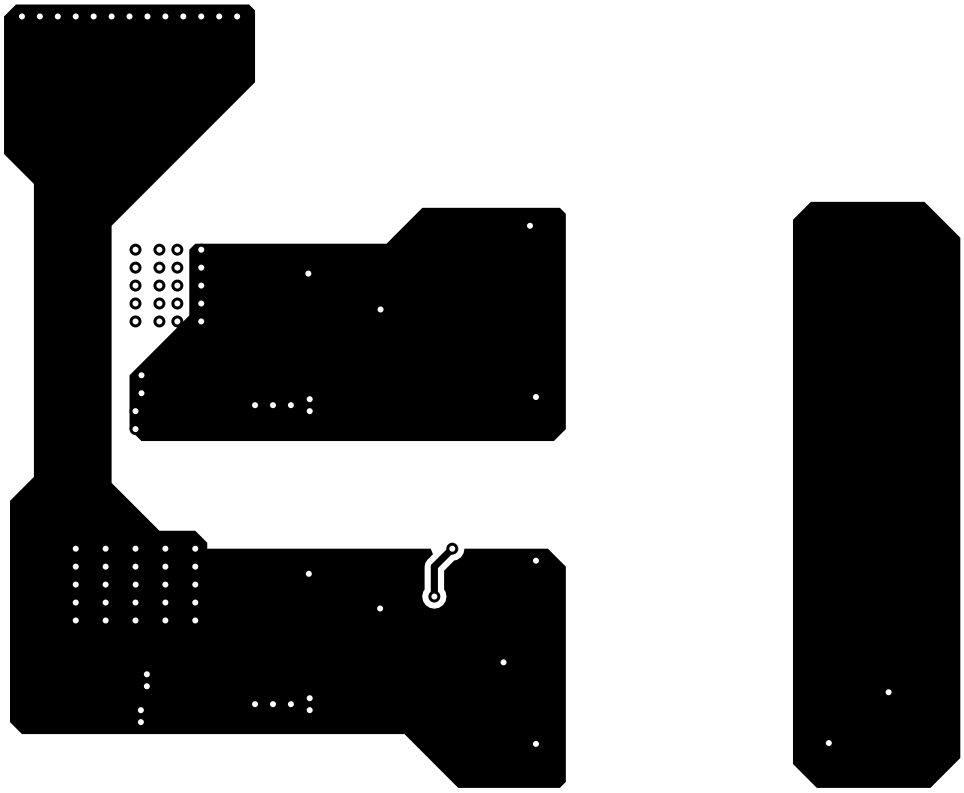

Figure 14. Mid-Layer 1 Copper of Example Power Stage

5 Example Results

To demonstrate the design tradeoffs the LMG3410-HB-EVM, which consists of two LMG3410x devices configured in a half bridge with the discussed design recommendations is measured under operation. As the waveforms show on Figure 15 when operated at 480-V input, 5-A output, and 100-kHz switching frequency with 50% duty cycle the voltage overshoot and ringing on the device is low and causes no problems. The thermal system performance is measured under these operating conditions with a fan blowing air across the device and heatsink, and as Figure 16 shows the case temperature stays within recommended operating conditions.

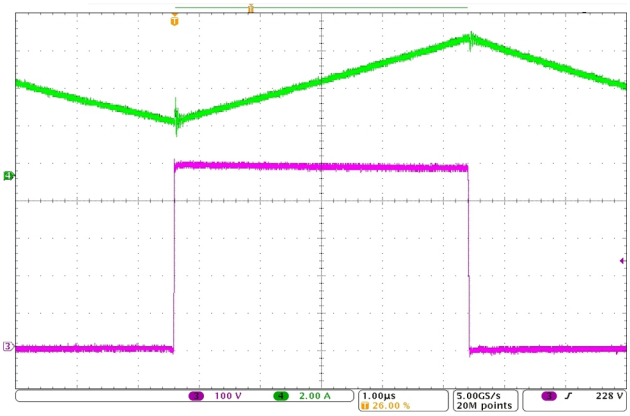

Figure 15. Power Stage Waveforms of LMG3410-HB-EVM (Top Switch Node Inductor Current, Bottom Switch Node Voltage)

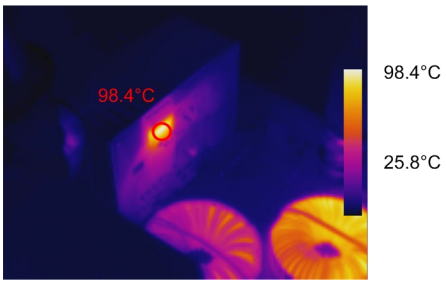

Figure 16. Thermal Measurement of LMG3410-HB-EVM

6 References

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to A Revision	Page
• In this revision, the guidelines for half-bridge design are described not just for a single device, LMG3410 (now known as LMG3410R070) but for the entire family of devices	2

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